4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 4 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-5, -6 or -7), power consumption (Normal, Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 4Mx4 EDO DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for high level computer, microcomputer and personal computer.

FEATURES

- Part Identification
  - KM44C4004B/B-L (5V, 4K Ref.)
  - KM44C4104B/B-L (5V, 2K Ref.)
  - KM44V4004B/B-L (3.3V, 4K Ref.)
  - KM44V4104B/B-L (3.3V, 2K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-5	324	396	495	605
-6	288	360	440	550
-7	252	324	385	495

- Refresh cycles

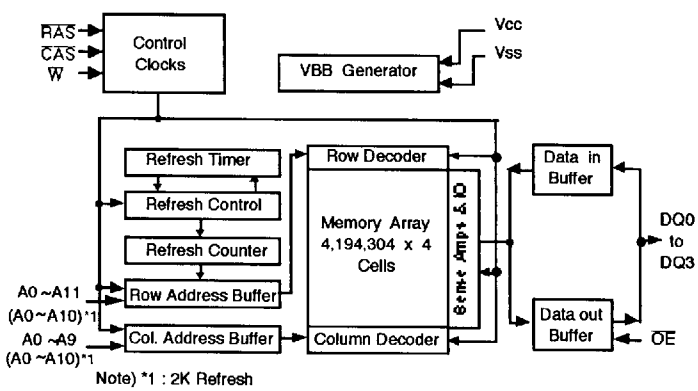
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L
C4004B	5V	4K	64ms	128ms
V4004B	3.3V			
C4104B	5V	2K	32ms	
V4104B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	13ns	84ns	20ns	5V/3.3V
-6	60ns	15ns	104ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V

- Extended Data Out mode operation (Fast Page Mode with Extended Data Out)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- Fast parallel test mode capability
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM



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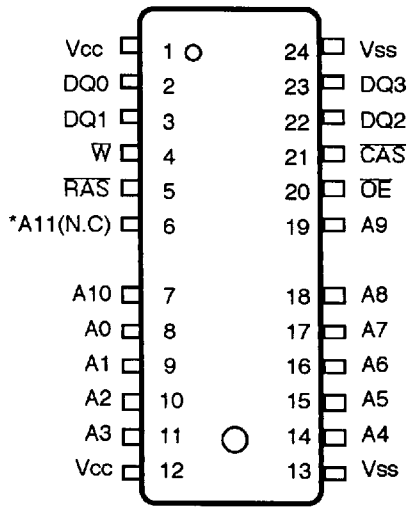
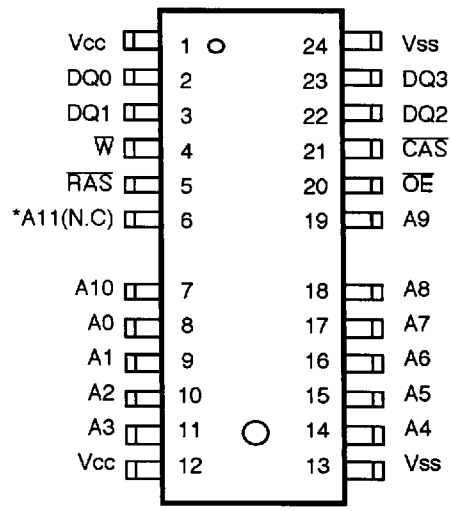
PIN CONFIGURATION (Top Views)

• **KM44C/V40(1)04BK**



• **KM44C/V40(1)04BS**



* A11 is N.C for KM44C/V4104B (5V/3.3V, 2K Ref. product)

K : 300mil 26(24) SOJ

S : 300mil 26(24) TSOP II

Pin Name	Pin Function
A0 ~ A11	Address Inputs (4K Product)
A0 ~ A10	Address Inputs (2K Product)
DQ0 ~ 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection (2K Ref. product)

ABSOLUTE MAXIMUM RATINGS *

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3 *1	2.4	-	Vcc+1 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	-1.0 *2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	μA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	μA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM44V4004B	KM44V4104B	KM44C4004B	KM44C4104B	
I_{CC1}	Don't care	-5	90	110	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	90	110	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
I_{CC4}	Don't care	-5	100	110	100	110	mA
		-6	90	100	90	100	mA
		-7	80	90	80	90	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.3	0.3	0.3	0.3	mA
I_{CC6}	Don't care	-5	90	110	90	110	mA
		-6	80	100	80	100	mA
		-7	70	90	70	90	mA
I_{CC7}	L	Don't care	450	400	450	400	μA
I_{CCS}	L	Don't care	250	250	300	300	μA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$= 0.2V
Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 62.5μs(2K/L-ver),
T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ3]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		ns	
Read-modify-write cycle time	tRWC	116		140		170		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		13		15		20	ns	3,4
Access time from column address	tAA		25		30		35	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	ns	5,13
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		15		20		ns	
$\overline{CAS}$ hold time	tCSH	38		45		50		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	37	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	7
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	8
Data hold time	tDH	8		10		15		ns	8
Refresh period(2K, Normal)	tREF		32		32		32	ms	
Refresh period(4K, Normal)	tREF		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	30		34		44		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40	ns	3
Hyper Page cycle time	tHPC	20		25		30		ns	14
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		ns	14
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		ns	
$\overline{OE}$ access time	tOEA		13		15		20	ns	
$\overline{OE}$ to data delay	tOED	13		15		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	ns	5
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		ns	10
Write command hold time (Test mode in)	tWTH	10		10		10		ns	10
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	5,13
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulth width (Hyper Page Cycle)	tWPE	5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		us	12

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : V_{CC}=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : V_{CC}=3.3V±0.3V, V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		ns	12

TEST MODE CYCLE

(Note. 10, 11)

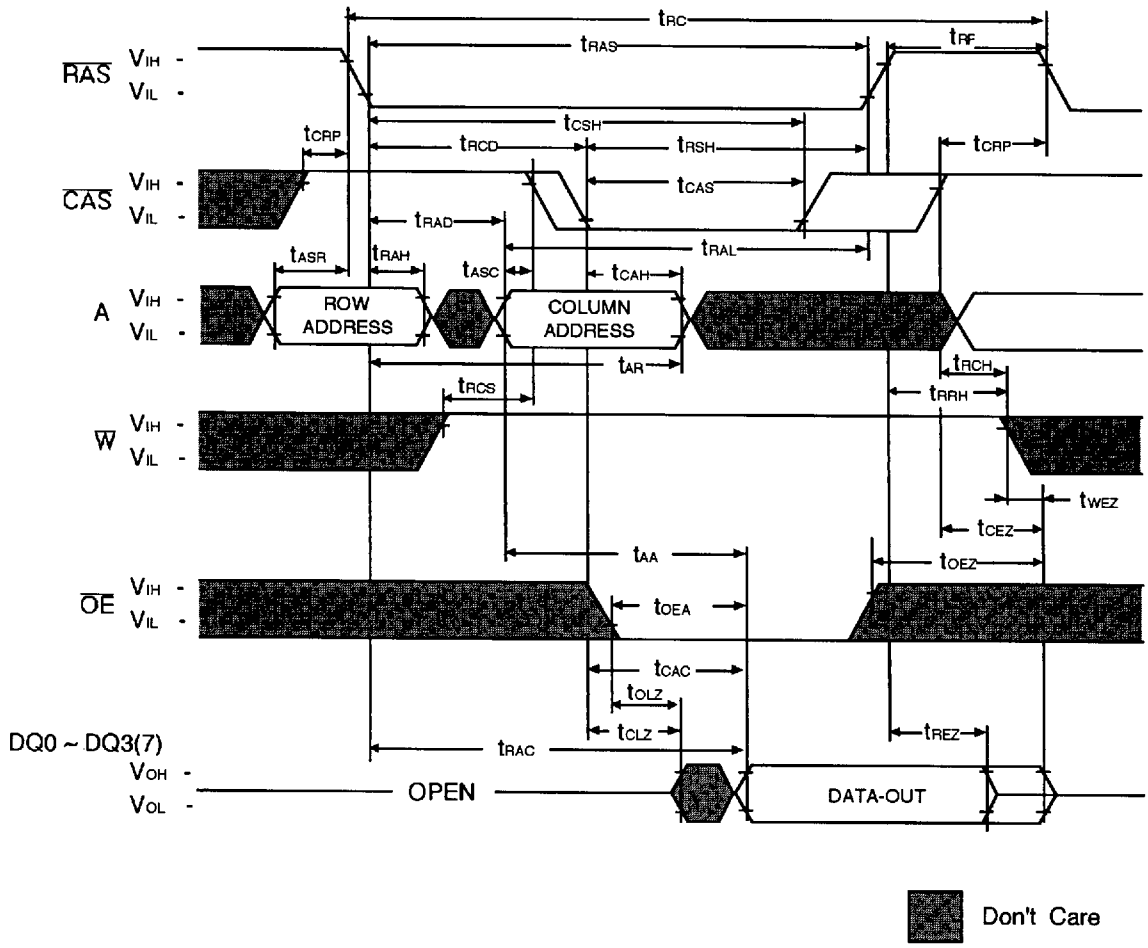
Parameter	Symbol	-5		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	89		109		129		ns	
Read-modify-write cycle time	tRWC	121		145		175		ns	
Access time from $\overline{RAS}$	tRAC		55		65		75	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4
Access time from column address	tAA		30		35		40	ns	3,9
$\overline{RAS}$ pulse width	tRAS	55	10K	65	10K	75	10K	ns	
$\overline{CAS}$ pulse width	tCAS	13	10K	15	10K	20	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	
$\overline{CAS}$ hold time	tCSH	43		50		55		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	35		39		49		ns	6
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	72		84		99		ns	6
Column address to $\overline{W}$ delay time	tAWD	47		54		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	52		59		69		ns	6
Hyper Page cycle time	tHPC	25		30		35		ns	14
Hyper page read-modify-write cycle time	tHPRWC	53		61		76		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	55	200K	65	200K	75	200K	ns	
Access time form $\overline{CAS}$ precharge	tCPA		33		40		45	ns	3
$\overline{OE}$ access time	tOEA		18		20		25	ns	
$\overline{OE}$ to data delay	tOED	18		20		25		ns	
$\overline{OE}$ command hold time	tOEH	18		20		25		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
10. These specifications are applied in the test mode.
11. In test mode read cycle, the values of tRAC, tAA and tCAC are delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding 5ns to the specified value in this data sheet.
12. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/2048(2K Ref.) cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. tASC ≥ 6ns, Assume tT = 2.0 ns

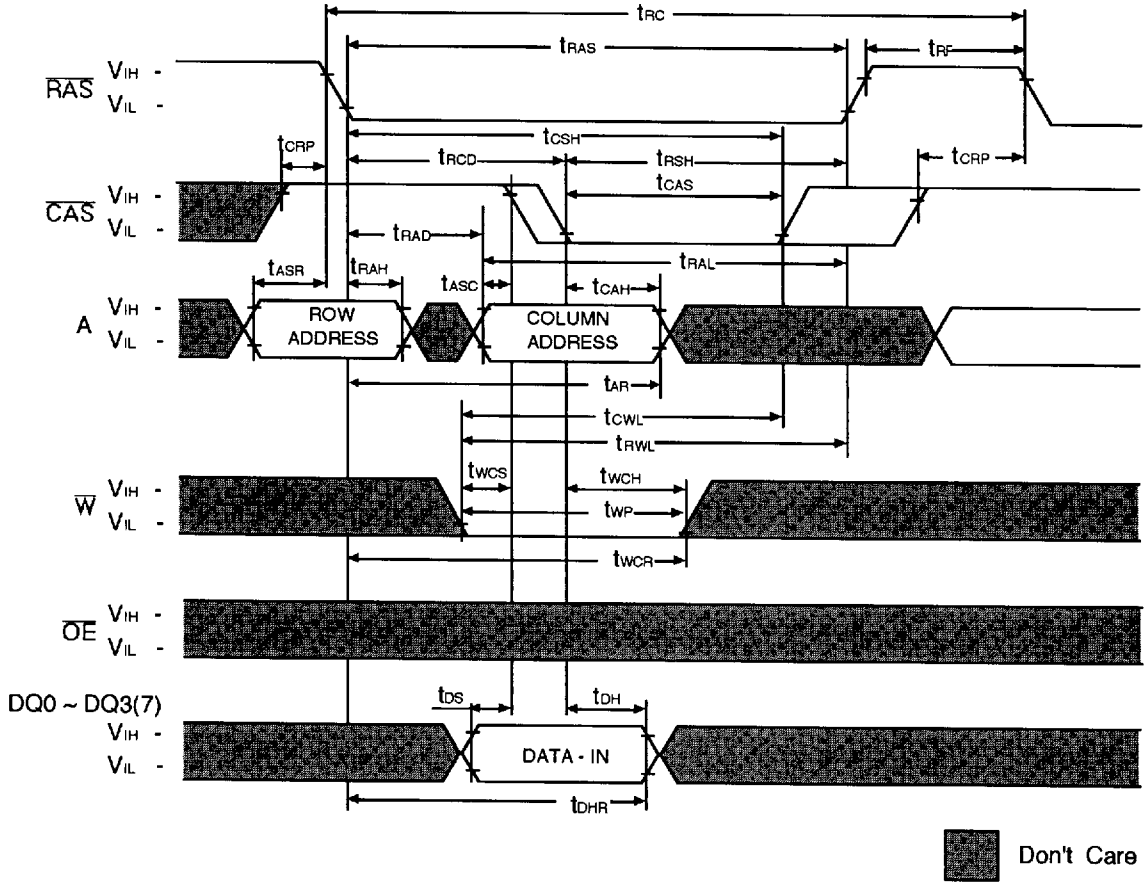
TIMING DIAGRAM

READ CYCLE



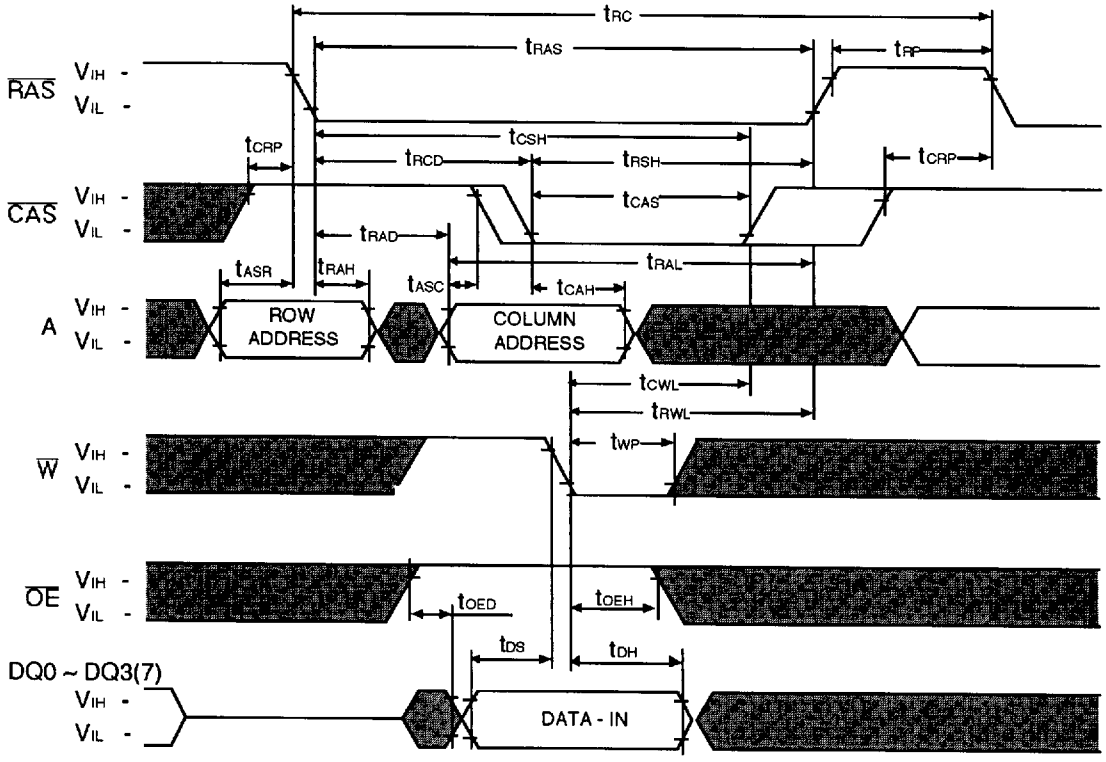
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



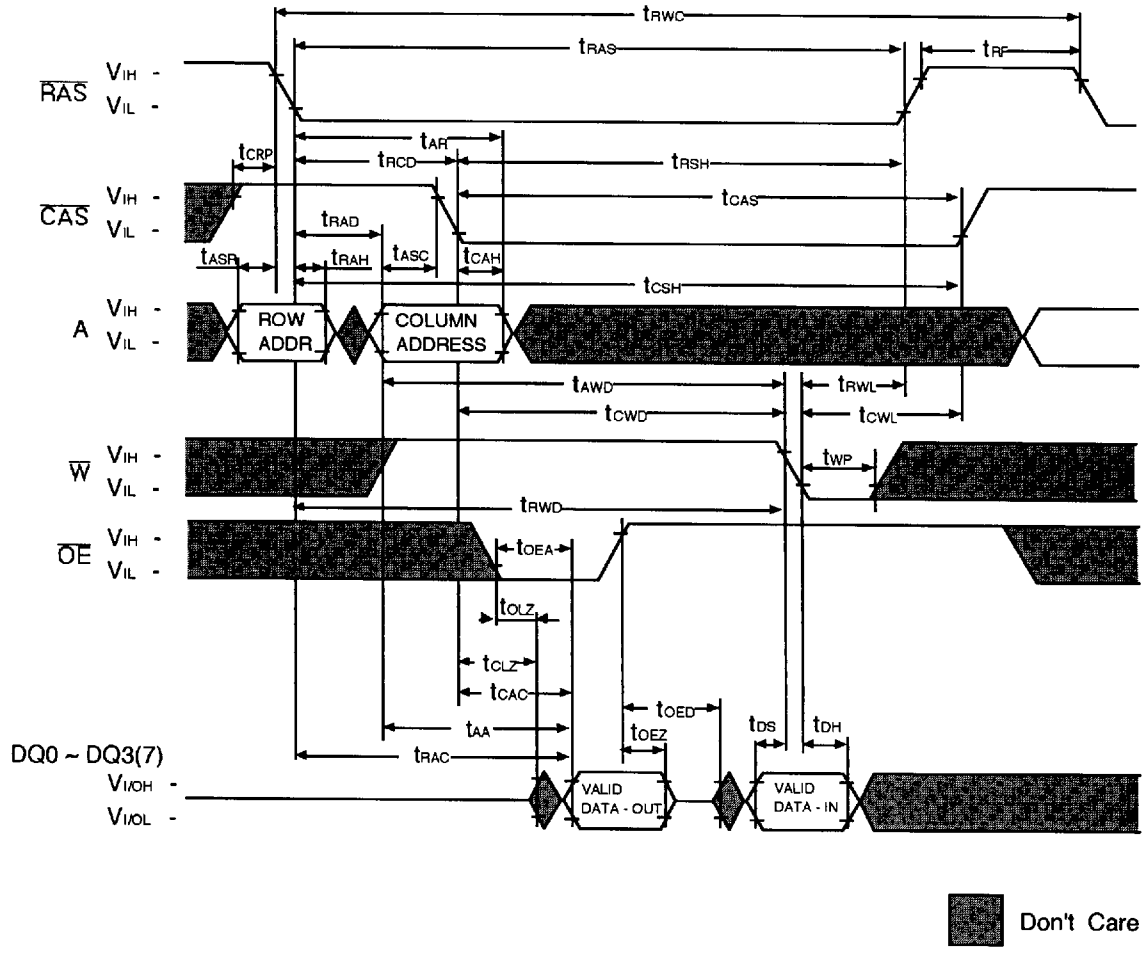
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

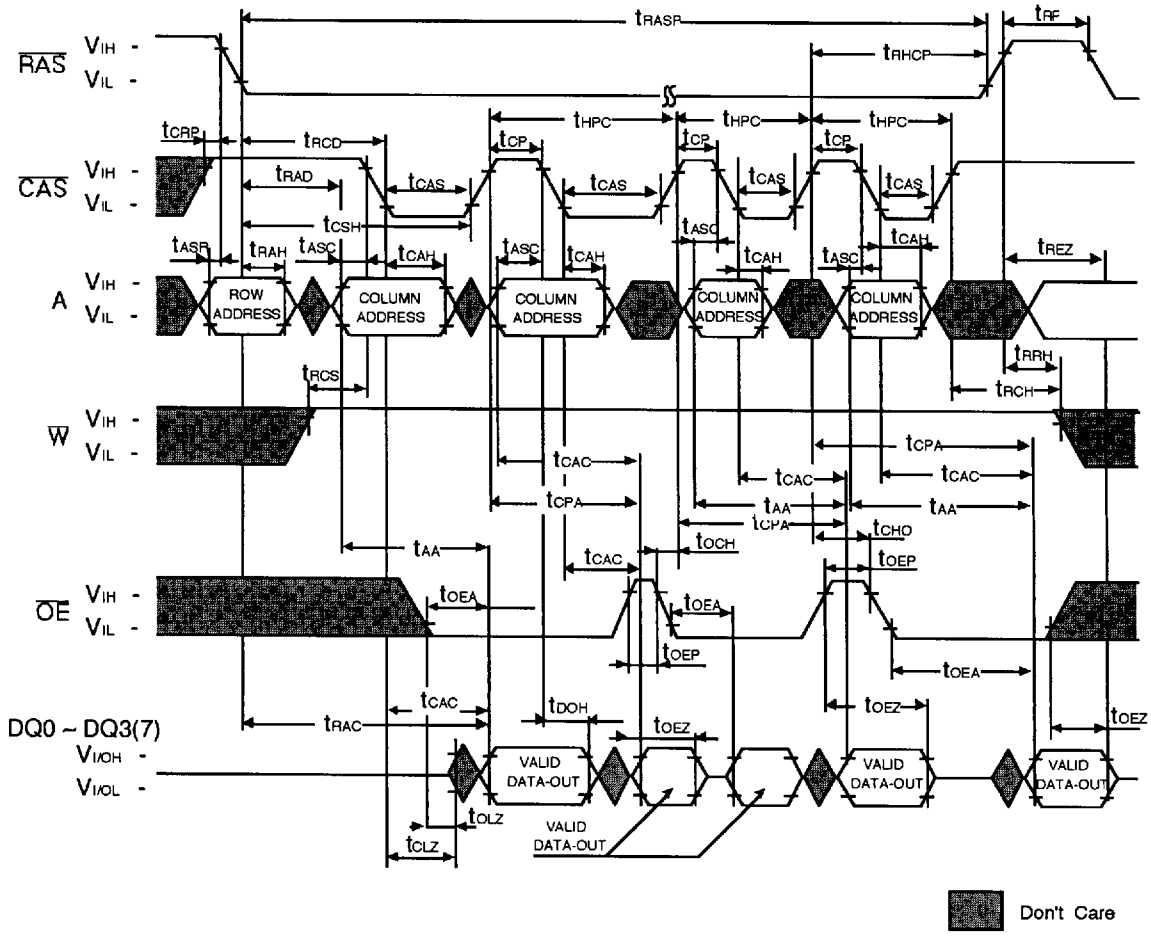


Don't Care

READ - MODIFY - WRITE CYCLE

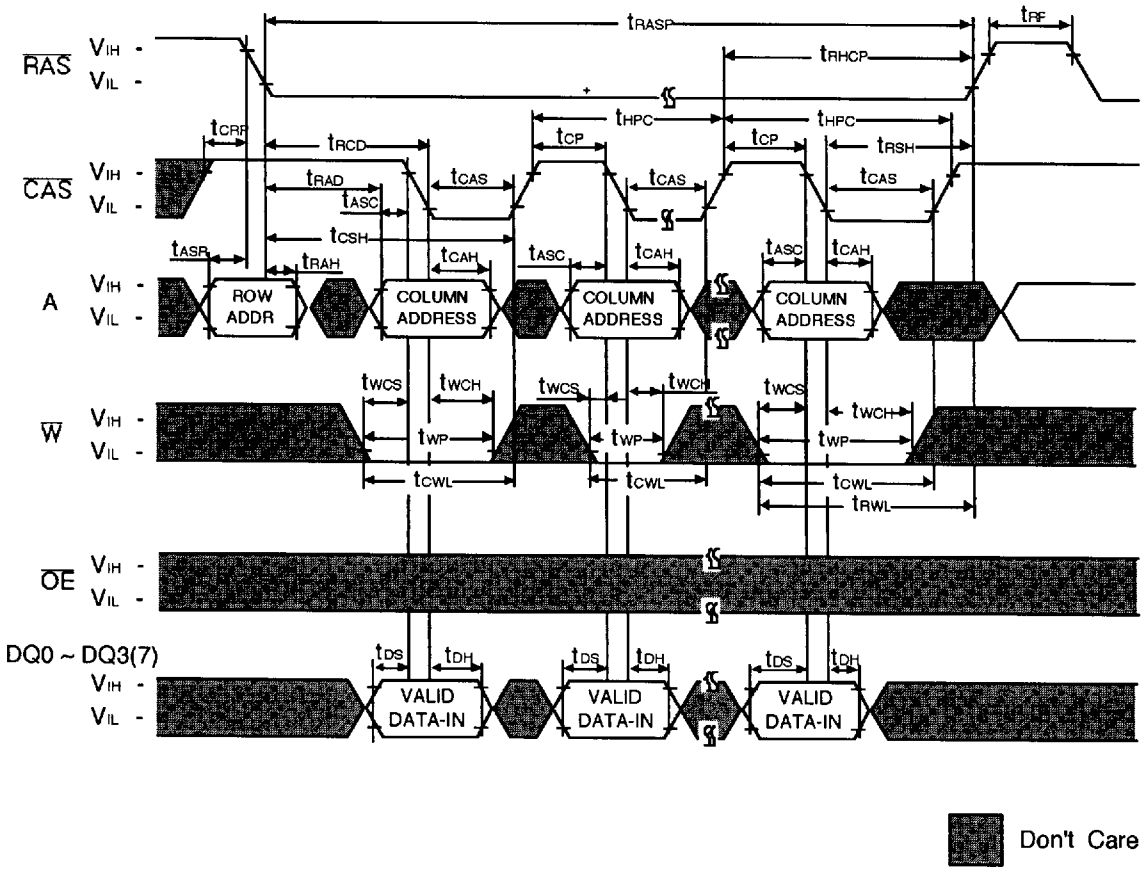


HYPER PAGE READ CYCLE

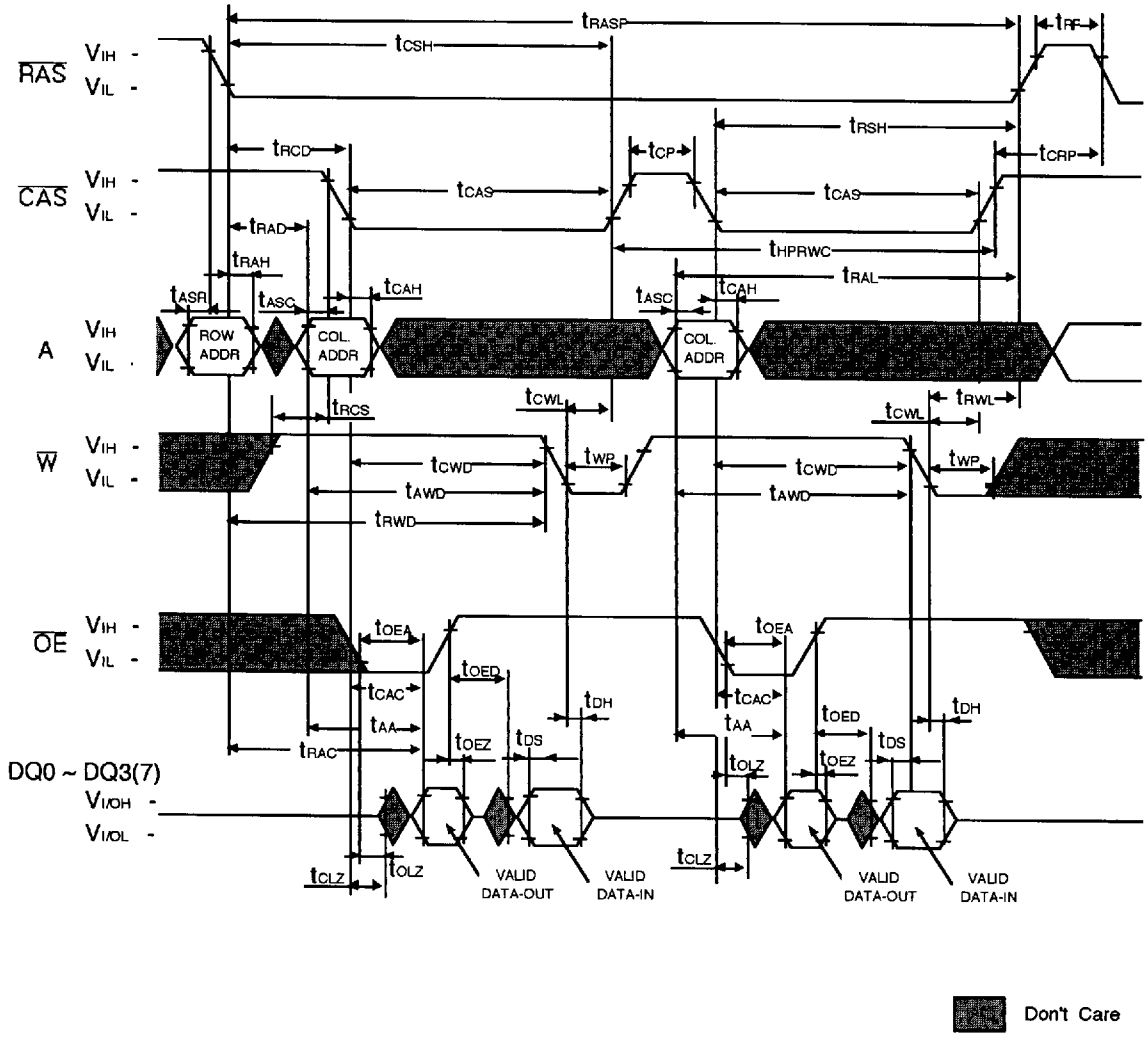


HYPER PAGE WRITE CYCLE (EARLY WRITE)

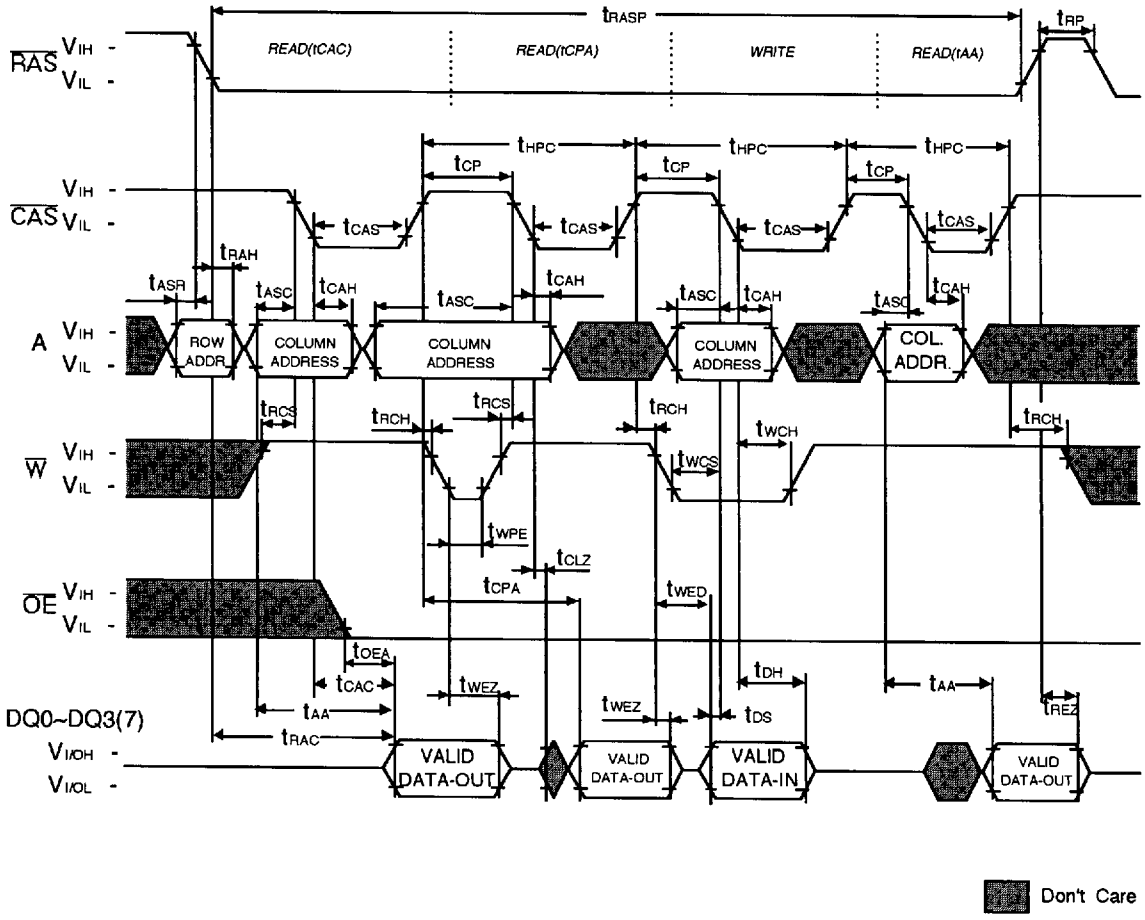
NOTE : D_{OUT} = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE

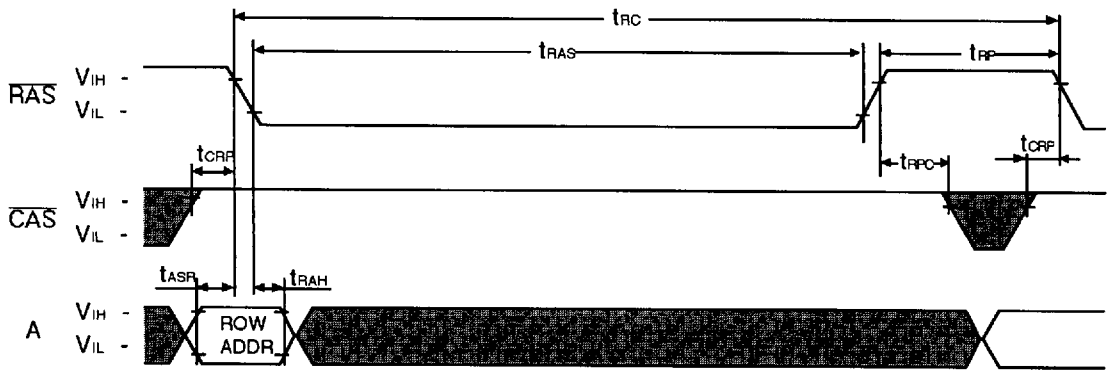


HYPER PAGE READ AND WRITE MIXED CYCLE



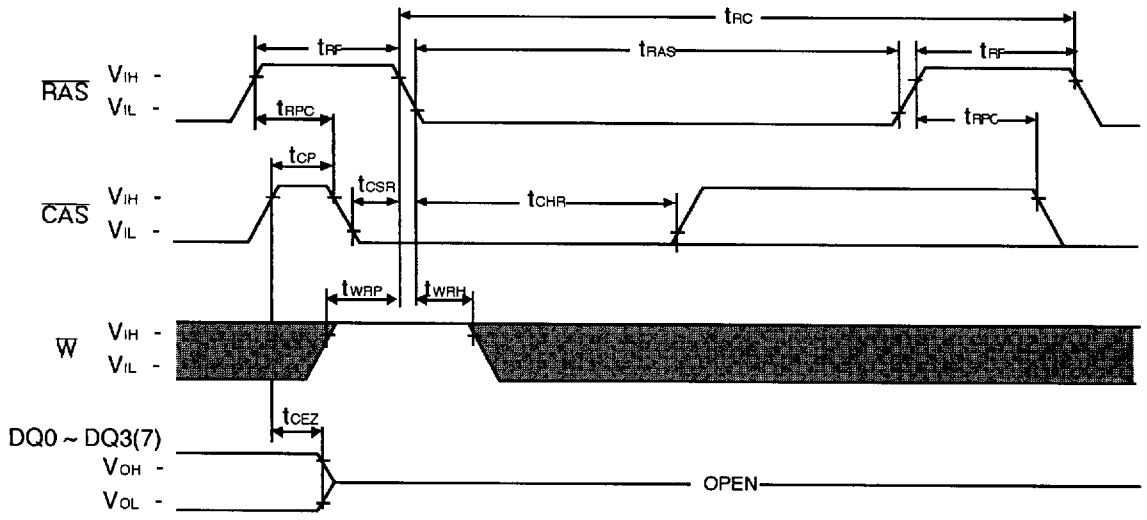
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

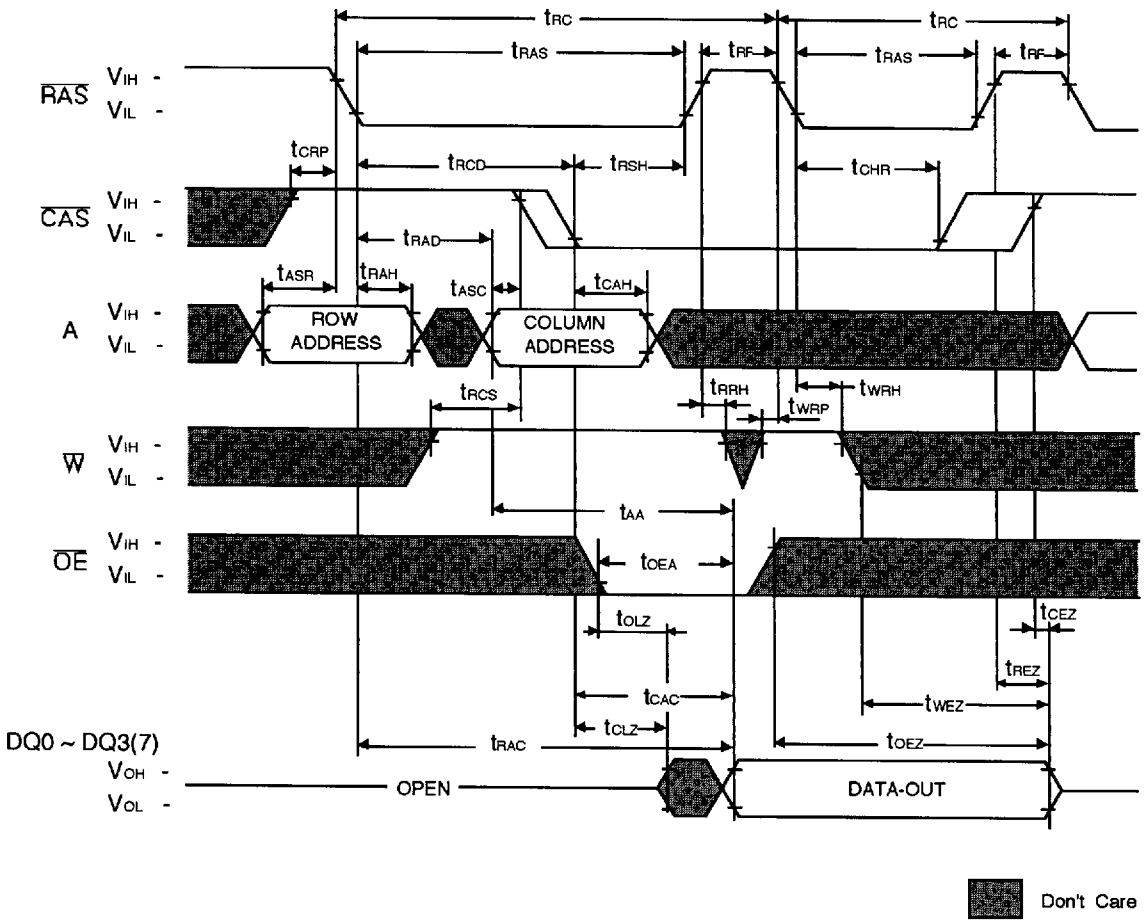


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care

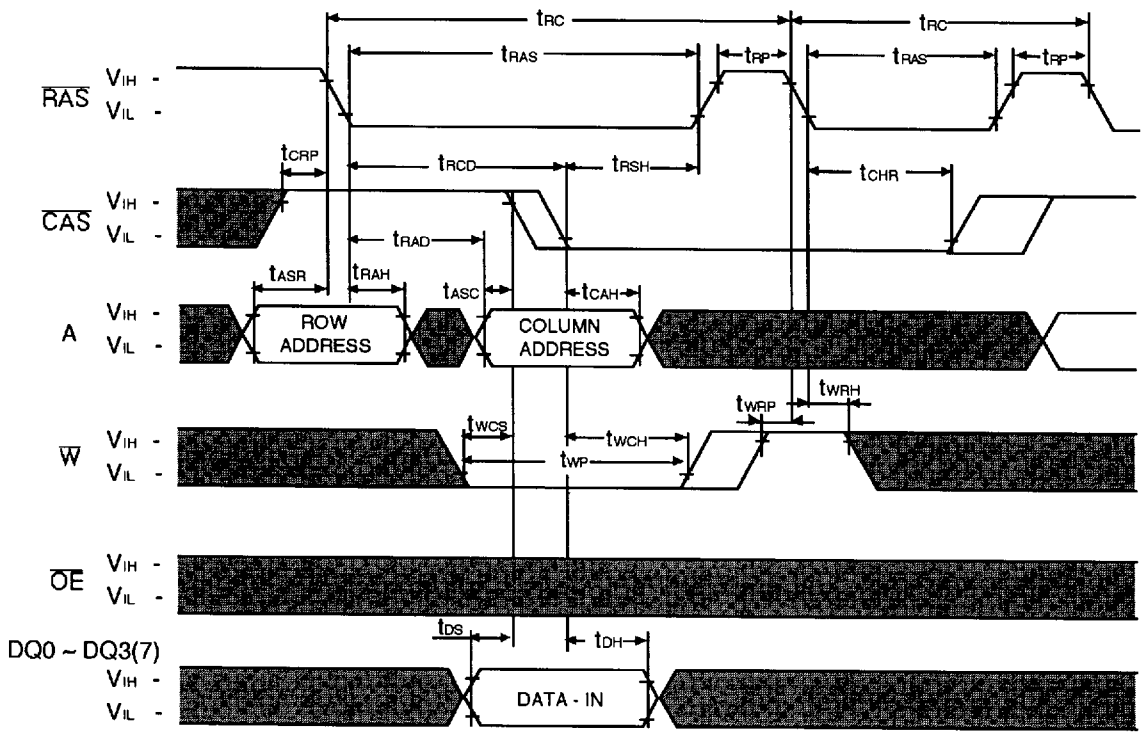


HIDDEN REFRESH CYCLE (READ)



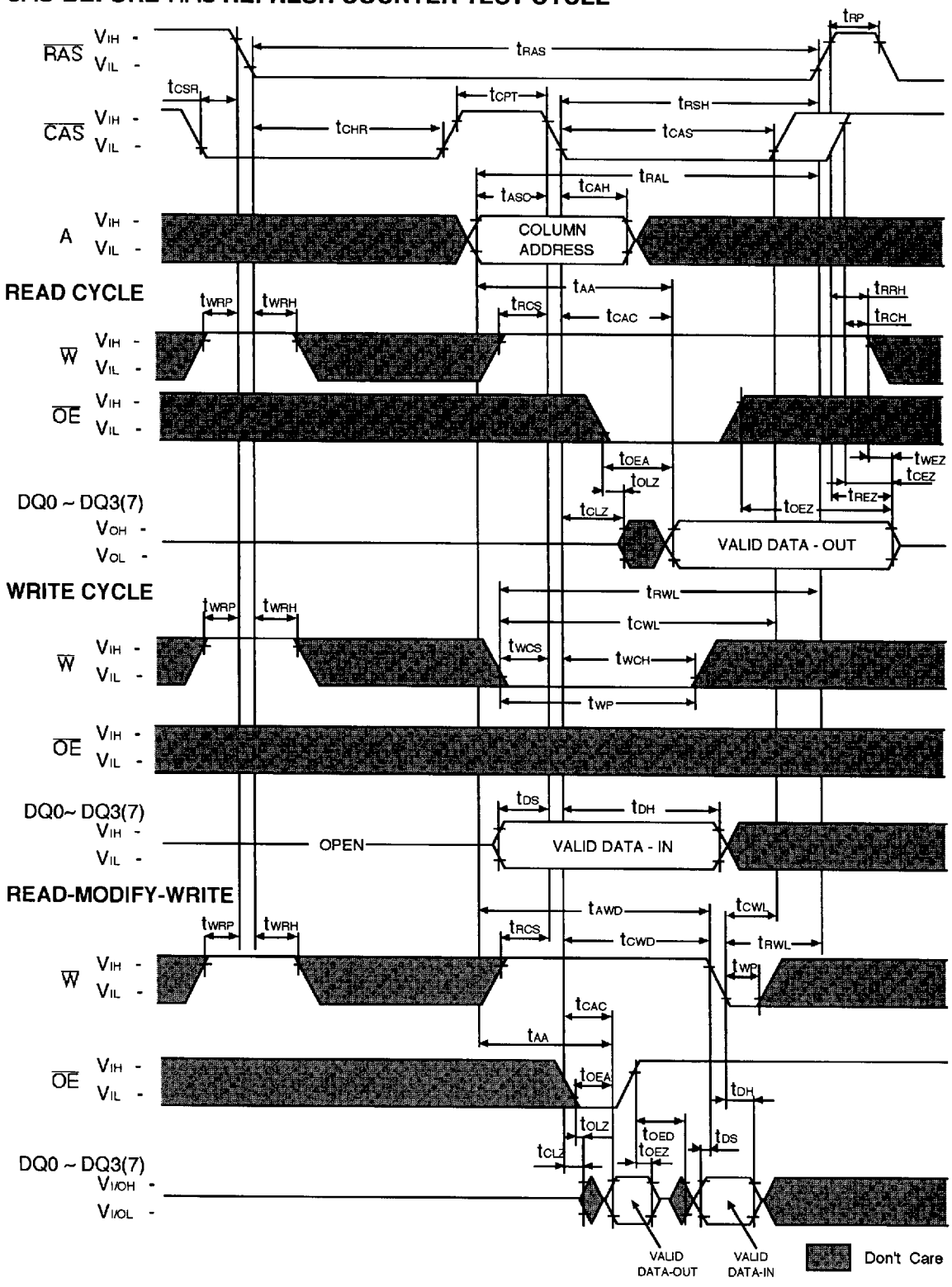
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



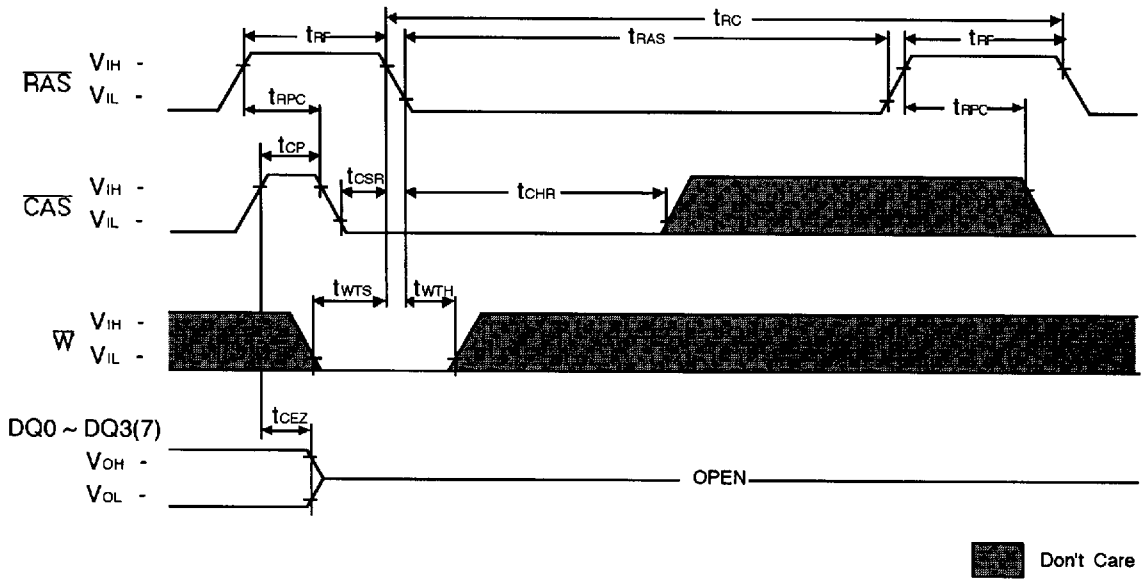
Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



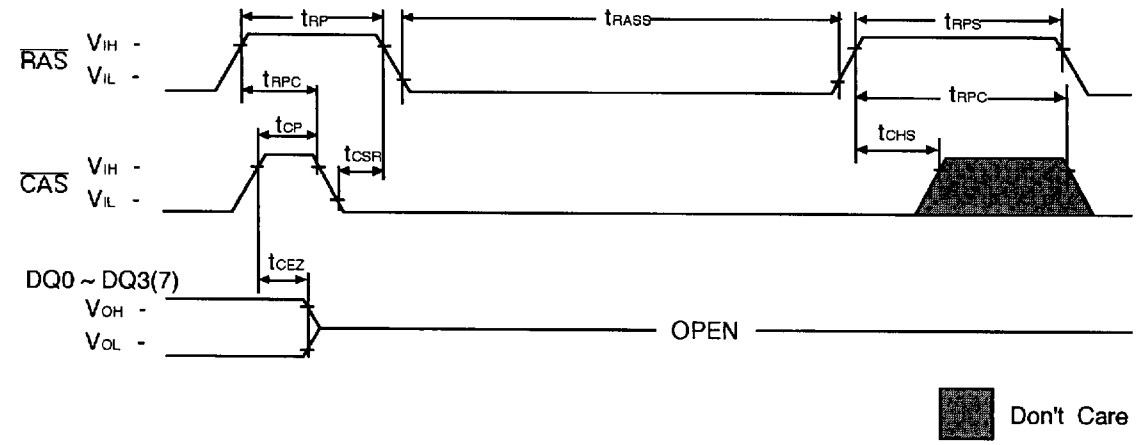
TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

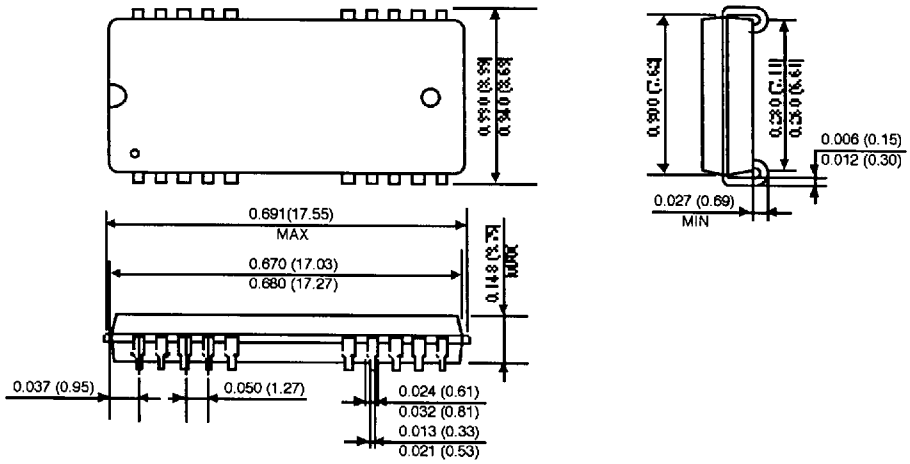
NOTE : $\overline{W}$=VIH (1Mx4, 4Mx4, 16Mx4, 2Mx8, 8Mx8)
Don't Care (512Kx8)
$\overline{OE}$, A = Don't Care



PLASTIC SMALL OUT-LINE J-LEAD

20(26) SOJ 300 mil

Unit : Inches (millimeters)



24(26) SOJ 300 mil

Unit : Inches (millimeters)