

32Kx8 Bit High Speed CMOS Static RAM

FEATURES

- Fast Access Time : 70, 85, 100ns (Max.)
- Low Power Dissipation
 - Standby (CMOS): 550μW (max.) L Version
 - 110μW (max.) LL Version
 - Operating : 385mW(max.)
- Single 5V±10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
 - No clock or refresh required
- Three state Output
- Low Data Retention Voltage : 2V (Min.)
- Standard Pin Configuration
 - KM62256BLS/BLS-L : 28-pin DIP-300
 - KM62256BLP/BLP-L : 28-pin DIP-600B
 - KM62256BLG/BLG-L : 28-pin SOP-450
 - KM62256BLTG/BLTG-L : 28-pin TSOP1-0813.4F
 - KM62256BLRG/BLRG-L : 28-pin TSOP1-0813.4R

GENERAL DESCRIPTION

The KM62256BL/BL-L is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits.

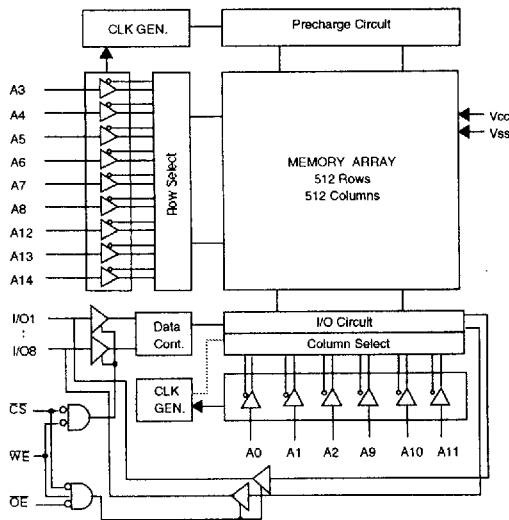
The device is fabricated using Samsung's advanced CMOS process with poly resistors.

The KM62256BL/BL-L has an output enable input for precise control of the data outputs.

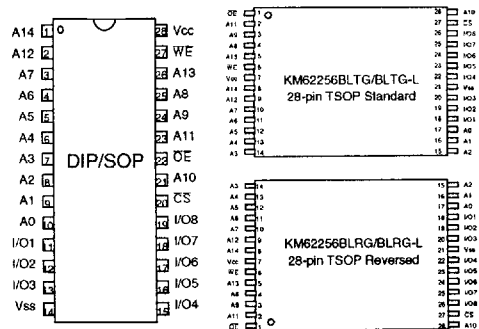
It also has a chip enable input for the minimum current power down mode.

The KM62256BL/BL-L has been designed for high speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A14	Address Inputs
WE	Write Enable Input
CS	Chip Select Input
OE	Output Enable Input
I/O1-I/O8	Data Inputs/Outputs
Vcc	Power(5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN,OUT}	-0.5 to V _{CC} +0.5	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{stg}	-65 to 150	°C
Operating Temperature	T _A	0 to 70	°C
Soldering Temperature and Time	T _{solder}	260°C, 10sec(Lead Only)	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL}	-0.5 *	-	0.8	V

* V_{IL}(Min.)= -3.0V for ≤50 ns Pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70 °C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition	Min.	Typ*	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-	-	±1	μA
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{I/O} =V _{SS} to V _{CC}	-	-	±1	μA
Operating Power Supply Current	I _{CC}	$\overline{CS}=V_{IL}$, V _{IN} = or V _{IH} or V _{IL} , I _{I/O} =0mA	-	7	15	mA
Average Operating Current	I _{CC 1}	Cycle Time=1μs, 100% Duty $\overline{CS} \leq 0.2V$, V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V, I _{I/O} =0mA	-	-	7	mA
		Min Cycle, 100% Duty $\overline{CS}=V_{IL}$, I _{I/O} =0mA	-	45	70	mA
Standby Power Supply Current	I _{SB}	$\overline{CS}=V_{IH}$	-	-	1	mA
	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$ V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	L	-	2	100
L-L			-	1	20	μA
Output Low Voltage	V _{OL}	I _{ol} =2.1 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{oh} =-1.0 mA	2.4	-	-	V

* Typ; V_{CC}=5V, T_A=25°C

CAPACITANCE * (f=1MHz, TA=25 °C)

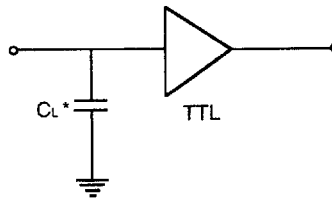
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output Capacitance	C _{IO}	V _{IO} =0V	-	8	pF

* Note: Capacitance is sampled and not 100% tested.

TEST CONDITIONS

(TA=0 to 70 °C, VCC=5V±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L =100pF+1TTL



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	trc	70	-	85	-	100	-	ns
Address Access Time	tAA	-	70	-	85	-	100	ns
Chip Select to Output	tCO	-	70	-	85	-	100	ns
Output Enable to Valid Output	tOE	-	35	-	45	-	50	ns
Chip Select to Low-Z Output	tLZ	10	-	10	-	10	-	ns
Output Enable to Low-Z Output	tOLZ	5	-	5	-	5	-	ns
Chip Disable to High-Z Output	tHZ	0	30	0	30	0	35	ns
Output Disable to High-Z Output	tOHZ	0	30	0	30	0	35	ns
Output Hold from Address Change	tOH	5	-	5	-	10	-	ns

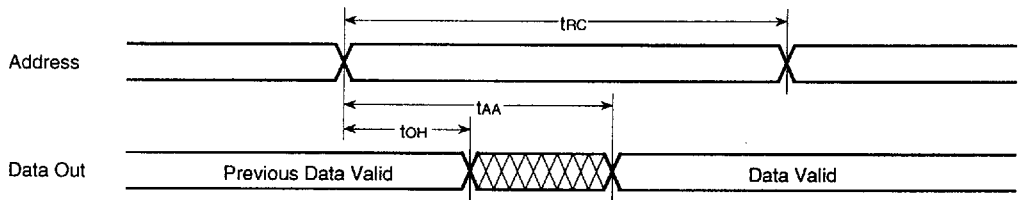
WRITE CYCLE

Parameter	Symbol	KM62256BL-7 KM62256BL-7L		KM62256BL-8 KM62256BL-8L		KM62256BL-10 KM62256BL-10L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{wc}	70	-	80	-	100	-	ns
Chip Select to End of Write	t _{cw}	60	-	75	-	80	-	ns
Address Set-up Time	t _{as}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{aw}	60	-	75	-	80	-	ns
Write Pulse Width	t _{wp}	50	-	60	-	60	-	ns
Write Recovery Time	t _{wr}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{whz}	0	25	0	30	0	30	ns
Data to Write Time Overlap	t _{dw}	30	-	40	-	40	-	ns
Data Hold from Write Time	t _{dh}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{ow}	5	-	5	-	5	-	ns

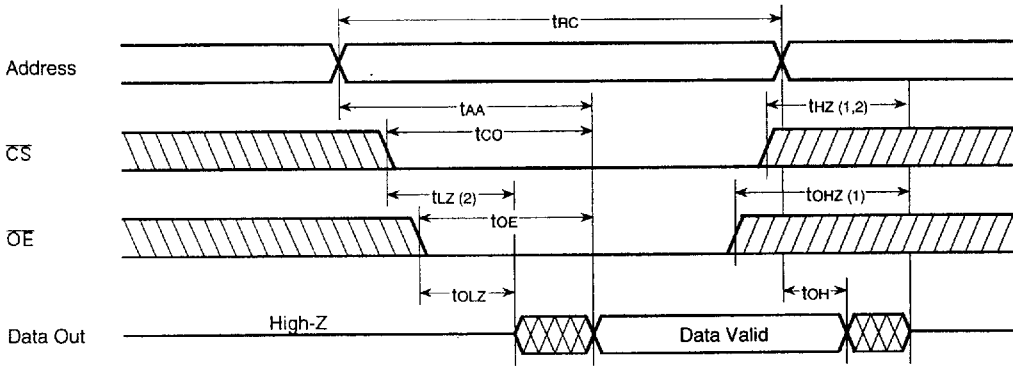
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=V_{IL}, WE=V_{IH})



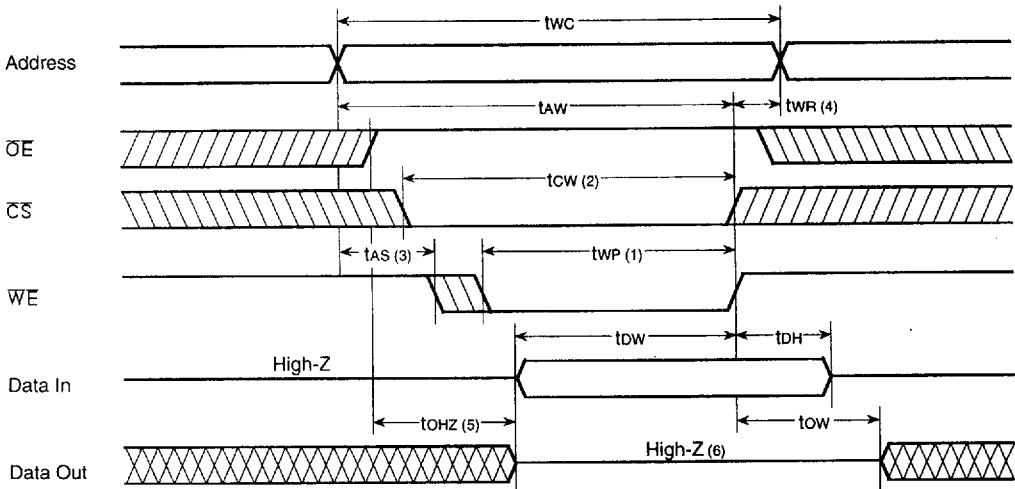
TIMING WAVEFORM OF READ CYCLE(2) (WE=V_{IH})



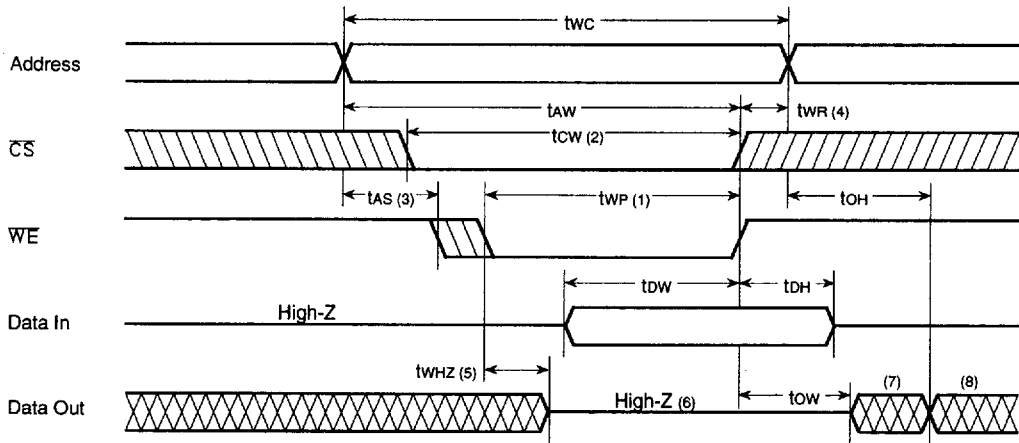
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition tHZ(max) is less than tLZ(min) both for a given device and from device to device.
3. WE is high for read cycle.
4. Address valid prior to or coincident with CS transition Low.

TIMING WAVEFORM OF WRITE CYCLE(1) (OE Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} Fixed)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low \overline{CS} and low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low : A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{cW} is measured from the later of \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. If $\overline{OE}, \overline{WE}$ are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If \overline{CS} goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain high impedance state.
7. Dout is the same phase of the latest written data in this write cycle
8. Dout is the read data of new address

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	Vcc Current
H	X	X	Power down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	DOUT	I_{CC}
L	L	X	Write	DIN	I_{CC}

Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS ($T_a=0$ to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Vcc for Data Retention	Vdr	$\overline{CS} \geq V_{cc}-0.2V$	2.0		5.5	V
Data Retention Current	I _{dr}	V _{cc} =3.0V	L	1	50*	μA
		$\overline{CS} \geq V_{cc}-0.2V$	L-L	0.5	10**	μA
Data Retention Set-up Time	t _{SDR}	See Data Retention Waveforms (below)	0			ns
Recovery Time	t _{RDR}	See Data Retention Waveforms (below)	5			ms

* 20 μA (Max.) at 0°C - 40°C

** 3 μA (Max.) at 0°C - 40°C

2

DATA RETENTION WAVEFORM 1 (\overline{CS} Controlled)

