

Document Title

**128Kx8 High Speed Static RAM(5V Operating), Evolutionary Pin Out.
Operated at Commercial Temperature Range.**

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>																											
Rev. 0.0	Initial release with Design Target.	Jan. 18th, 1995	Design Target																											
Rev. 1.0	Release to Preliminary Data Sheet. 1.1. Replace Design Target to Preliminary	Apr. 22th, 1995	Preliminary																											
Rev. 2.0	Release to final Data Sheet. 2.1. Delete Preliminary	Feb. 29th, 1996	Final																											
Rev. 3.0	Update D.C and A.C parameters. 3.1. Update D.C parameters <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Items</th> <th>Previous spec. (15/17/20ns part)</th> <th>Updated spec. (15/17/20ns part)</th> </tr> </thead> <tbody> <tr> <td>lcc</td> <td>190/180/170mA</td> <td>165/165/160mA</td> </tr> <tr> <td>lsb</td> <td>30mA</td> <td>25mA</td> </tr> <tr> <td>lsb1</td> <td>10mA</td> <td>8mA</td> </tr> </tbody> </table> 3.2. Update A.C parameters <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Items</th> <th>Previous spec. (15/17/20ns part)</th> <th>Updated spec. (15/17/20ns part)</th> </tr> </thead> <tbody> <tr> <td>tcw</td> <td>12/12/13ns</td> <td>10/11/12ns</td> </tr> <tr> <td>tAW</td> <td>12/12/13ns</td> <td>10/11/12ns</td> </tr> <tr> <td>tWP1(OE=H)</td> <td>12/12/13ns</td> <td>10/11/12ns</td> </tr> <tr> <td>tdw</td> <td>8/9/10ns</td> <td>7/8/9ns</td> </tr> </tbody> </table>	Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)	lcc	190/180/170mA	165/165/160mA	lsb	30mA	25mA	lsb1	10mA	8mA	Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)	tcw	12/12/13ns	10/11/12ns	tAW	12/12/13ns	10/11/12ns	tWP1(OE=H)	12/12/13ns	10/11/12ns	tdw	8/9/10ns	7/8/9ns	Jul. 16th, 1996	Final
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Rev. 4.0	Update D.C and A.C parameters and add 300mil-SOJ PKG. 4. 1. Add 32-Pin 300mil-SOJ Package. 4. 2. Update D.C and A.C parameters. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Items</th> <th>Previous spec. (15/17/20ns part)</th> <th>Updated spec. (15/17/20ns part)</th> </tr> </thead> <tbody> <tr> <td>lcc</td> <td>165/165/160mA</td> <td>125/125/120mA</td> </tr> <tr> <td>tow</td> <td>3/4/5ns</td> <td>3/3/3ns</td> </tr> </tbody> </table> 4.3. Add the test condition for Voh1 with Vcc=5V±5% at 25°C 4.4. Add timing diagram to define tWP1 as "(Timing Wave Form of Write Cycle(OE=Low Fixed))"	Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)	lcc	165/165/160mA	125/125/120mA	tow	3/4/5ns	3/3/3ns	Jun. 2nd, 1997	Final																		
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Rev. 5.0	5.1. Delete 17ns Part 5.2. Delete 32-SOJ-300 Package	Feb. 25th, 1998	Final																											

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

128K x 8 Bit High-Speed CMOS Static RAM

FEATURES

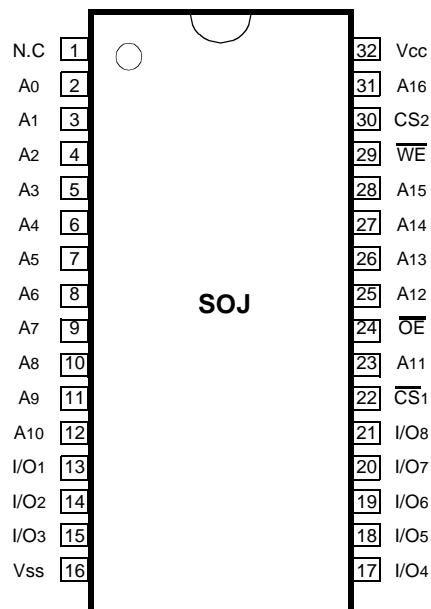
- Fast Access Time 15, 20ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 25mA(Max.)
 - (CMOS) : 8mA(Max.)
- Operating KM681001A - 15 : 125mA(Max.)
- KM681001A - 20 : 120mA(Max.)
- Single 5.0V ±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Standard Pin Configuration
 - KM681001AJ : 32-SOJ-400

GENERAL DESCRIPTION

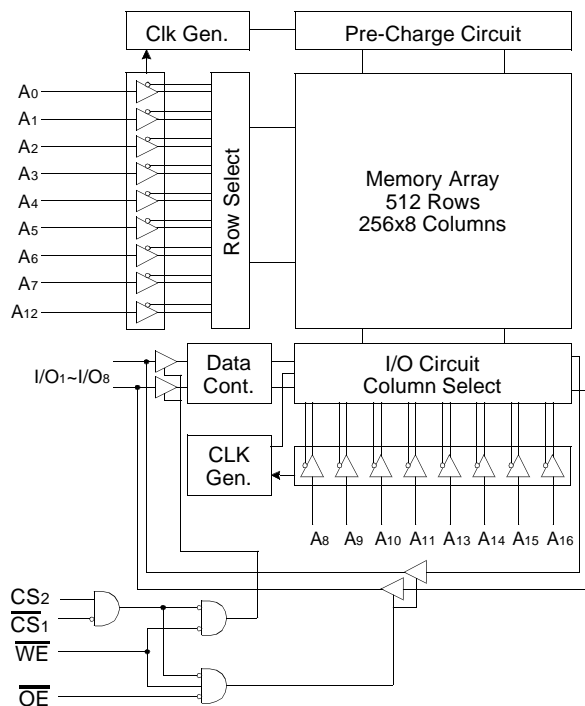
The KM681001A is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The KM681001A uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM681001A is packaged in a 400mil 32-pin plastic SOJ.

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PIN CONFIGURATION (Top View)



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

Pin Name	Pin Function
A0 - A16	Address Inputs
\overline{WE}	Write Enable
$\overline{CS1}$, CS2	Chip Selects
\overline{OE}	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS(T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} + 0.5**	V
Input Low Voltage	V _{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c.(Pulse Width≤10ns) for I_S≤20mA

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤10ns) for I_S≤20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	-2	2	μA	
Output Leakage Current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}	-2	2	μA	
Operating Current	I _{CC}	Min. Cycle, 100% Duty $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	15ns	-	125	mA
			20ns	-	120	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$	-	25	mA	
	I _{SB1}	f=0MHz, $\overline{CS}_1\geq V_{CC}-0.2V$ or $CS_2\leq 0.2V$, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	-	8	mA	
Output Low Voltage Level	V _{OL}	I _{OL} =8mA	-	0.4	V	
Output High Voltage Level	V _{OH}	I _{OH} =-4mA	2.4	-	V	
	V _{OH1} *	I _{OH1} =-0.1mA	-	3.95	V	

* V_{CC}=5.0V, Temp.=25°C

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* NOTE : Capacitance is sampled and not 100% tested.

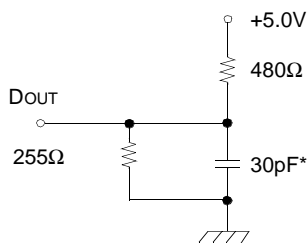
AC CHARACTERISTICS (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

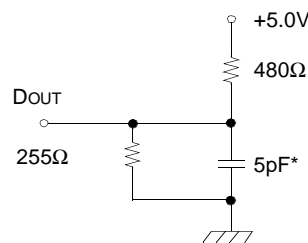
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Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-20		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	20	-	ns
Address Access Time	tAA	-	15	-	20	ns
Chip Select to Output	tCO*	-	15	-	20	ns
Output Enable to Valid Output	tOE	-	8	-	10	ns
Chip Enable to Low-Z Output	tLZ*	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ*	0	6	0	8	ns
Output Disable to High-Z Output	tOHZ	0	6	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	ns
Chip Selection to Power Down Time	tPD	-	15	-	20	ns

NOTE: tCO=tCO1, tCO2/ tLZ=tLZ1, tLZ2/ tHZ=tHZ1, tHZ2

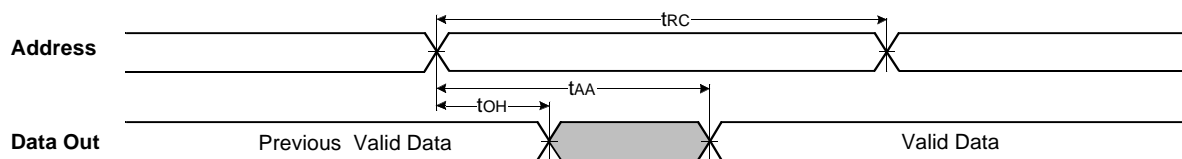
WRITE CYCLE

Parameter	Symbol	KM681001A-15		KM681001A-20		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	20	-	ns
Chip Select to End of Write	tcw	10	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	10	-	12	-	ns
Write Pulse Width(\overline{OE} High)	tWP	10	-	12	-	ns
Write Pulse Width(\overline{OE} Low)	tWP1	15	-	20	-	ns
Write Recovery Time	tWR*	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	ns
Data to Write Time Overlap	tdW	7	-	9	-	ns
Data Hold from Write Time	tdH	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	ns

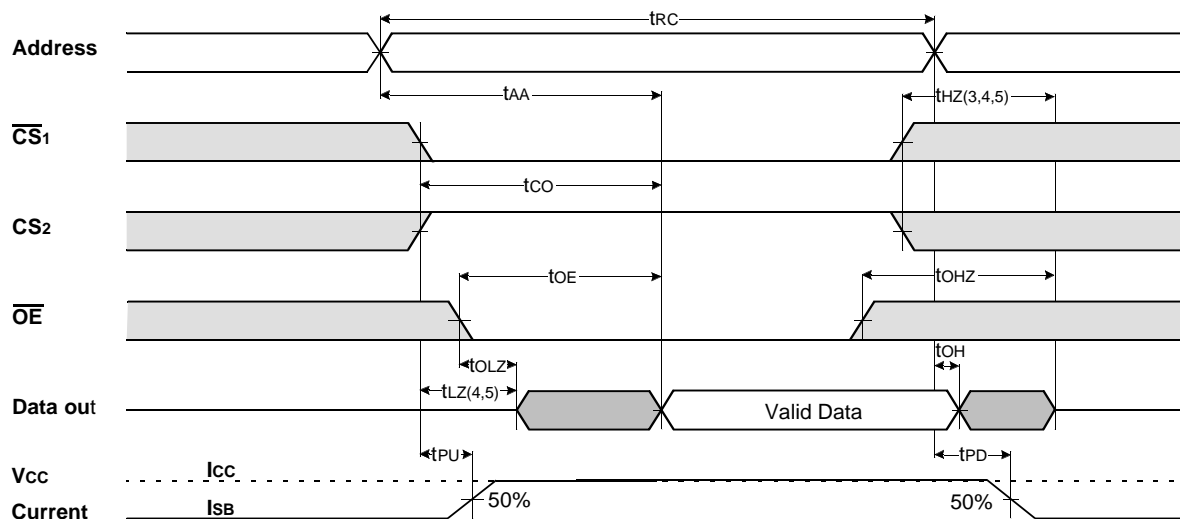
NOTE: tWR=tWR1, tWR2

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_1=\overline{OE}=V_{IL}$, $\overline{CS}_2=\overline{WE}=V_{IH}$)



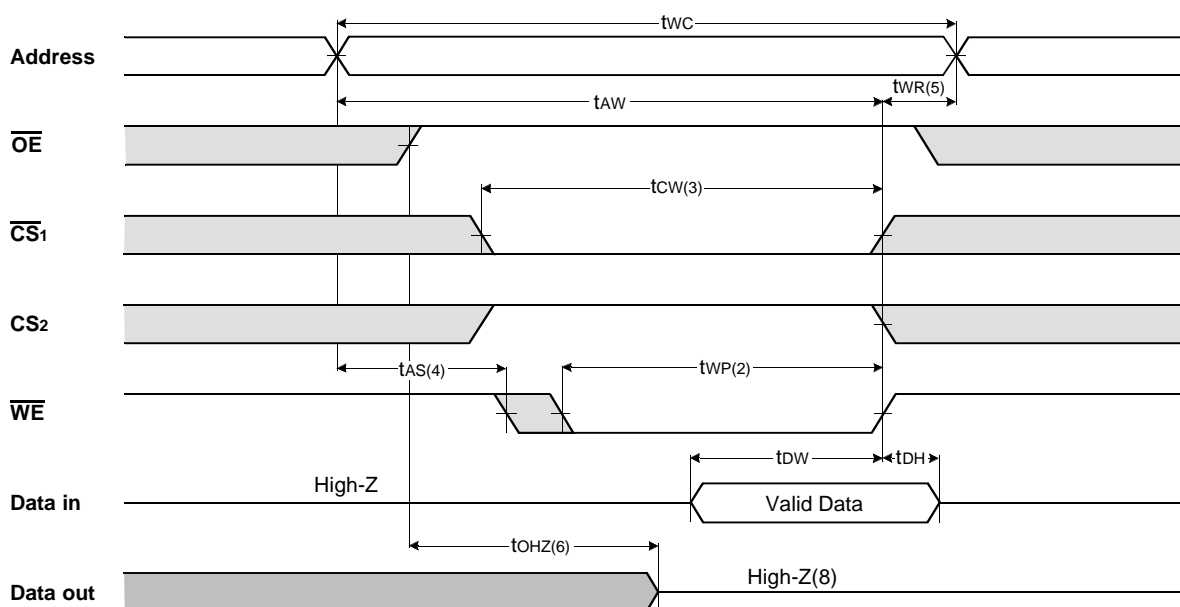
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



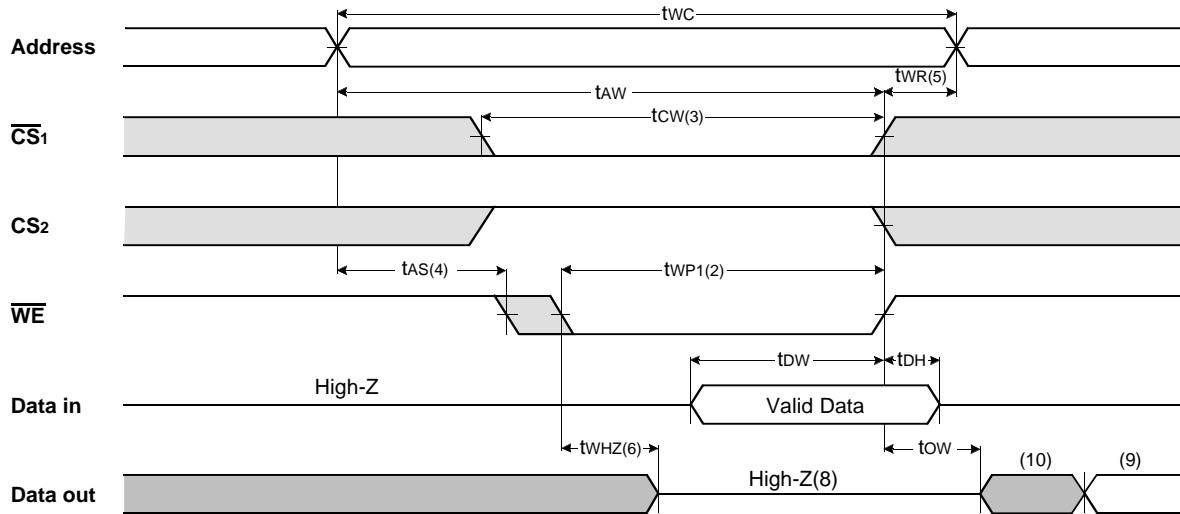
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{hz} and t_{ohz} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{hz}(Max.) is less than t_{lz}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}_1=V_{IL}$ and $CS_2=V_{IH}$.
7. Address valid prior to coincident with \overline{CS}_1 transition low and CS_2 transition high.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

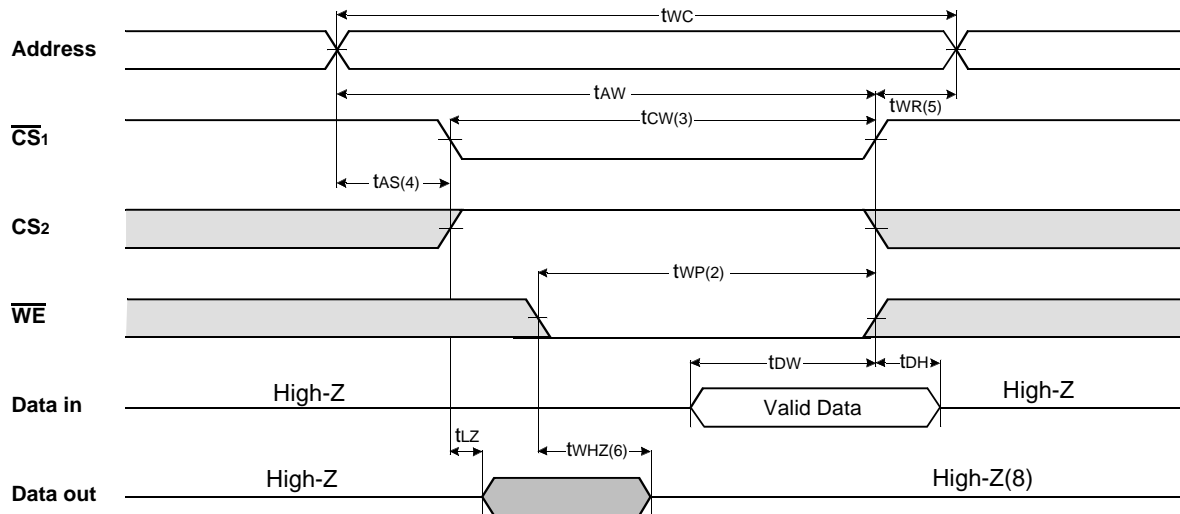
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE} = \text{Clock}$)



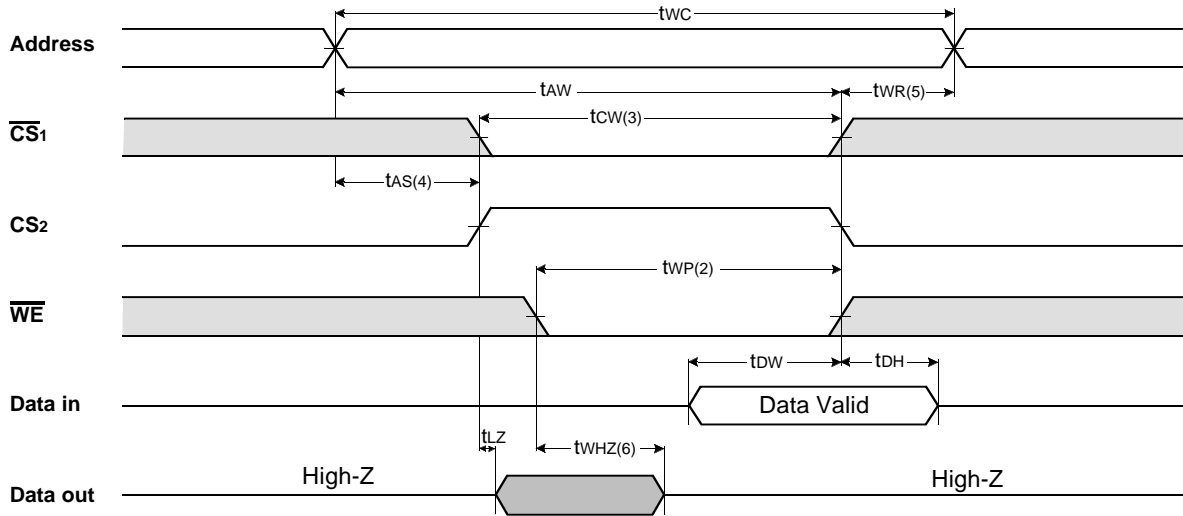
TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS1}$ = Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) (CS₂ = Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS₁, a high CS₂ and a low WE. A write begins at the latest transition CS₁ going low, a CS₂ going high and WE going low ; A write ends at the earliest transition CS₁ going high, CS₂ going low or WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of CS₁ going low or CS₂ going high to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as CS₁ or WE going high. t_{WR2} applied in case a write ends as CS₂ going low.
6. If OE, CS₁, CS₂ and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS₁ goes low and CS₂ goes high simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS₁ is low and CS₂ is high : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

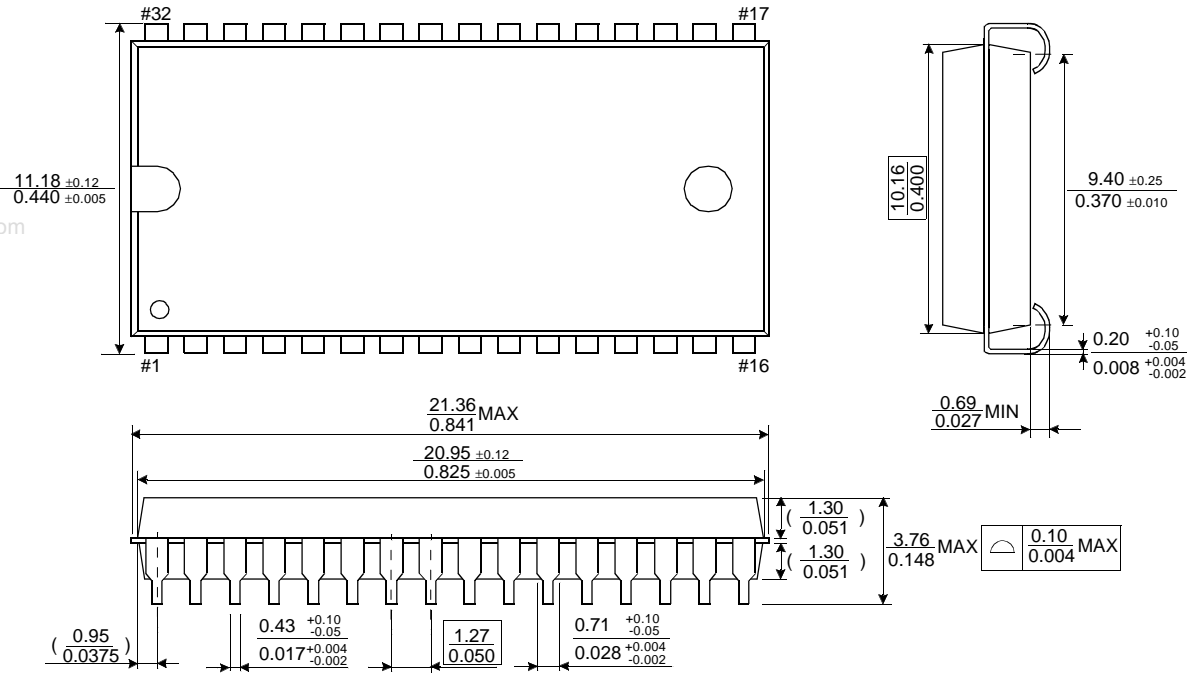
CS ₁	CS ₂	WE	OE	Mode	I/O Pin	Supply Current
H	X	X	X*	Not Select	High-Z	ISB, ISB1
X	L	X	X	Not Select	High-Z	ISB, ISB1
L	H	H	H	Output Disable	High-Z	I _{CC}
L	H	H	L	Read	DOUT	I _{CC}
L	H	L	X	Write	DIN	I _{CC}

* NOTE : X means Don't Care.

PACKAGE DIMENSIONS

32-SOJ-400

Units: millimeters/Inches



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