

Document Title

1Mx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft - Dual CS	June 22, 1999	Advance

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KM688100 Family

1Mx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 1M x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

GENERAL DESCRIPTION

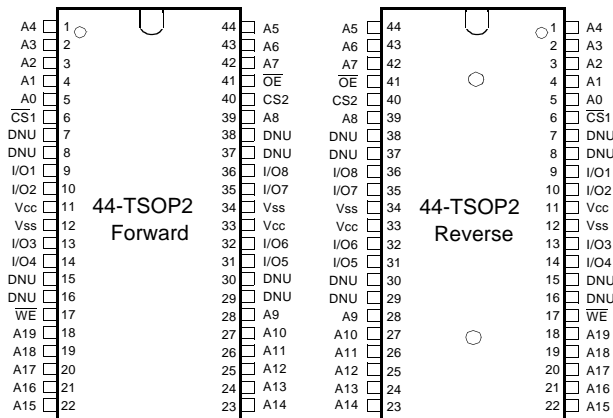
The KM688100 families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
KM688100L-L	Commercial(0~70°C)	4.5~5.5V	55 ¹⁾ /70ns	50μA	70mA	44-TSOP2-400F/R
KM688100LI-L	Industrial(-40~85°C)			80μA		

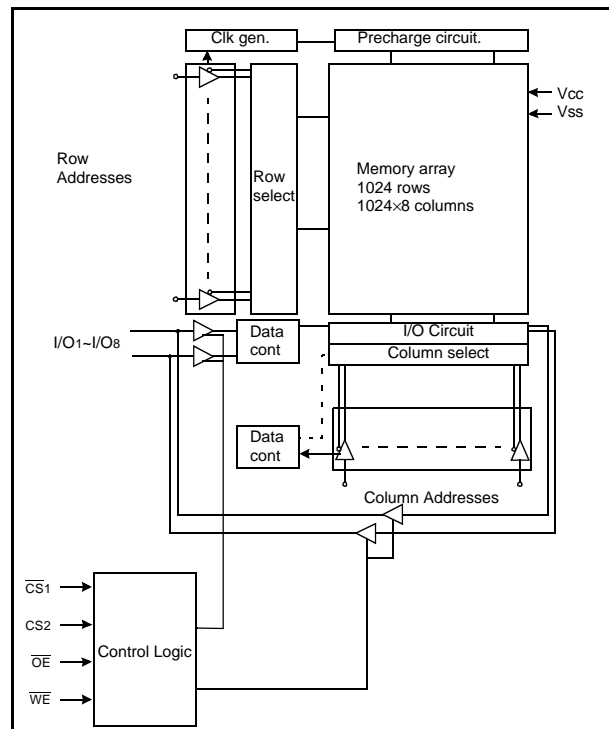
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS1}, \overline{CS2}$	Chip Select Inputs	Vcc	Power
\overline{OE}	Output Enable Input	Vss	Ground
\overline{WE}	Write Enable Input	A0~A19	Address Inputs
I/O1~I/O8	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM688100LT-7L KM688100LT-10L	44-TSOP2-F, 70ns, 5.0V, LL 44-TSOP2-F, 100ns, 5.0V, LL	KM688100LTI-7L KM688100LTI-10L	44-TSOP2-F, 70ns, 5.0V, LL 44-TSOP2-F, 100ns, 5.0V, LL
KM688100LR-7L KM688100LR-10L	44-TSOP2-R, 70ns, 5.0V, LL 44-TSOP2-R, 100ns, 5.0V, LL	KM688100LRI-7L KM688100LRI-10L	44-TSOP2-R, 70ns, 5.0V, LL 44-TSOP2-R, 100ns, 5.0V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O ₁₋₈	Mode	Power
H	X	X	X	High-Z	Deselected	Standby
X	L	X	X	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X	L	Din	Write	Active

Note : X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM688100L
		-40 to 85	°C	KM688100LI

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM688100 Family	4.5	5.0	5.5	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM688100 Family	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	KM688100 Family	-0.5 ³⁾	-	0.8	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specified.
Industrial Product : T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns.
3. Undershoot: -3.0V in case of pulse width ≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

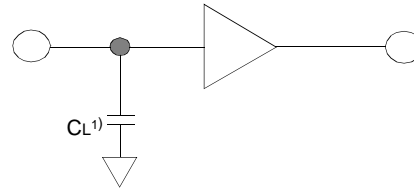
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , $\overline{WE}=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	-	12	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	10	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	70	mA	
Output low voltage	V _{OL}	I _{OL} = 2.1mA			0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4			V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	KM688100L-L	-	-	50	μA
			KM688100LI-L	-	-	80	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load(see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=4.5\sim 5.5\text{V}$, Commercial product: $T_A=0$ to 70°C , Industrial product: $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ1} , t _{LZ1}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Output hold from address change	t _{OH}	5	-	10	-	ns
	Chip disable to high-Z output	t _{HZ1} , t _{HZ1}	0	20	0	25	ns
	$\overline{\text{OE}}$ disable to high-Z output	t _{OHZ}	0	20	0	25	ns
Write	Write cycle time	t _{WC}	10	-	70	-	ns
	Chip select to end of write	t _{CW1} , t _{CW2}	-	25	60	-	ns
	Address set-up time	t _{AS}	0	20	0	-	ns
	Address valid to end of write	t _{AW}	55	-	60	-	ns
	Write pulse width	t _{WP}	45	-	55	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	45	-	0	25	ns
	Data to write time overlap	t _{DW}	45	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
End write to output low-Z	t _{OW}	0	20	5	-	ns	

DATA RETENTION CHARACTERISTICS

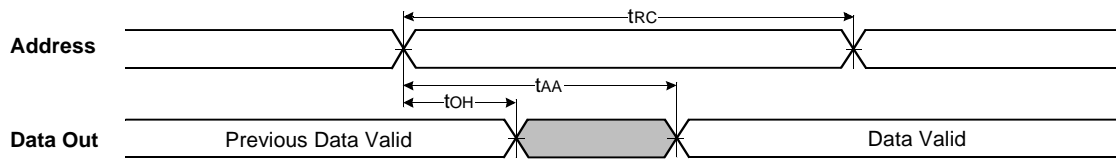
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	2.0	-	5.5	V
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}$, $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	-	-	20 ⁽²⁾	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

1. $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}$, $\text{CS}_2 \geq V_{CC}-0.2\text{V}$ (CS_1 controlled) or $\text{CS}_2 \geq V_{CC}-0.2\text{V}$ (CS_2 controlled).

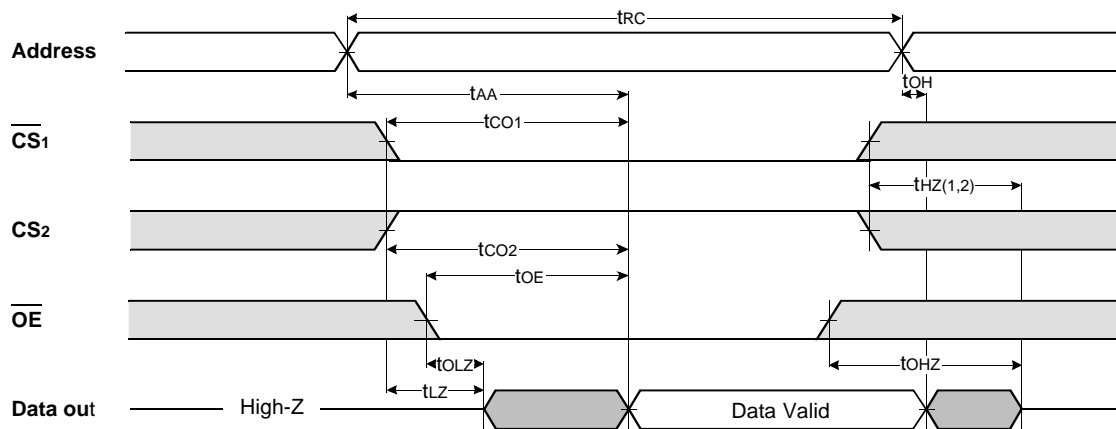
2. Industrial product=30 μA

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $CS_2 = \overline{WE} = V_{IH}$)



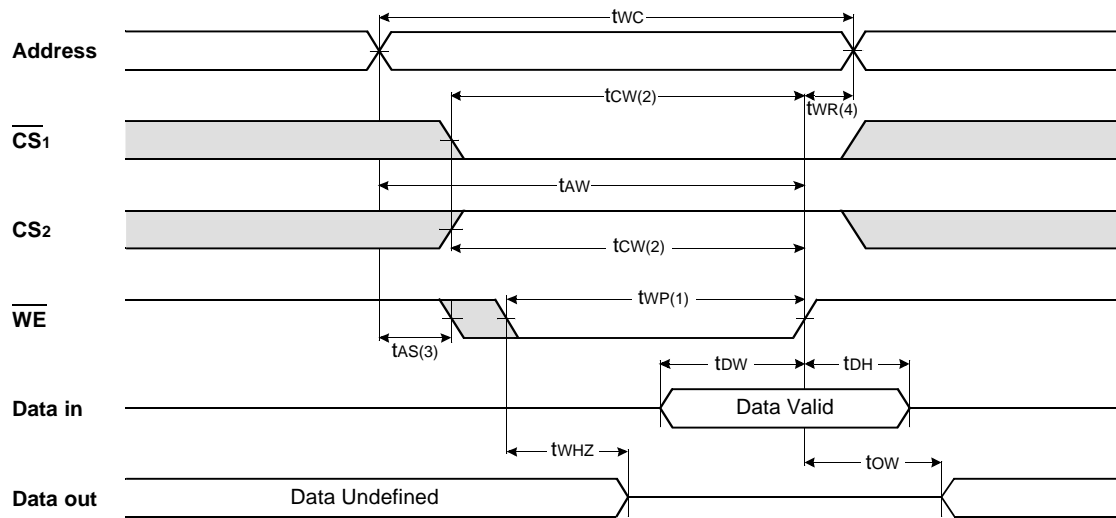
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE} = V_{IH}$)



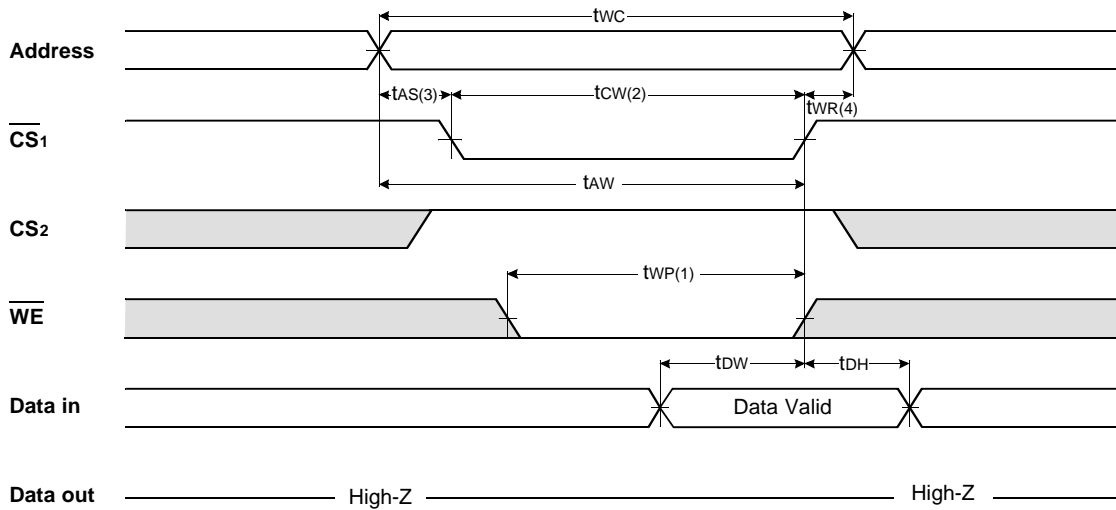
NOTES (READ CYCLE)

1. t_{HZ} and t_{OH} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

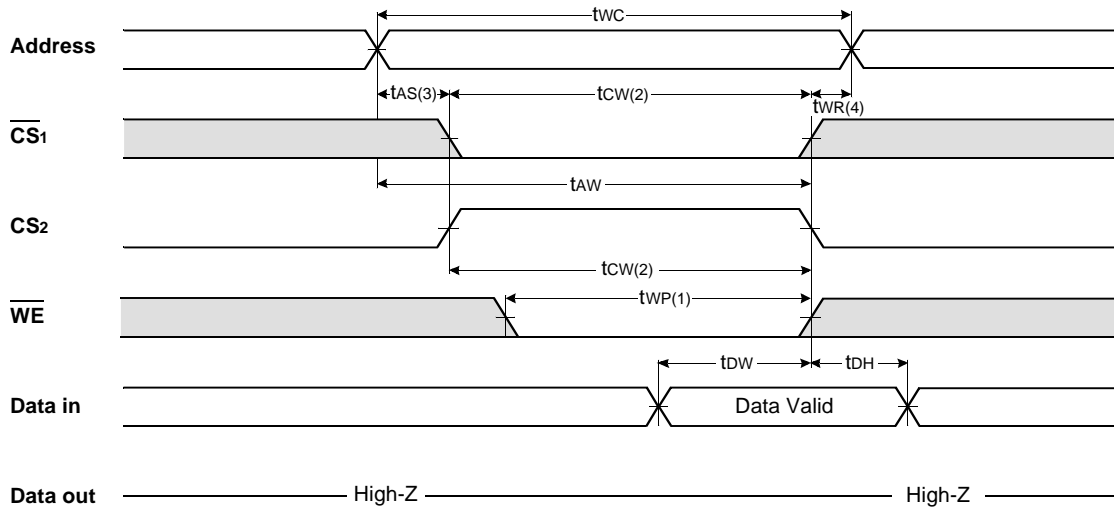
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

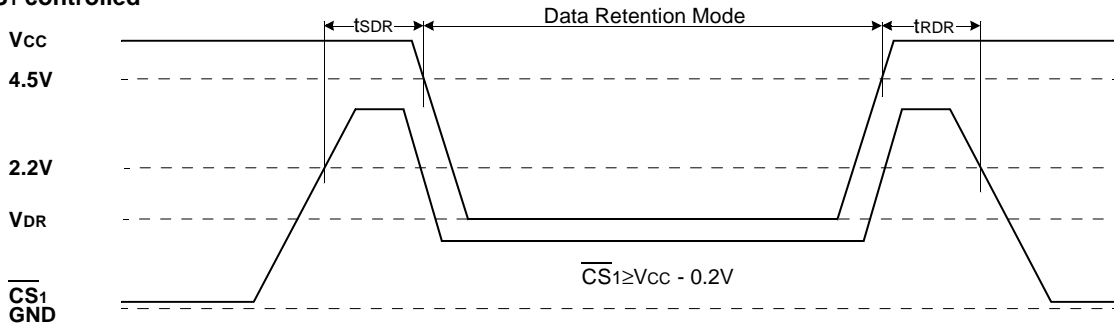


NOTES (WRITE CYCLE)

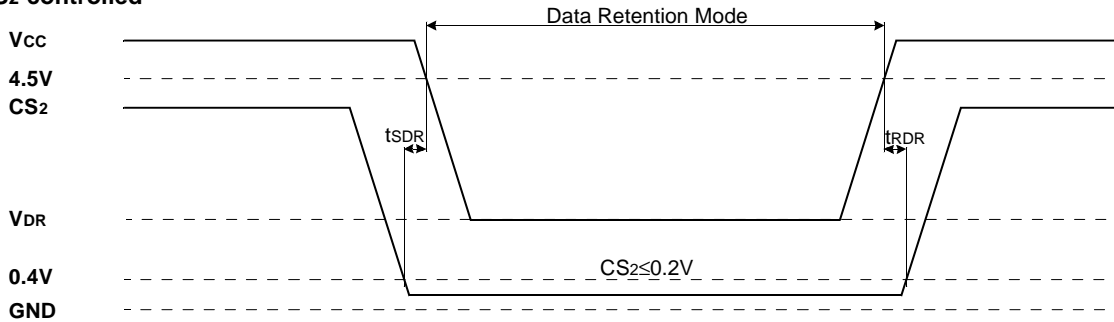
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low : A write ends at the earliest transition among \overline{CS}_1 going high, CS_2 going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as \overline{CS}_1 or \overline{WE} going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

\overline{CS}_1 controlled



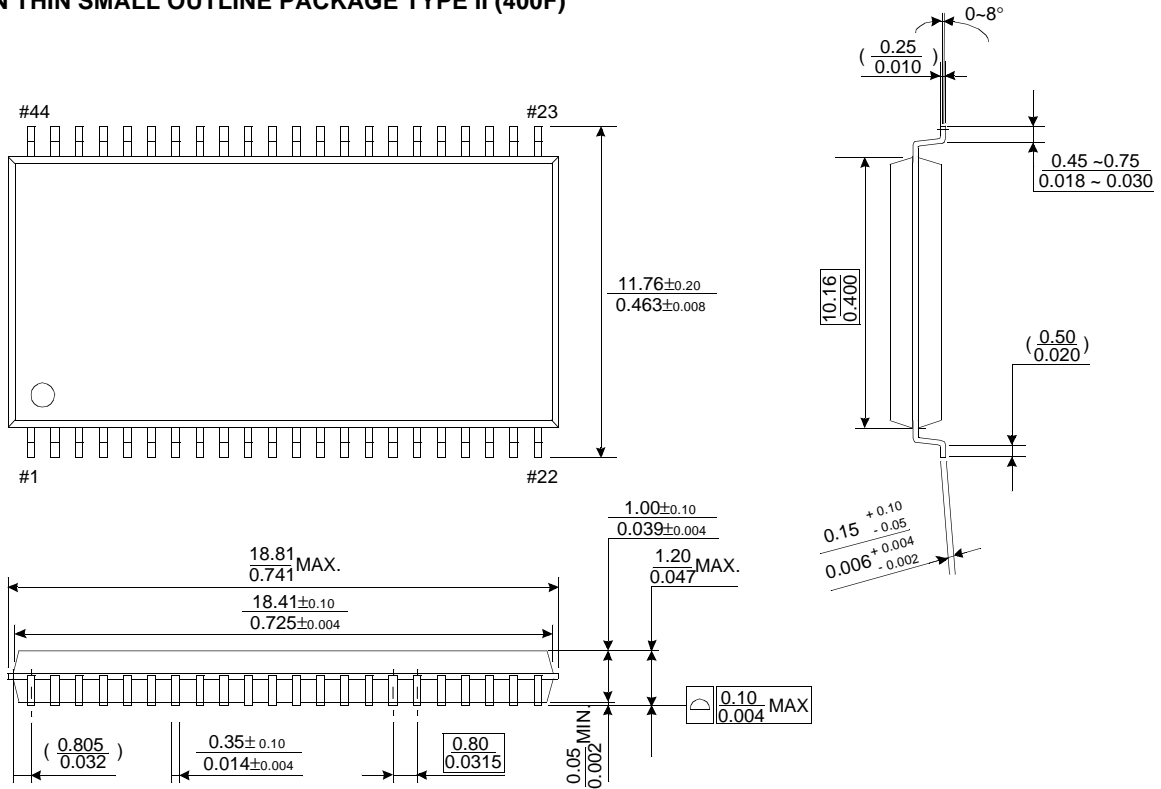
CS_2 controlled



PACKAGE DIMENSIONS

Unit: millimeters(inches)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

