32K x 8 Bit High-Speed BiCMOS Static RAM

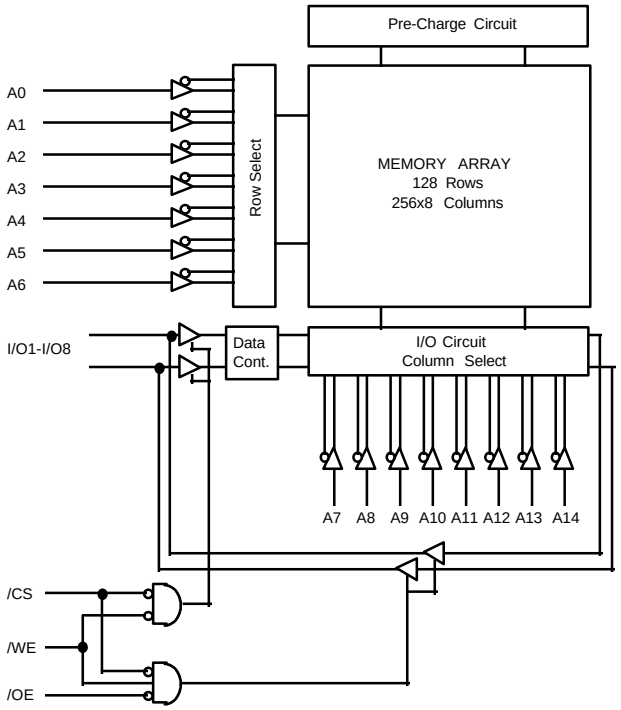
FEATURES

- Fast Access Time 6,7,8ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 110 mA(Max.)
  - (CMOS) : 20 mA(Max.)
  - Operating Current : 170 mA(f=100MHz)
- Single 5V ± 5% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68B261AJ : 32-SOJ-300

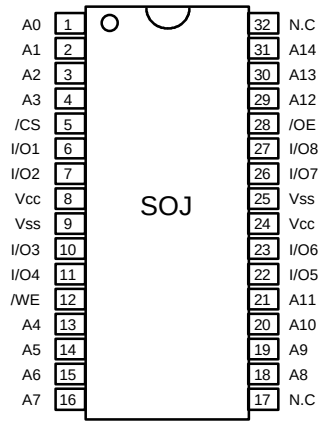
GENERAL DESCRIPTION

The KM68B261A is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68B261A uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung`s advanced BiCMOS process and designed for high-speed system applications. It is particularly well suited for use in high-density high-speed system applications. The KM68B261A is packaged in a 300 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



PIN DESCRIPTION

Pin Name	Pin Function
A0-A14	Address Inputs
/WE	Write Enable
/CS	Chip Select
/OE	Output Enable
I/O1-I/O8	Data Inputs/Outputs
Vcc	Power (5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	VIN,OUT	- 0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	- 0.5 to 7.0	V
Power Dissipation	PD	1.0	W
Storage Temperature	Tstg	- 65 to 150	°C
Operating Temperature	TA	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	4.75	5.0	5.25	V
Ground	Vss	0	0	0	V
Input Low Voltage	VIH	2.2	-	Vcc+0.5**	V
Input High Voltage	VIL	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0 (Pulse Width ≤3ns) for I ≤ 20mA

** V_{IH}(Max) = Vcc+2.0V(Pulse width ≤ 8ns)for I ≤20mA

DC AND OPERATING CHARACTERISTICS

(TA= 0 to 70°C, Vcc=5 V ± 5%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	ILI	VIN=Vss to Vcc	-10	10	µA
Output Leakage Current	ILO	/CS=VIH or /OE=VIH or /WE=VIL V_{OUT}=Vss to Vcc	-10	10	µA
Operating Current	ICC	f=100MHz, 100% Duty, /CS=VIL, VIN=VIH or VIL, IOUT=0mA	-	170	mA
Standby Current	ISB	Min. Cycle, /CS=VIH	-	110	mA
	ISB1	f=0MHz, /CS ≥ Vcc-0.2V, VIN ≥ Vcc -0.2V or VIN ≤ 0.2V	-	20	mA
Output Low Voltage	VOL	IOL=8mA	-	0.4	V
Output High Voltage	VOH	IOH = - 4mA	2.4	-	V

CAPACITANCE*(f=1MHz, TA =25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	CIN	VIN=0V	-	7	pF
Input/Output Capacitance	CI/O	VI/O=0V	-	7	pF

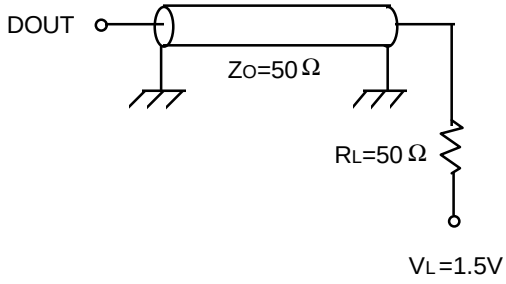
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

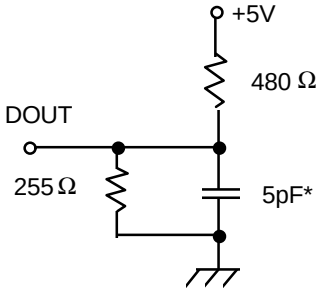
TEST CONDITIONS ON DATA RAM (TA= 0 to 70° C, Vcc=5V± 5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
for tHZ, tLZ, tWHZ, tOW, tOLZ, & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

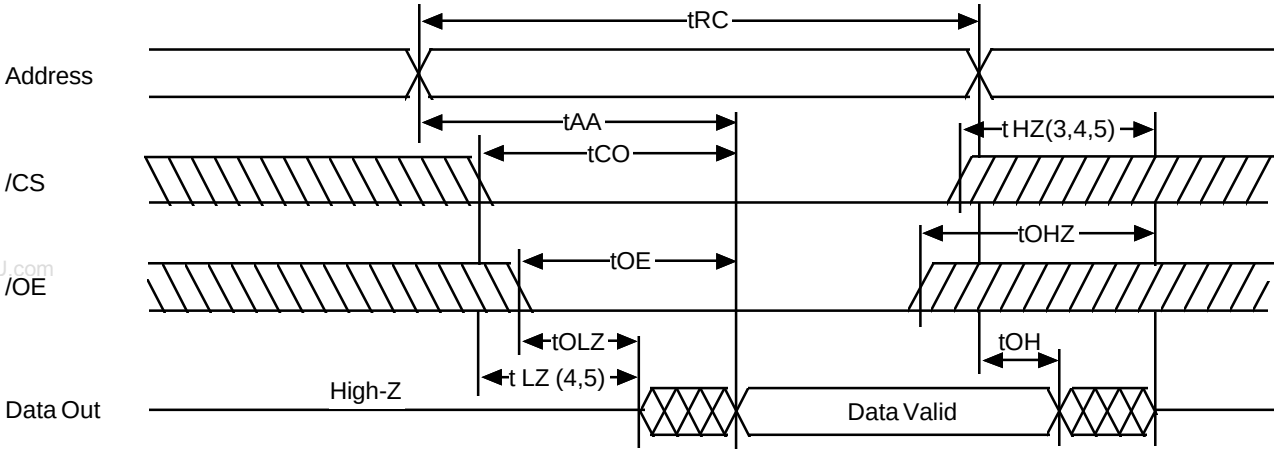
Parameter	Symbol	KM68B261A-6		KM68B261A -7		KM68B261A -8		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	6	-	7	-	8	-	ns
Address Access Time	tAA	-	6	-	7	-	8	ns
Chip Select to Output	tCO	-	6	-	7	-	8	ns
Output Enable to Valid Output	tOE	-	4	-	4	-	4	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	1	-	1	-	1	-	ns
Chip Disable to High-Z Output	tHZ	0	3	0	3.5	0	4	ns
Output Disable to High-Z Output	tOHZ	0	3	0	3.5	0	4	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns

WRITE CYCLE

Parameter	Symbol	KM68B261A -6		KM68B261A -7		KM68B261A -8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	6	-	7	-	8	-	ns
Chip Select to End of Write	tCW	6	-	7	-	8	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	3.5	-	4	-	4.5	-	ns
Write Pulse Width(/OE High)	tWP	3.5	-	4	-	4.5	-	ns
Write Pulse Width(/OE Low)	tWP	6	-	7	-	8	-	ns
Write Recovery Time	tWR	1	-	1	-	1	-	ns
Write to Output High-Z	tWHZ	0	3	0	3.5	0	4	ns
Data to Write Time Overlap	tDW	3	-	3.5	-	4	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	3	-	3	-	3	-	ns

TIMING DIAGRAMS

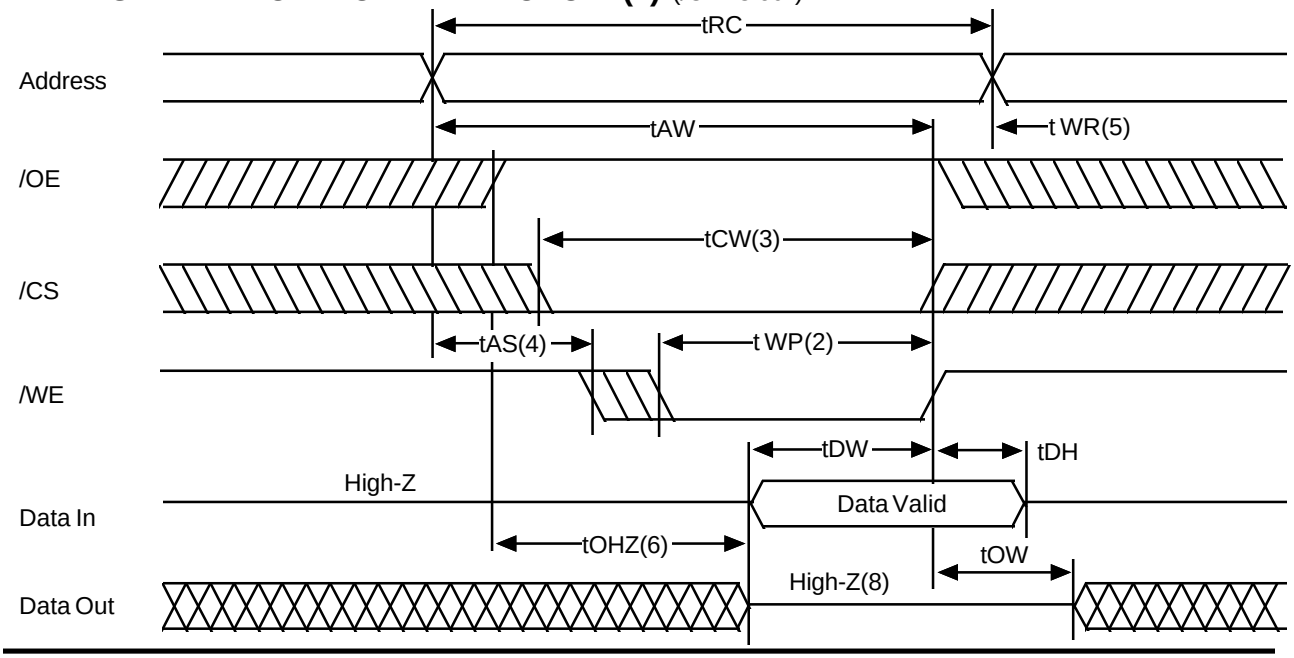
TIMING WAVE FORM OF READ CYCLE (/WE=VIH)



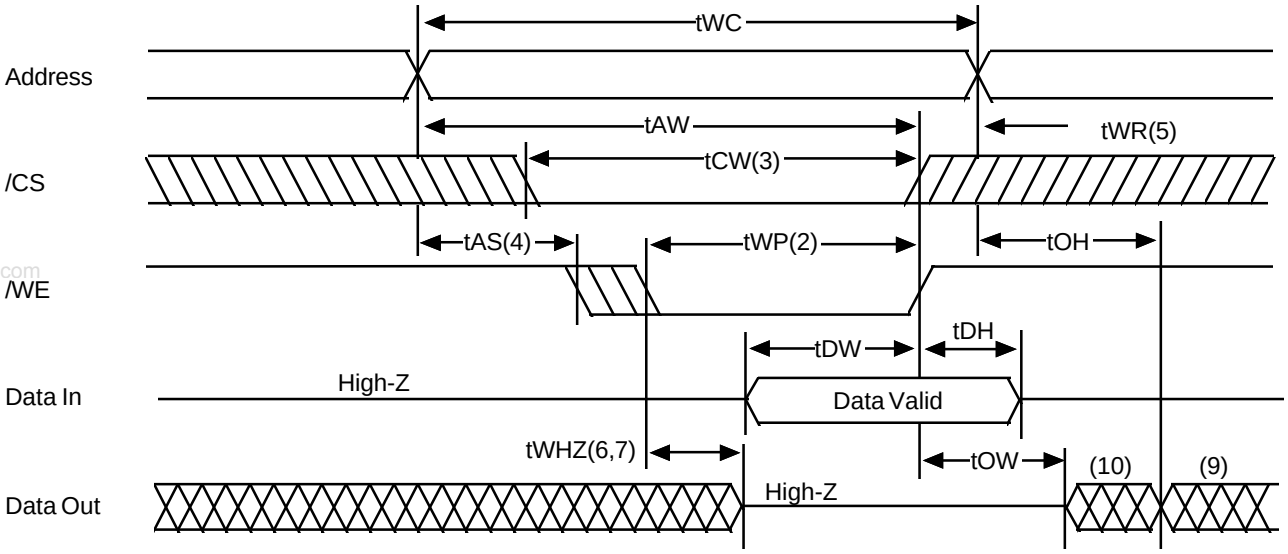
NOTES (READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit condition and are not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ± 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=VIL
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVE FORM OF WRITE CYCLE(1) (/OE=Clock)



TIMING WAVE FORM OF WRITE CYCLE(2) (/OE Low Fixed)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low; A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of /CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS, or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

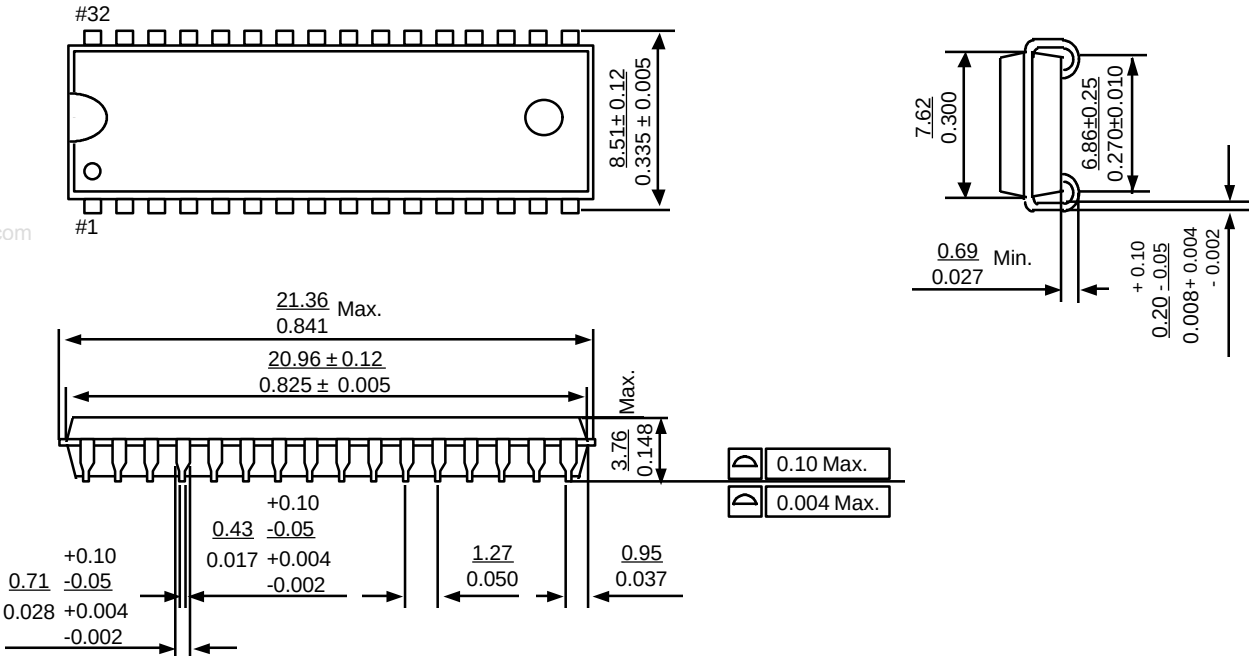
/CS	/WE	/OE	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	ICC
L	H	L	Read	DOUT	ICC
L	L	X	Write	DIN	ICC

*Note : X means Don't Care.

PACKAGE DIMENSIONS

Unit: mm / Inch

32-SOJ-300



*Note : Do not include mold protrusion