

**Document Title****32Kx8 Bit High Speed Static RAM(3.3V Operating), Evolutionary Pin out.****Revision History**

<b><u>RevNo.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
Rev. 0.0	Initial release with Preliminary.	Jun. 1st, 1994	Preliminary
Rev. 1.0	Release to final Data Sheet. 1. Delete Preliminary	Oct. 4th, 1994	Final
Rev. 2.0	2.1. Add 28-TSOP1 Package.	Feb. 22th, 1996	Final
Rev. 3.0	3.1. Delete DIP Package. 3.2. Delete 20ns part 3.3. Add Capacitive load of the test environment in A.C test load	Feb. 25th, 1998	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



**32K x 8 Bit High-Speed CMOS Static RAM (3.3V Operating)**

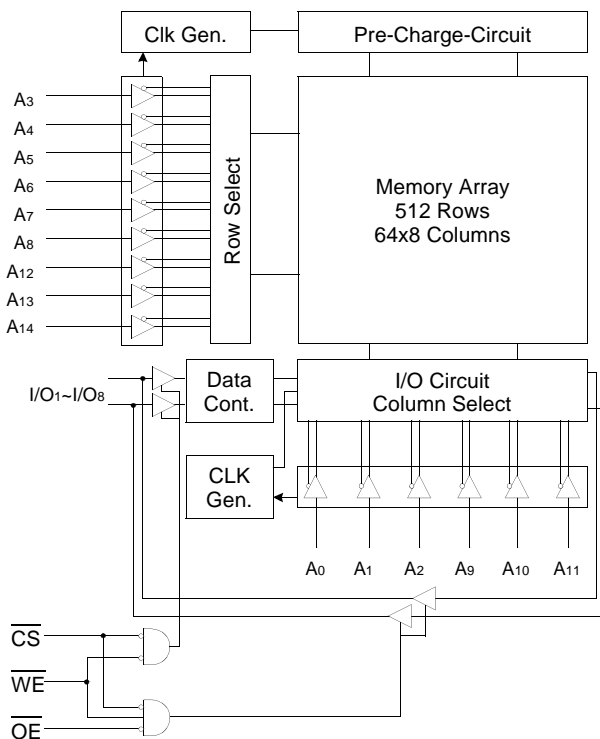
**FEATURES**

- Fast Access Time 15, 17ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 30mA(Max.)
  - (CMOS) : 0.1mA(Max.)
  - Operating KM68V257C - 15 : 90mA(Max.)
  - KM68V257C - 17 : 80mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention; L-ver. only
- Standard Pin Configuration
  - KM68V257CJ : 28-SOJ-300
  - KM68V257CTG : 28-TSOP1-0813, 4F

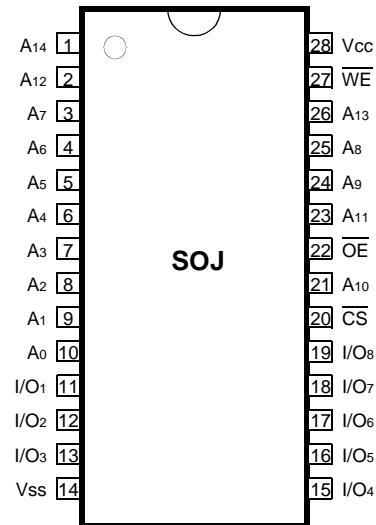
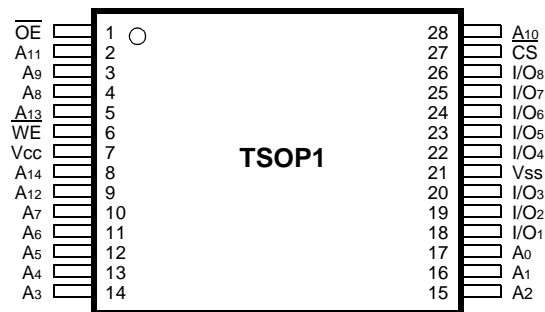
**GENERAL DESCRIPTION**

The KM68V257C is a 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bits. The KM68V257C uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V257C is packaged in a 300mil 28-pin plastic SOJ or TSOP1 forward.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION (Top View)**



**PIN FUNCTION**

Pin Name	Pin Function
A0 - A14	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground

**ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.3*	-	0.8	V

\* V<sub>IL</sub>(Min) = -2.0(Pulse Width ≤ 12ns) for I ≤ 20mA

\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub>+2.0V(Pulse Width ≤ 12ns) for I ≤ 20mA

**DC AND OPERATING CHARACTERISTICS**(T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	15ns	-	90	mA
			17ns	-	80	
Standby Current	I <sub>SB</sub>	Min. Cycle, $\overline{CS}=V_{IH}$	-	30	mA	
	I <sub>SB1</sub>	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	-	0.1		
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA	-	0.4	V	
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA	2.4	-	V	

**CAPACITANCE\***(T<sub>A</sub>=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	7	pF

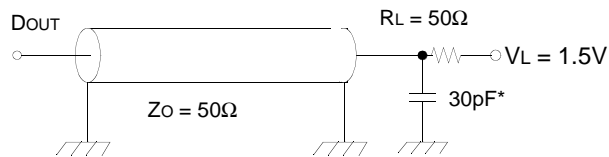
\* Capacitance is sampled and not 100% tested.

## AC CHARACTERISTICS (TA=0 to 70°C, VCC=3.3±0.3V, unless otherwise noted.)

### TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

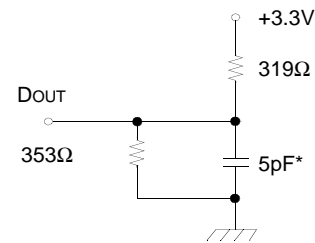
Output Loads(A)



\* Capacitive Load consists of all components of the test environment.

Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Including Scope and Jig Capacitance

### READ CYCLE

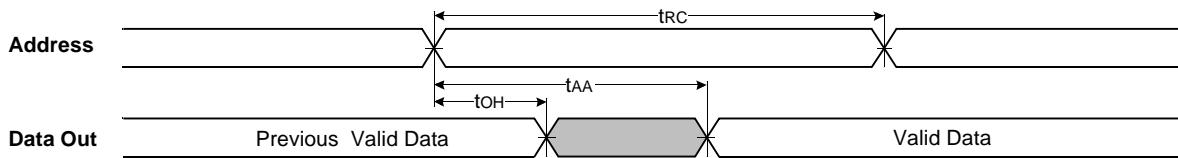
Parameter	Symbol	KM68V257C-15		KM68V257C-17		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	15	-	17	-	ns
Address Access Time	tAA	-	15	-	17	ns
Chip Select to Output	tCO	-	15	-	17	ns
Output Enable to Valid Output	tOE	-	7	-	8	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	7	0	8	ns
Output Disable to High-Z Output	tOHZ	0	7	0	8	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	15	-	17	ns

**WRITE CYCLE**

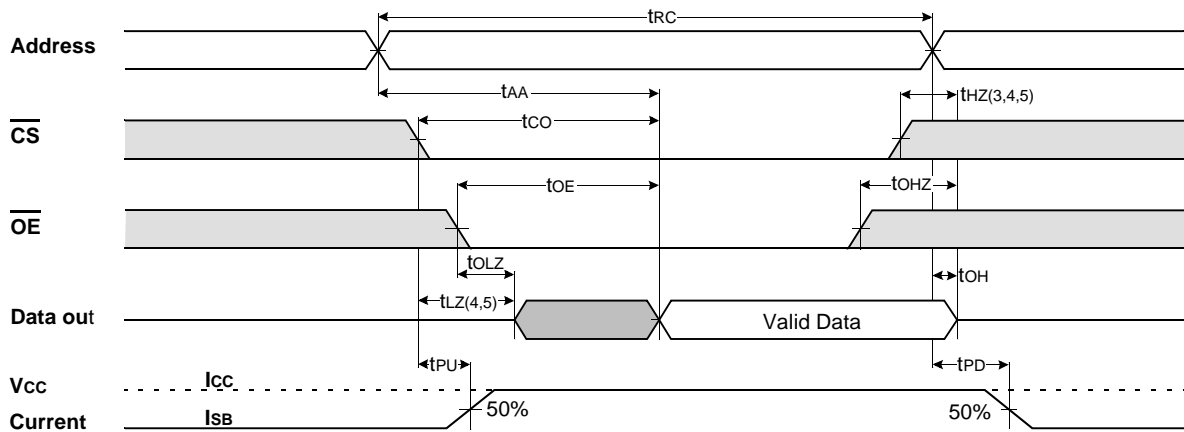
Parameter	Symbol	KM68V257C-15		KM68V257C-17		Unit
		Min	Max	Min	Max	
Write Cycle Time	tWC	15	-	17	-	ns
Chip Select to End of Write	tCW	11	-	12	-	ns
Address Setup Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	11	-	12	-	ns
Write Pulse Width( $\overline{OE}$ High)	tWP	11	-	12	-	ns
Write Pulse Width( $\overline{OE}$ Low)	tWP1	15	-	17	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	6	ns
Data to Write Time Overlap	tdW	8	-	8	-	ns
Data Hold from Write Time	tdH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

**TIMMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



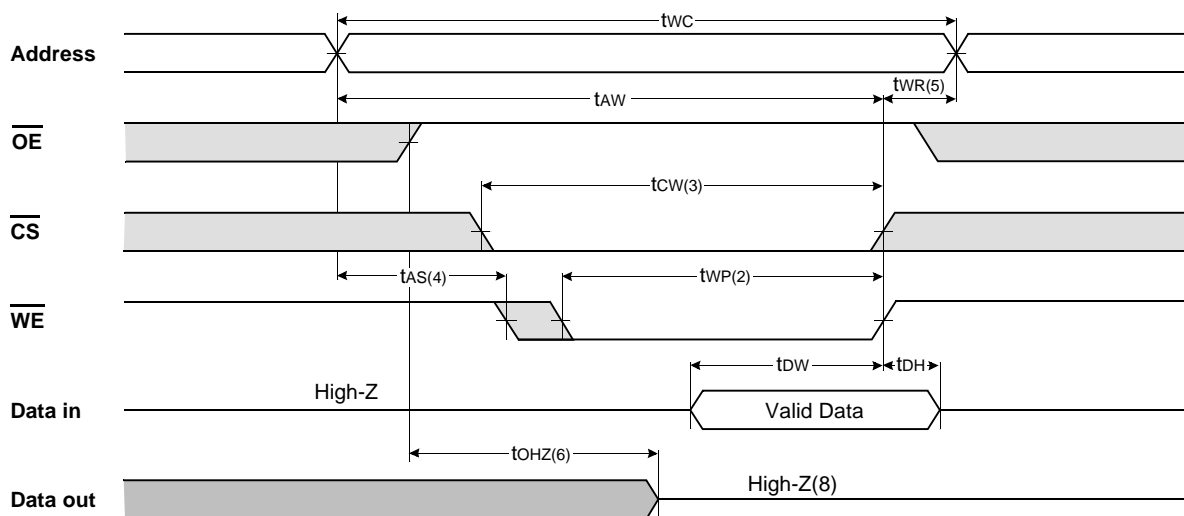
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



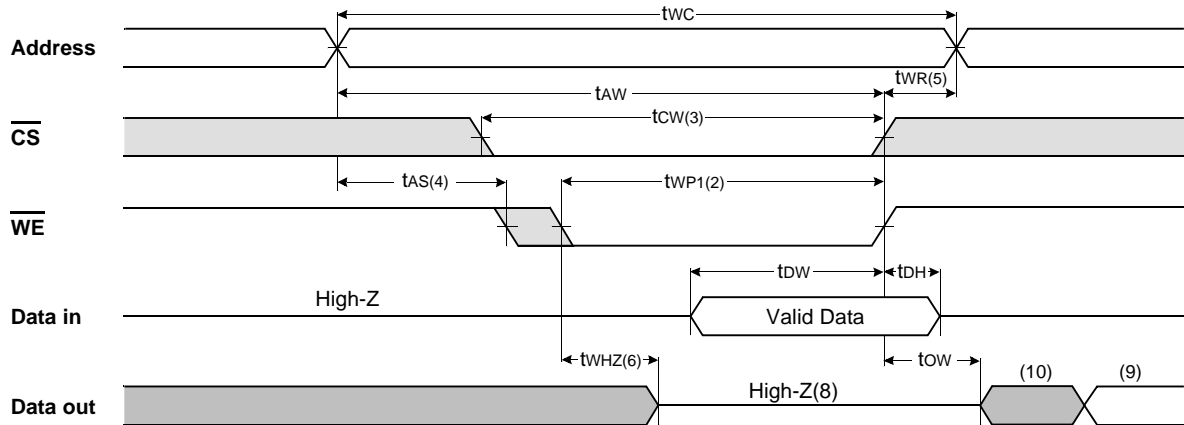
NOTES(READ CYCLE)

- $\overline{WE}$  is high for read cycle.
- All read cycle timing is referenced from the last valid address to the first transition address.
- $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
- At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
- Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
- Device is continuously selected with  $\overline{CS}=V_{L}$ .
- Address valid prior to coincident with  $\overline{CS}$  transition low.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

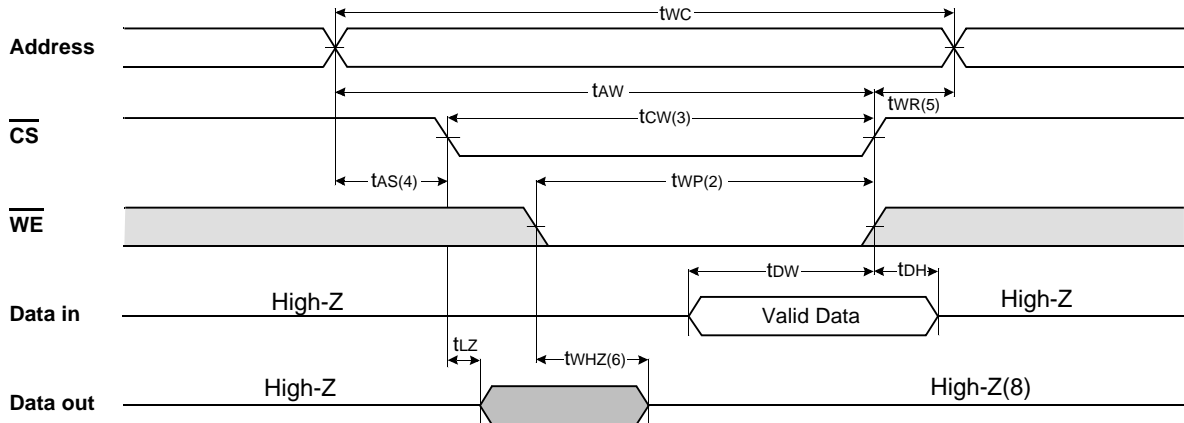
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}=\text{Clock}$ )



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$ =Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$  = Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$  and  $\overline{WE}$ . A write begins at the latest transition  $\overline{CS}$  going low and  $\overline{WE}$  going low ; A write ends at the earliest transition  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9.  $D_{out}$  is the read data of the new address.
10. When  $\overline{CS}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

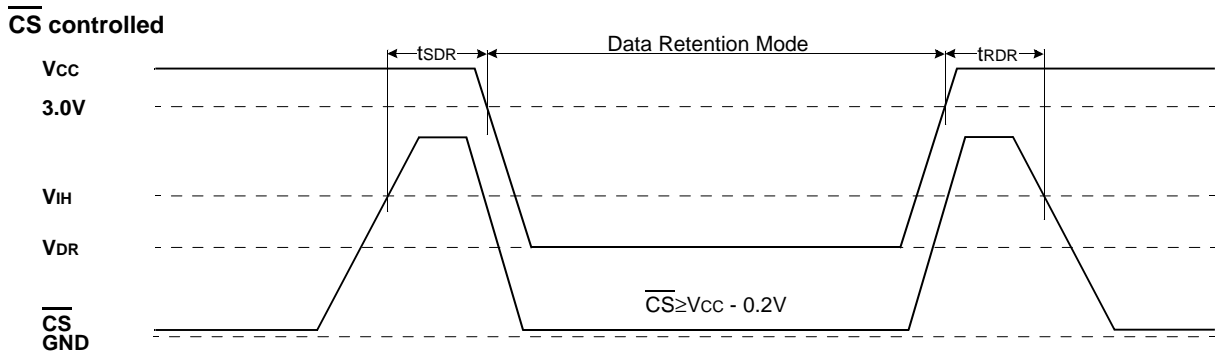
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
L	H	H	Output Disable	High-Z	I <sub>CC</sub>
L	H	L	Read	DOUT	I <sub>CC</sub>
L	L	X	Write	DIN	I <sub>CC</sub>

\* NOTE : X means Don't Care.

DATA RETENTION CHARACTERISTICS (T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 3.0V, $\overline{CS} \geq V_{CC} - 0.2V$	-	-	0.07	mA
Data Retention Set-Up Time	t <sub>SDR</sub>	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	t <sub>RDR</sub>		5	-	-	ms

DATA RETENTION WAVE FORM

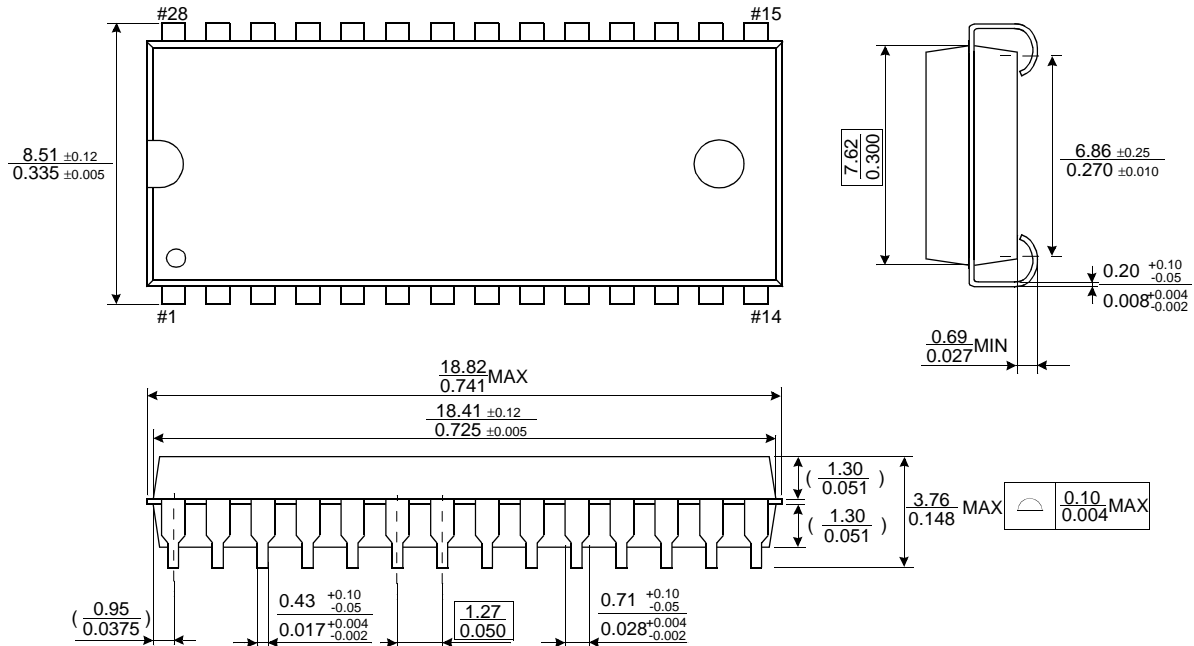




PACKAGE DIMENSIONS

28-SOJ-300

Units: millimeters/Inches



28-TSOP1-0813.4F

Units: millimeters/Inches

