KMA010P20Q

P-Ch Trench MOSFET

General Description

It s mainly suitable for battery pack or power management in cell phone, and PDA.

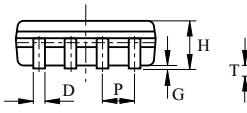
FEATURES

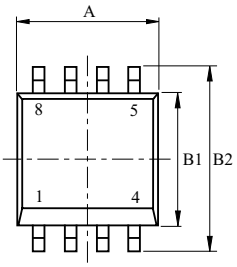
· V_{DSS}=-20V, I_D=-10A.

· Drain-Source ON Resistance.

: $R_{DS(ON)}$=14mΩ (Max.) @ V_{GS}=-4.5V, I_D=-10A.

: $R_{DS(ON)}$=24mΩ (Max.) @ V_{GS}=-2.5V, I_D=-7.6A.





DIM	MILLIMETERS
A	4.85± 0.2
B1	3.94 ± 0.2
B2	6.02± 0.3
D	0.4 ± 0.1
G	0.15+0.1/-0.05
H	1.63± 0.2
L	0.65 ± 0.2
P	1.27
T	0.20+0.1/-0.05

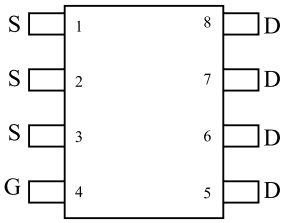
FLP-8

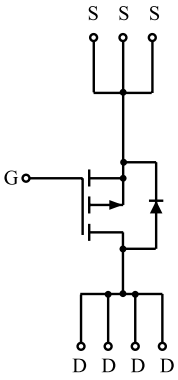
MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current	DC	I_D *	±10	A
	Pulsed (Note1)	I_{DP}*	±48	
Source-Drain Diode Current		I_S *	-2.3	A
Drain Power Dissipation	Ta=25℃	P_D *	1.6	W
	Ta=100℃		0.625	
Maximum Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55～150	℃
Thermal Resistance, Junction to Ambient		R_{thJA} *	80	℃/W

* : Surface Mounted on 1”×1” FR4 Board, t≤5sec.

PIN CONNECTION (TOP VIEW)





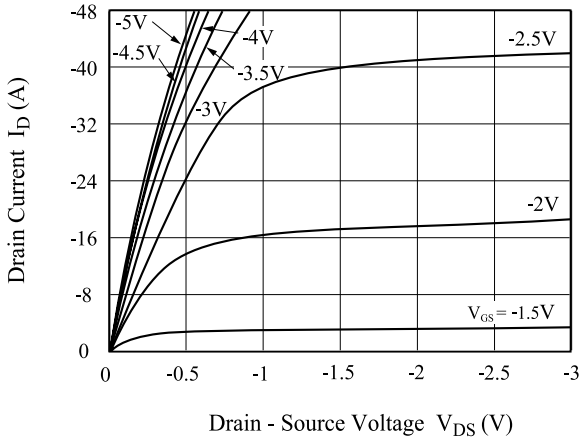
ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250㎂, V_{GS}=0V,	-20	-	-	V
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=-20V	-	-	-1	㎂
		V_{GS}=0V, V_{DS}=-16V, Tj=70℃	-	-	-5	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=-250㎂	-0.6	-	-	V
Gate Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-10A (Note 1)	-	11	14	mΩ
		V_{GS}=-2.5V, I_D=-7.6A (Note 1)	-	18	24	
ON State Drain Current	$I_{D(ON)}$	V_{GS}=-4.5V, V_{DS}=-5V (Note 1)	-48	-	-	A
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_D=-10A (Note 1)	-	31	-	S
Source-Drain Diode Forward Voltage	V_{SD}	I_S=-10A, V_{GS}=0V (Note 1)	-	-	-1.1	V
Dynamic (Note 2)						
Total Gate Charge	Q_g	V_{DS}=-10V, R_D=1.0Ω V_{GS}=-4.5V (Fig.1)	-	36	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	13	-	
Turn-on Delay time	$t_{d(on)}$	V_{DD}=-10V, R_D=1.0Ω, V_{GS}=-4.5V, R_G=6Ω (Fig.2)	-	10	-	ns
Turn-on Rise time	t_r		-	72	-	
Turn-off Delay time	$t_{d(off)}$		-	78	-	
Turn-off Fall time	t_f		-	108	-	

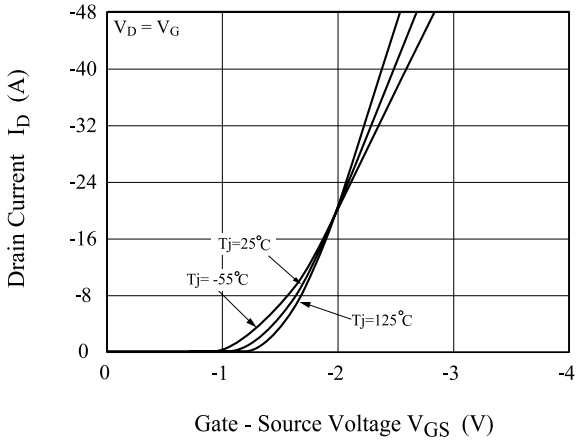
Note 1) Pulse test : Pulse width ≤300㎲, Duty Cycle ≤2%.

Note 2) Guaranteed by design. Not subject to production testing.

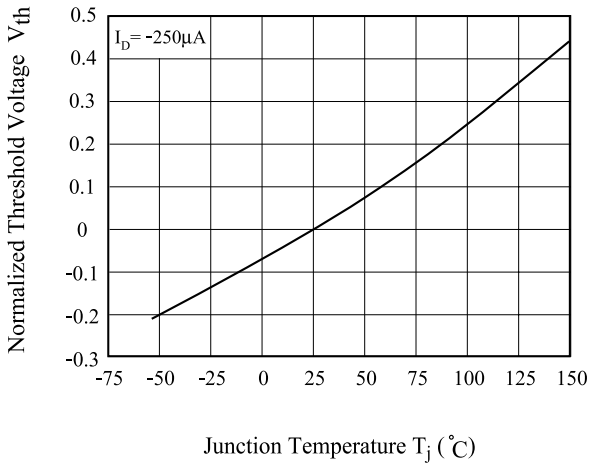
I_D - V_{DS}



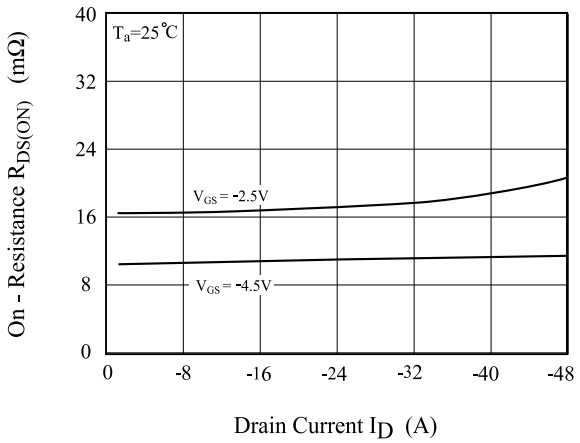
I_D - V_{GS}



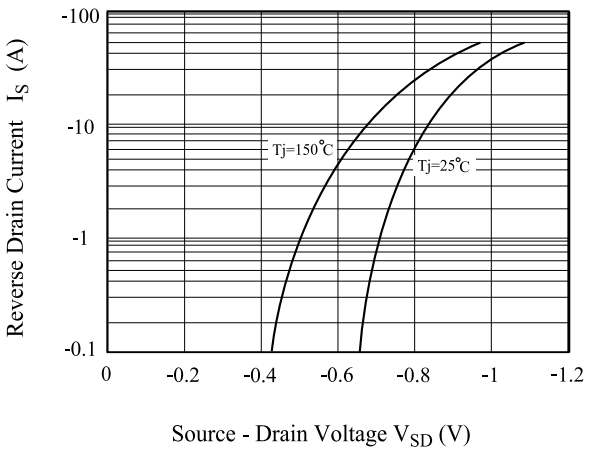
V_{th} - T_j



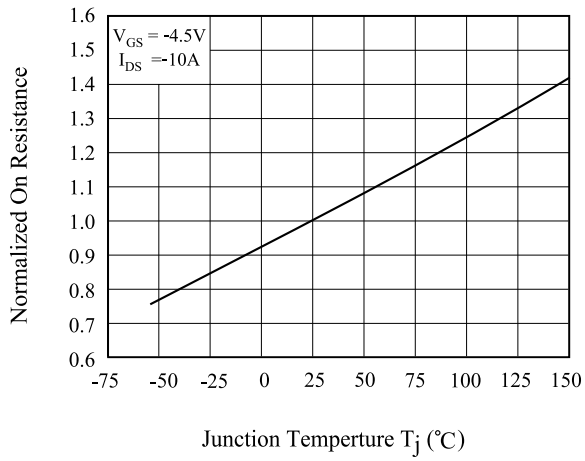
$R_{DS(ON)}$ - I_D



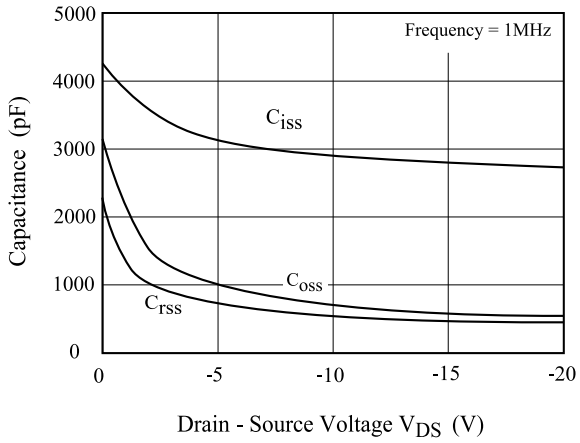
I_S - V_{SD}



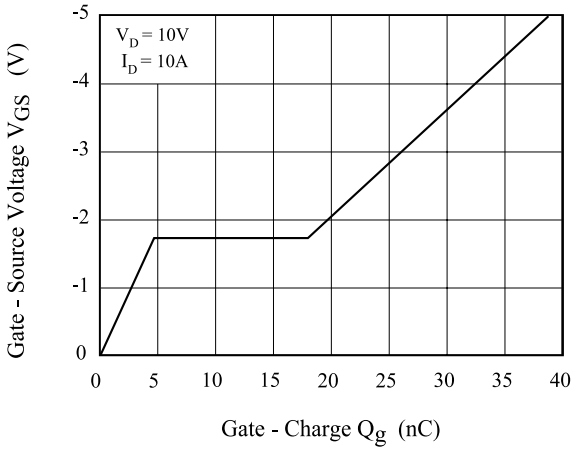
$R_{DS(ON)}$ - T_j



C - V_{DS}



Q_g - V_{GS}



R_{th}

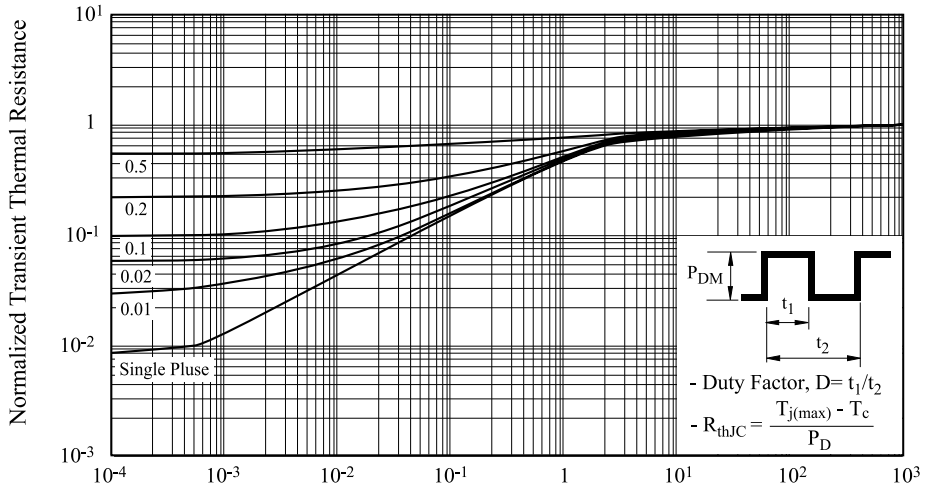


Fig. 1 Gate Charge

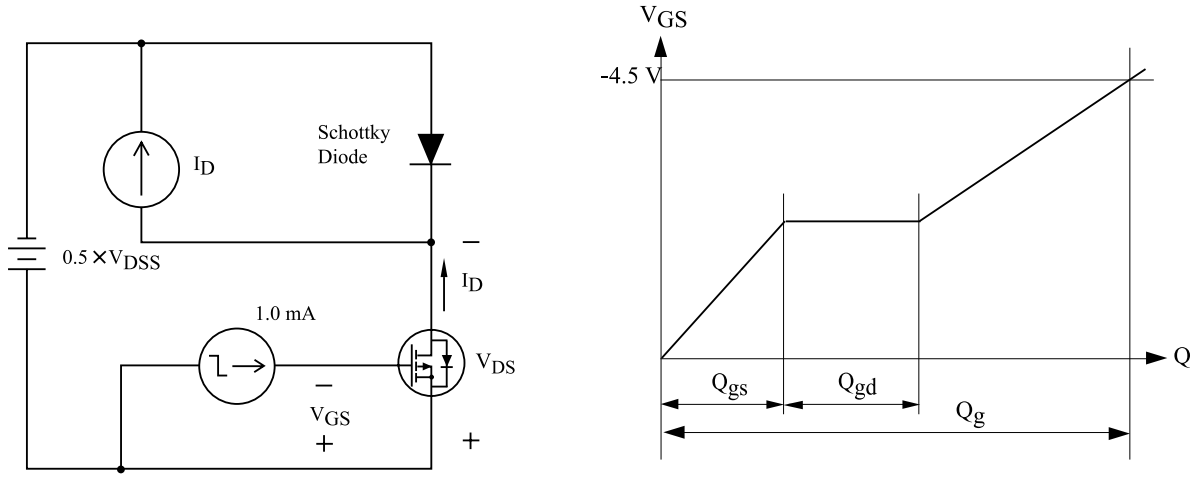


Fig. 2 Resistive Load Switching