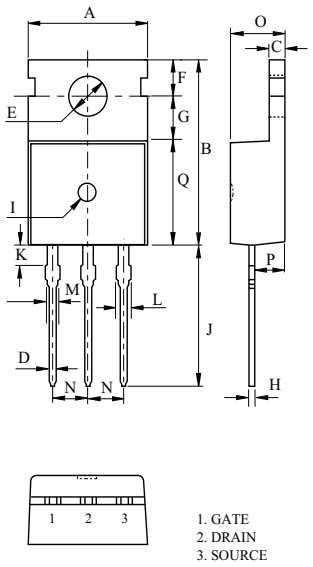
# KMB075N75P

**N CHANNEL MOS FIELD EFFECT TRANSISTOR**

## General Description

This planar stripe MOSFET has better characteristics, such as fast switching time, low on resistance, low gate charge and excellent avalanche characteristics. It is mainly suitable for active power factor correction , electronic lamp ballasts based on half bridge topology and switching mode power supplies.

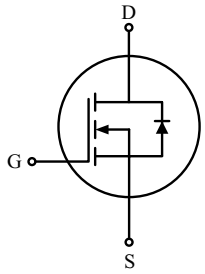



| DIM | MILLIMETERS |
|---|---|
| A | 9.9± 0.2 |
| B | 15.95 MAX |
| C | 1.3+0.1/-0.05 |
| D | 0.8± 0.1 |
| E | ø 3.6 ±0.2 |
| F | 2.8± 0.1 |
| G | 3.7 |
| H | 0.5+0.1/-0.05 |
| I | ø 1.5 |
| J | 13.08± 0.3 |
| K | 1.46 |
| L | 1.4± 0.1 |
| M | 1.27± 0.1 |
| N | 2.54± 0.2 |
| O | 4.5± 0.2 |
| P | 2.4± 0.2 |
| Q | 9.2± 0.2 |

TO-220AB

## FEATURES

- $V_{DSS}$= 75V, $I_D$= 75A
- Drain-Source ON Resistance :
  $R_{DS(ON)}$=0.017 Ω @$V_{GS}$ = 10V
- Qg(typ.) = 85nC
- Improved dv/dt capacity, high Ruggedness
- Maximum Junction Temperature Range (175℃)




## MAXIMUM RATING (Tc=25℃)

| CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 75 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Drain Current | @$T_C$=25℃ | $I_D$ | 75 | A |
| | @$T_C$=100℃ | | 52.5 | |
| | Pulsed (Note1) | $I_{DP}$ | 300 | |
| Single Pulsed Avalanche Energy (Note 2) | | $E_{AS}$ | 1350 | mJ |
| Repetitive Avalanche Energy (Note 1) | | $E_{AR}$ | 19 | mJ |
| Peak Diode Recovery dv/dt (Note 3) | | dv/dt | 7.0 | V/ns |
| Drain Power Dissipation | Tc=25℃ | $P_D$ | 190 | W |
| | Derate above 25℃ | | 1.27 | W/℃ |
| Maximum Junction Temperature | | $T_j$ | 175 | ℃ |
| Storage Temperature Range | | $T_{stg}$ | -55～175 | ℃ |
| **Thermal Characteristics** | | | | |
| Thermal Resistance, Junction-to-Case | | $R_{thJC}$ | 0.79 | ℃/W |
| Thermal Resistance, Case-to-Sink | | $R_{thCS}$ | 0.5 | ℃/W |
| Thermal Resistance, Junction-to-Ambient | | $R_{thJA}$ | 62.5 | ℃/W |

**ELECTRICAL CHARACTERISTICS (Tc=25℃)**

| CHARACTERISTIC | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$=250㎂, $V_{GS}$=0V | 75 | - | - | V |
| Breakdown Voltage Temperature Coefficient | $\Delta BV_{DSS}/\Delta T_j$ | $I_D$=250㎂, Referenced to 25℃ | - | 0.08 | - | V/℃ |
| Drain Cut-off Current | $I_{DSS}$ | $V_{DS}$=75V, $V_{GS}$=0V, | - | - | 10 | ㎂ |
| Gate Threshold Voltage | $V_{th}$ | $V_{DS}$=$V_{GS}$, $I_D$=250㎂ | 2.0 | - | 4.0 | V |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| Drain-Source ON Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=37.5A | - | 0.013 | 0.017 | Ω |
| **Dynamic** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$= 60V, $I_D$= 75A<br>$V_{GS}$=10V (Note4,5) | - | 85 | 110 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 15 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 40 | - | |
| Turn-on Delay time | $t_{d(on)}$ | $V_{DD}$= 37.5V<br>$I_D$=75A<br>$R_G$= 25 Ω (Note4,5) | - | 25 | 60 | ns |
| Turn-on Rise time | $t_r$ | | - | 300 | 700 | |
| Turn-off Delay time | $t_{d(off)}$ | | - | 150 | 310 | |
| Turn-off Fall time | $t_f$ | | - | 180 | 370 | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25V, $V_{GS}$=0V, f=1.0MHz | - | 3000 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 250 | - | |
| Output Capacitance | $C_{oss}$ | | - | 1100 | - | |
| **Source-Drain Diode Ratings** | | | | | | |
| Continuous Source Current | $I_S$ | $V_{GS}$<$V_{th}$ | - | - | 75 | A |
| Pulsed Source Current | $I_{SP}$ | | - | - | 300 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=75A, $V_{GS}$=0V | - | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_S$=75A, $V_{GS}$=0V,<br>dIs/dt=100A/㎲ | - | 90 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 250 | - | ㎌ |

Note 1) Repetivity rating : Pulse width limited by junction temperature.

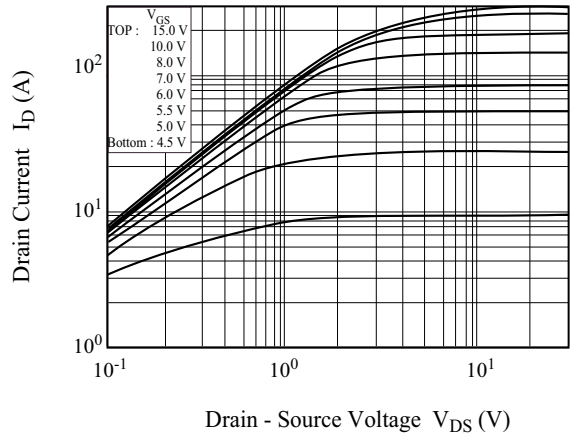
Note 2) L=0.32mH, $I_S$=75A, $V_{DD}$=25V, $R_G$=25 Ω, Starting $T_j$=25℃.

Note 3) $I_S \leq$75A, dI/dt≤300A/㎲, $V_{DD} \leq BV_{DSS}$, Starting $T_j$=25℃.

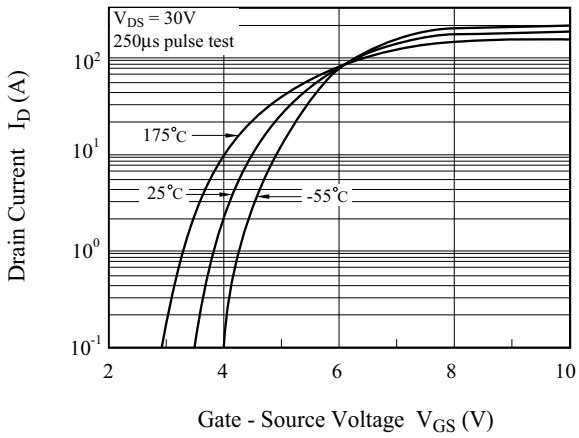
Note 4) Pulse Test : Pulse width ≤300㎲, Duty Cycle ≤2%.

Note 5) Essentially independent of operating temperature.

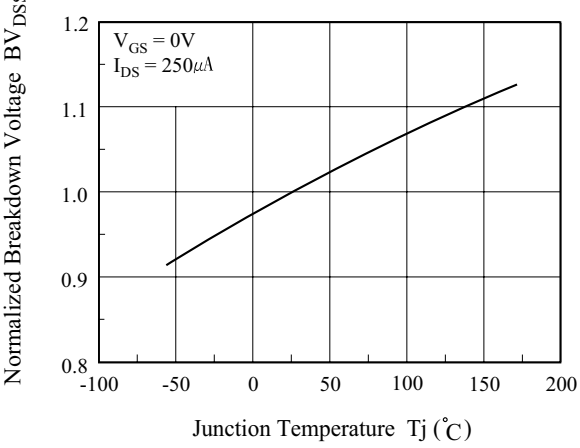
$I_D$ - $V_{DS}$



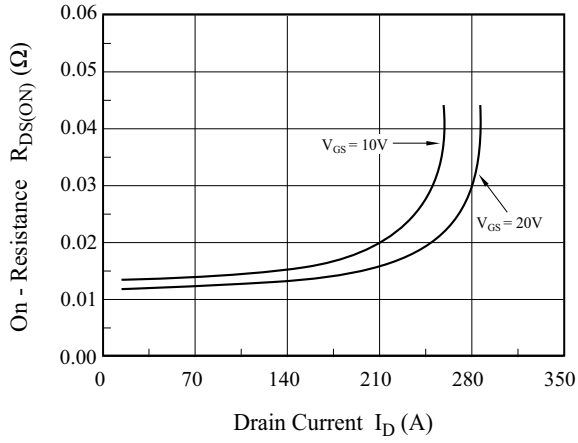

$I_D$ - $V_{GS}$



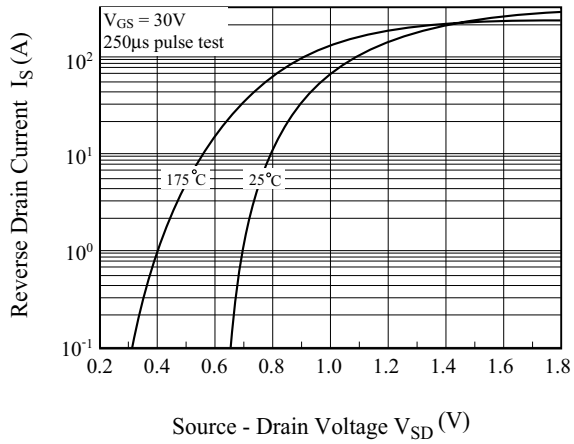

$BV_{DSS}$ - $T_j$



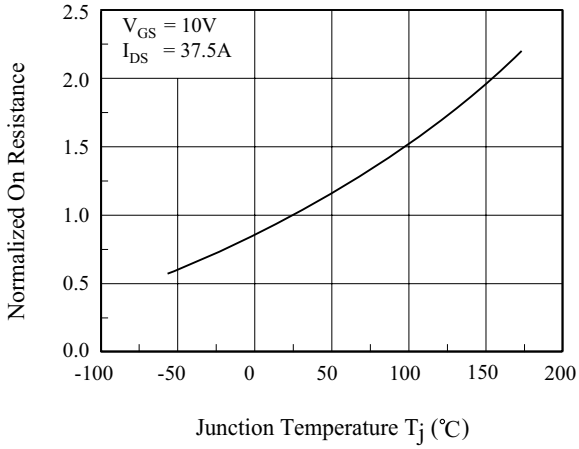

$R_{DS(ON)}$ - $I_D$



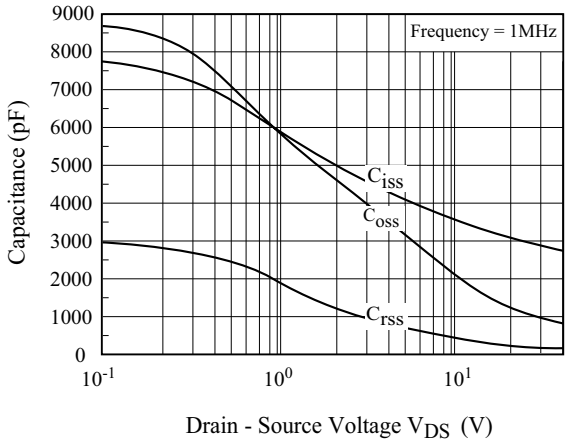

$I_S$ - $V_{SD}$



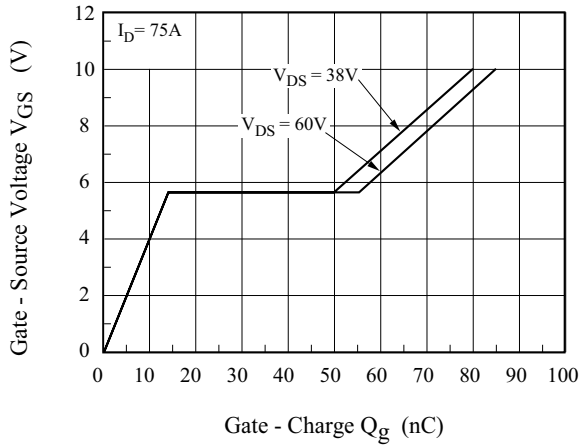

$R_{DS(ON)}$ - $T_j$



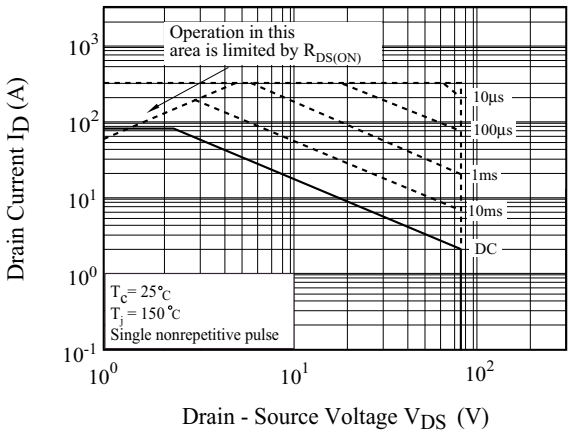
C - $V_{DS}$



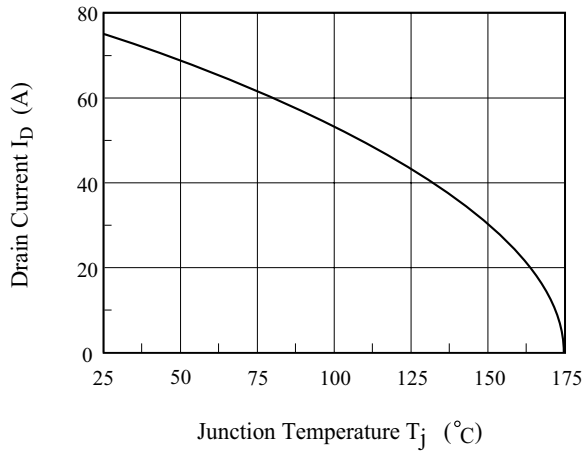

$Q_g$- $V_{GS}$



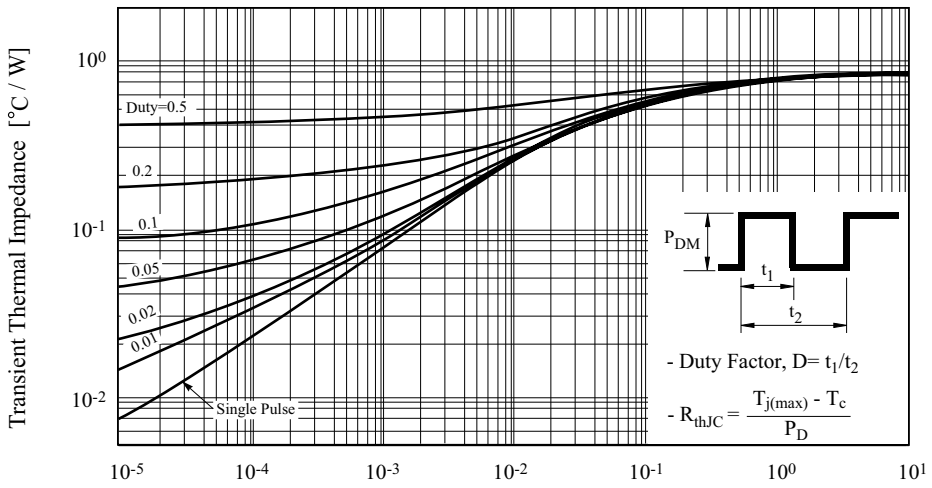

Safe Operation Area



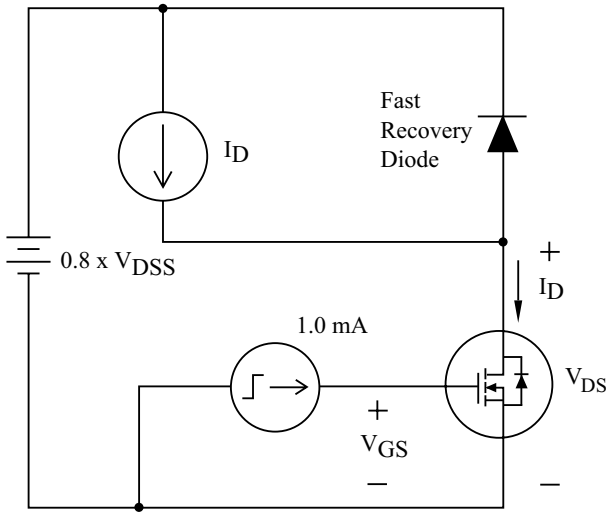

$I_D$ - $T_j$

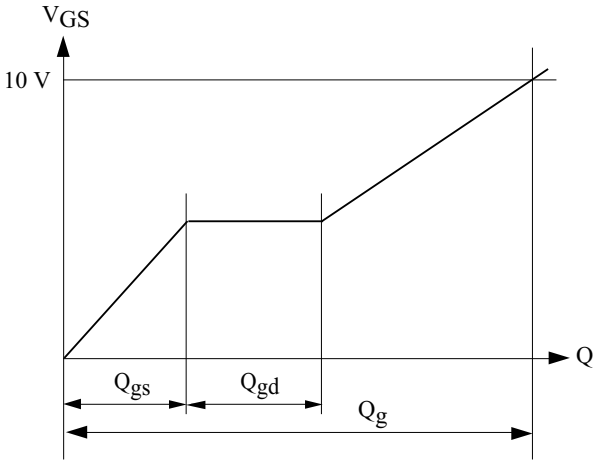



$R_{th}$

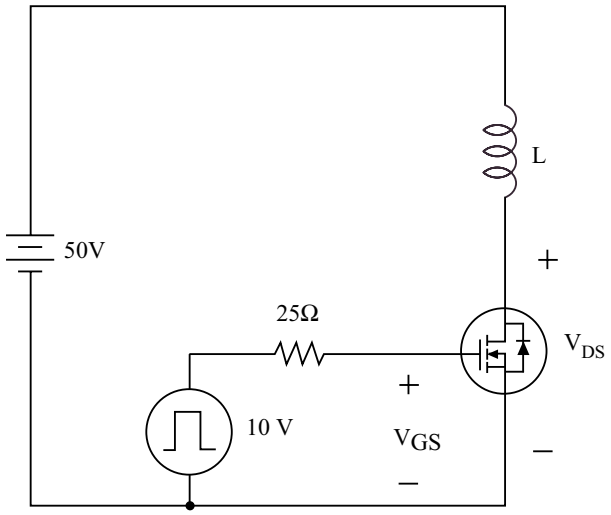


- Gate Charge

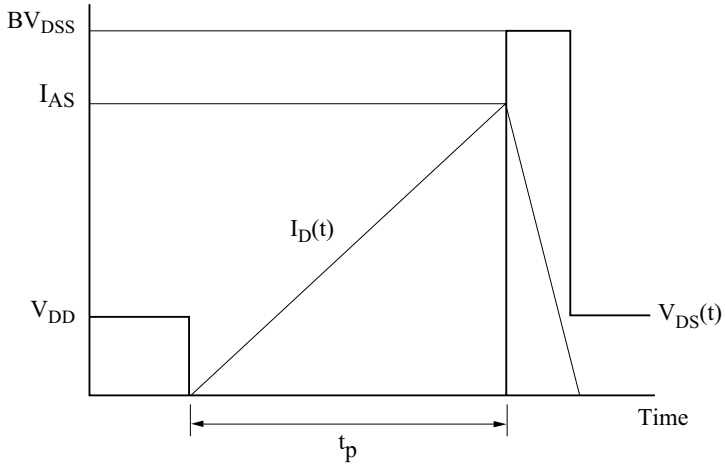


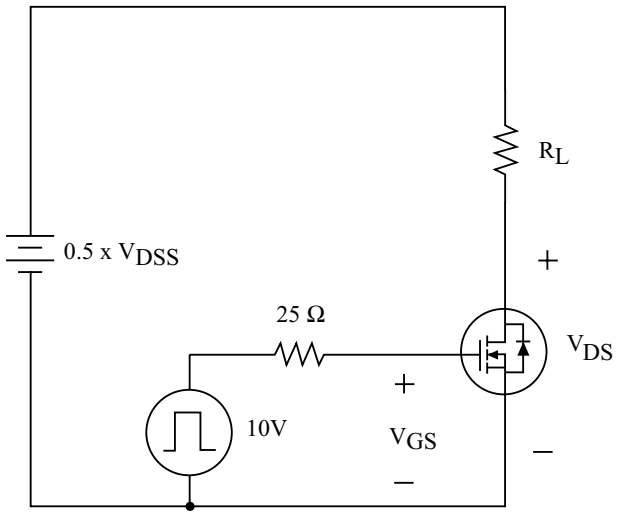

- Single Pulsed Avalanche Energy

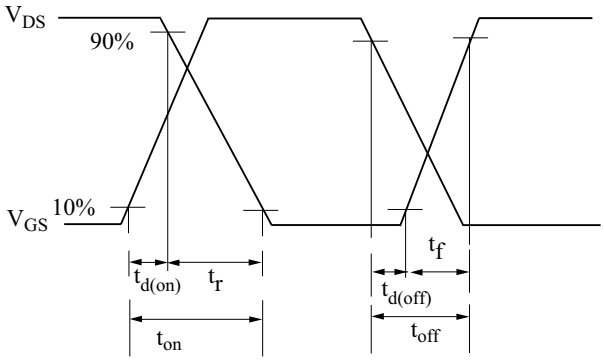



$$E_{AS}= \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$




- Resistive Load Switching



- Source - Drain Diode Reverse Recovery and dv /dt