KML0D6NP20EA

N and P-Ch Trench MOSFET

General Description

It's Mainly Suitable for Load Switching Cell Phones, Battery Powered Systems and Level-Shifter.

FEATURES

· N-Channel

: V_{DSS}=20V, I_D=600mA ($R_{DS(ON)}$=0.70Ω @ V_{GS}=4.5V).

: V_{DSS}=20V, I_D=500mA ($R_{DS(ON)}$=0.85Ω @ V_{GS}=2.5V).

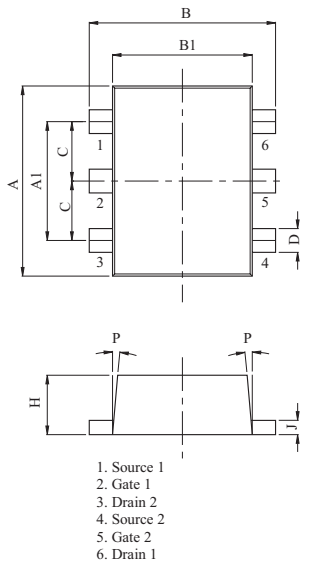
: V_{DSS}=20V, I_D=350mA ($R_{DS(ON)}$=1.25Ω @ V_{GS}=1.8V).

· P-Channel

: V_{DSS}=-20V, I_D=-400mA ($R_{DS(ON)}$=1.2Ω @ V_{GS}=-4.5V).

: V_{DSS}=-20V, I_D=-300mA ($R_{DS(ON)}$=1.6Ω @ V_{GS}=-2.5V).

: V_{DSS}=-20V, I_D=-150mA ($R_{DS(ON)}$=2.7Ω @ V_{GS}=-1.8V).



DIM	MILLIMETERS
A	1.6±0.05
A1	1.0±0.05
B	1.6±0.05
B1	1.2±0.05
C	0.50
D	0.2±0.05
H	0.5±0.05
J	0.12±0.05
P	5°

1. Source 1
2. Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain 1

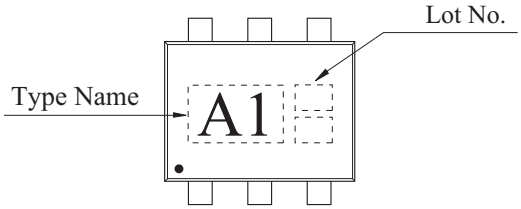
TES6

MAXIMUM RATING (Ta=25℃)

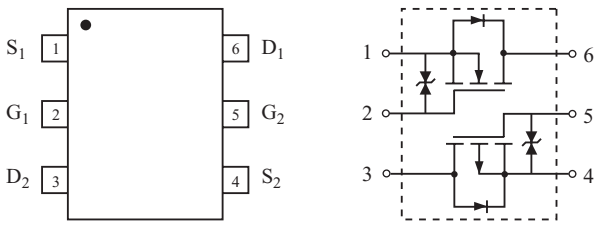
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	20	-20	V
Gate-Source Voltage		V_{GSS}	±6	±6	V
Drain Current	DC @T_A=25℃	I_D*	515	-390	mA
	DC @T_A=85℃		370	-280	
	Pulsed	I_{DP}	650	-650	
Source-Drain Diode Current		I_S	450	-450	
Drain Power Dissipation		P_D*	280	280	mW
Maximum Junction Temperature		T_j	150		℃
Storage Temperature Range		T_{stg}	-55 150		℃
Thermal Resistance, Junction to Ambient		R_{thJA}*	446		℃/W

Note 1) *Surface Mounted on FR4 Board, t≤5sec

Marking



PIN CONNECTION (TOP VIEW)



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V	N-Ch	20	-	-	V
		I_D=-250 μA, V_{GS}=0V	P-Ch	-20	-	-	
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=16V	N-Ch	-	0.3	100	nA
		V_{GS}=0V, V_{DS}=-16V	P-Ch	-	-0.3	-100	
Gate Leakage Current	I_{GSS}	V_{GS}=±4.5V, V_{DS}=0V	N-Ch	-	±0.5	±1.0	μA
			P-Ch	-	±1.0	±2.0	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	N-Ch	0.45	-	1.0	V
		V_{DS}=V_{GS}, I_D=-250 μA	P-Ch	-0.45	-	-1.0	
Drain-Source ON Resistance	$R_{DS(ON)}$*	V_{GS}=4.5V, I_D=600mA	N-Ch	-	0.41	0.70	Ω
		V_{GS}=-4.5V, I_D=-350mA	P-Ch	-	0.80	1.20	
		V_{GS}=2.5V, I_D=500mA	N-Ch	-	0.53	0.85	
		V_{GS}=-2.5V, I_D=-300mA	P-Ch	-	1.20	1.60	
		V_{GS}=1.8V, I_D=350mA	N-Ch	-	0.70	1.25	
		V_{GS}=-1.8V, I_D=-150mA	P-Ch	-	1.80	2.70	
ON State Drain Current	$I_{D(ON)}$*	V_{GS}=4.5V, V_{DS}=5V	N-Ch	700	-	-	mA
		V_{GS}=-4.5V, V_{DS}=-5V	P-Ch	-700	-	-	
Forward Transconductance	g_{fs}*	V_{DS}=10V, I_D=400mA	N-Ch	-	1.0	-	S
		V_{DS}=-10V, I_D=-250mA	P-Ch	-	0.4	-	
Source-Drain Diode Forward Voltage	V_{SD}*	I_S=150mA, V_{GS}=0V	N-Ch	-	0.8	1.2	V
		I_S=-150mA, V_{GS}=0V	P-Ch	-	-0.8	-1.2	
Dynamic							
Total Gate Charge	Q_g*	**N-Ch** : V_{DS}=10V, I_D=250mA, V_{GS}=4.5V **P-Ch** : V_{DS}=-10V, I_D=-250mA, V_{GS}=-4.5V	N-Ch	-	750	-	pC
			P-Ch	-	1500	-	
Gate-Source Charge	Q_{gs}*		N-Ch	-	75	-	
			P-Ch	-	150	-	
Gate-Drain Charge	Q_{gd}*		N-Ch	-	225	-	
			P-Ch	-	450	-	
Turn-on Delay time	$t_{d(on)}$*	**N-Ch** : V_{DD}=10V, I_D=200mA, V_{GS}=4.5V, R_G=10Ω **P-Ch** : V_{DD}=-10V, V_{GS}=-4.5V, I_D=-200mA, R_G=10Ω	N-Ch	-	5	-	ns
			P-Ch	-	5	-	
Turn-off Delay time	$t_{d(off)}$*		N-Ch	-	25	-	
			P-Ch	-	35	-	

Note 2) *Pulse test : Pulse width≤300μs, Duty Cycle≤2%.

N-Channel

Fig 1. I_D - V_{DS}

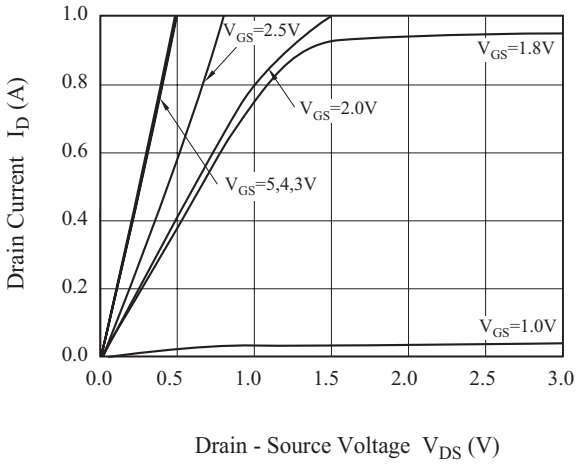


Fig 2. $R_{DS(on)}$ - I_D

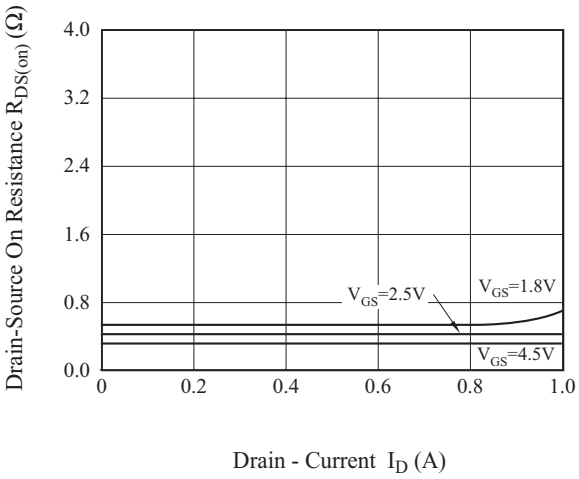


Fig 3. I_D - V_{GS}

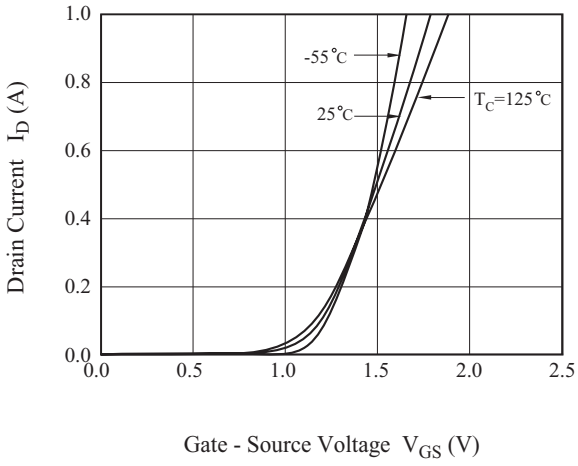


Fig 4. $R_{DS(ON)}$ - T_j

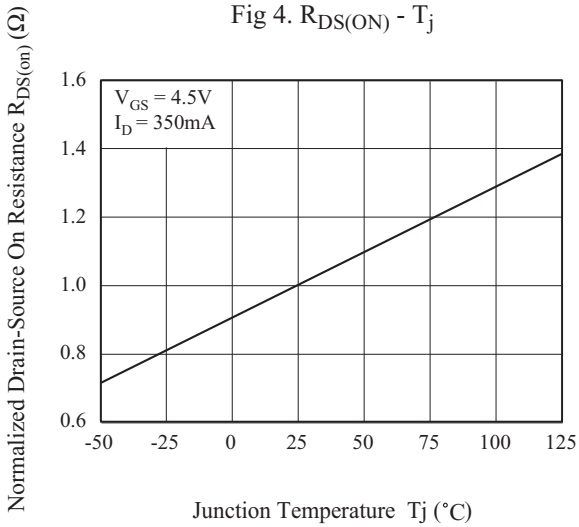


Fig 5. V_{th} - T_j

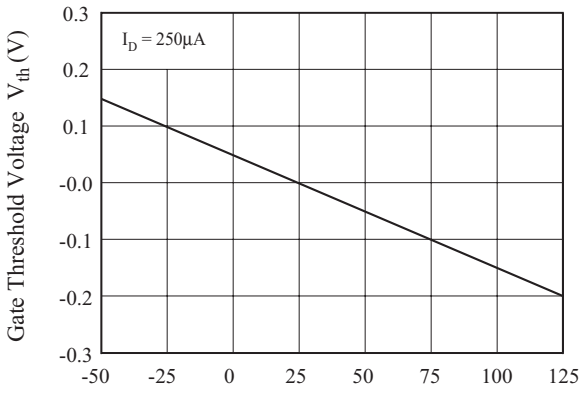


Fig 6. I_{DR} - V_{SDF}

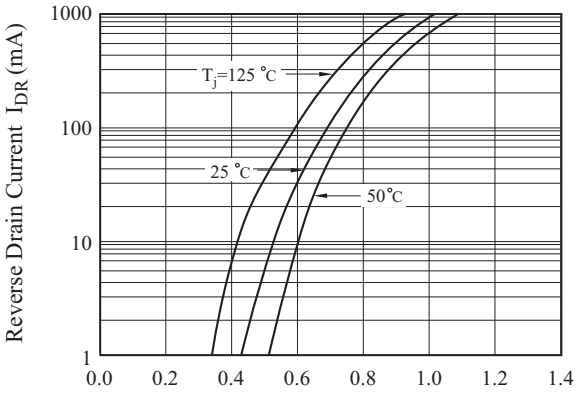


Fig 7. V_{GS} - Q_g

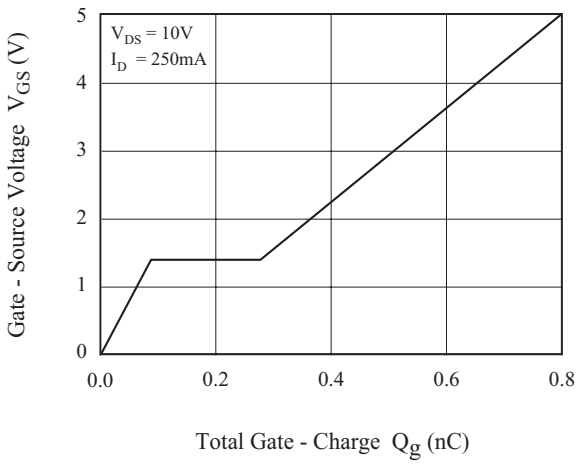


Fig 8. C - V_{DS}

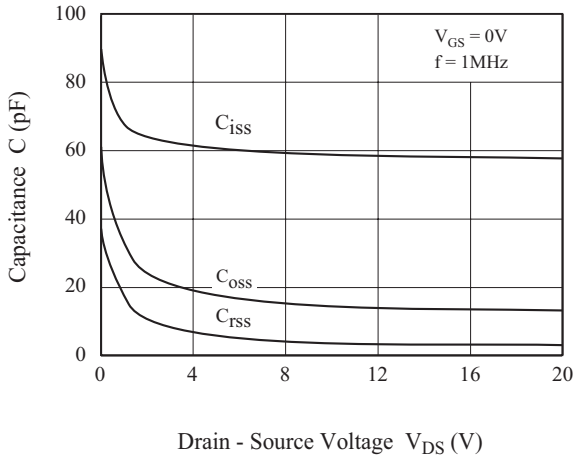
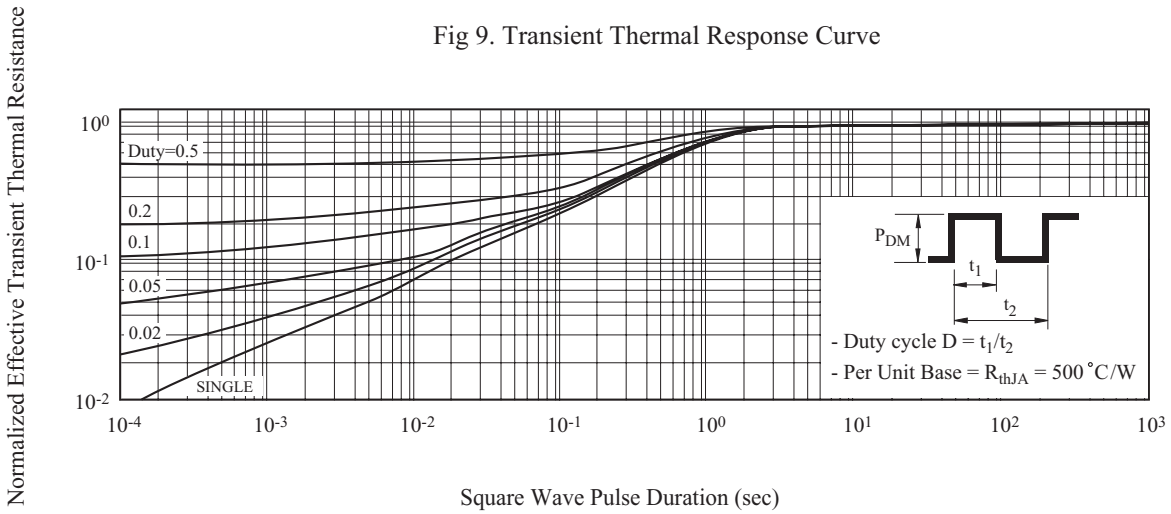


Fig 9. Transient Thermal Response Curve



P-Channel

Fig 1. I_D - V_{DS}

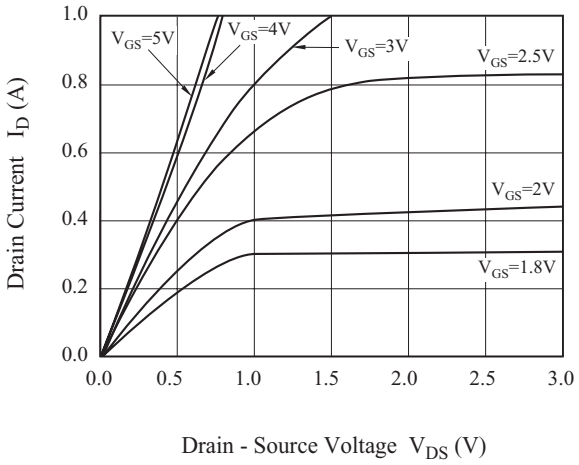


Fig 2. $R_{DS(on)}$ - I_D

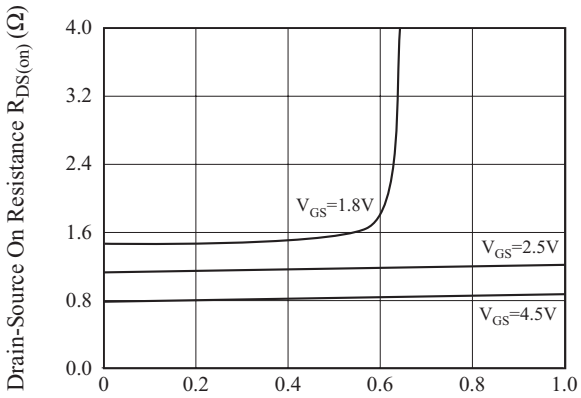


Fig 3. I_D - V_{GS}

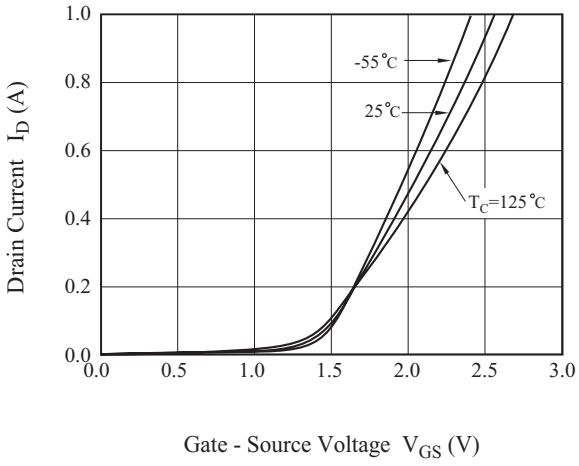


Fig 4. $R_{DS(ON)}$ - T_j

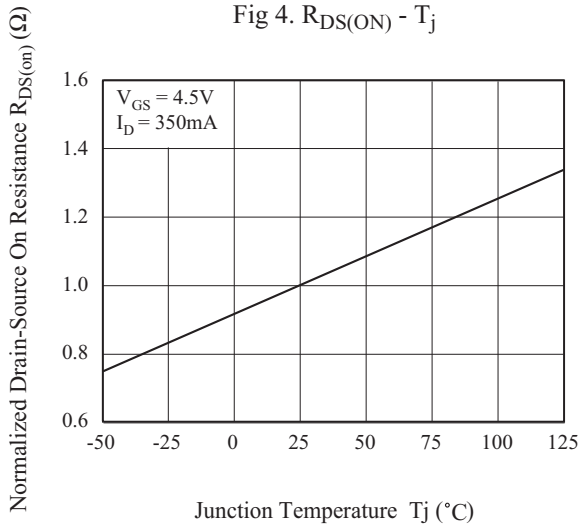


Fig 5. V_{th} - T_j

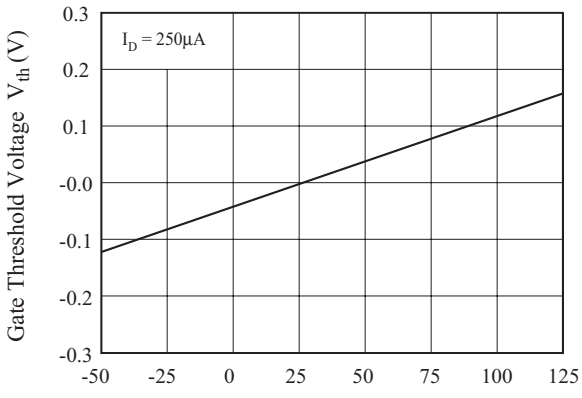


Fig 6. I_{DR} - V_{SDF}

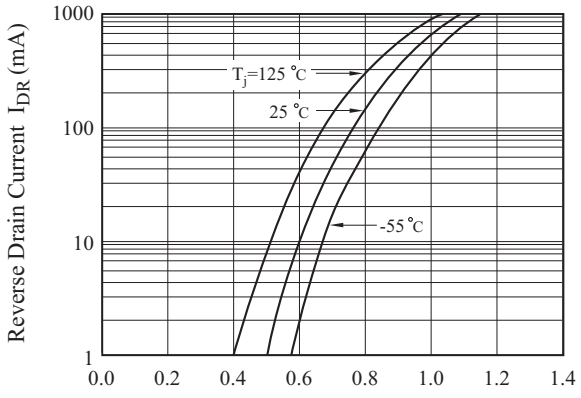


Fig 7. V_{GS} - Q_g

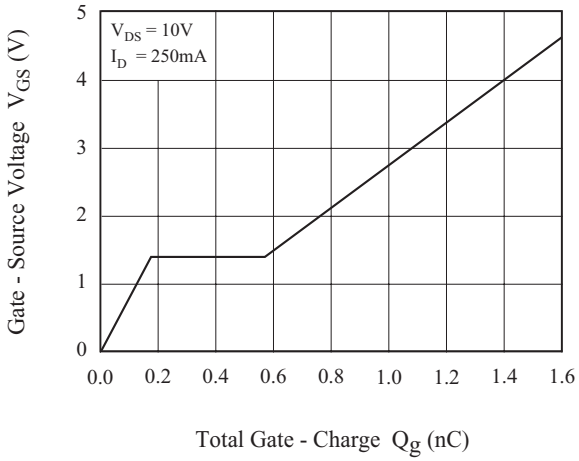
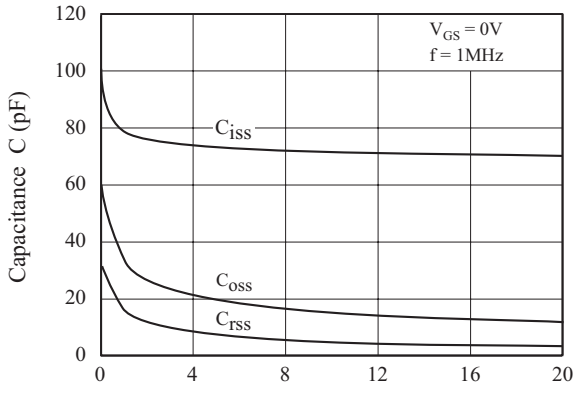


Fig 8. C - V_{DS}



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