KMN9W000RM-B205

MCP Specification

2GB e·MMC
+ 2Gb LPDDR2 S4 SDRAM

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	Initial issue. - 2GB e·MMC A-die_ Ver 0.5 - 2Gb LPDDR2 S4 SDRAM D-die_ Ver 1.4	Mar. 25, 2013	Preliminary	K.N.Kang
1.0	<2GB e·MMC A-die>_Ver 0.6 1. Entering Time for APS Mode is changed to 6ms in Table 25 . - Final datasheet.	Apr. 12, 2013	Final	K.N.Kang

1. FEATURES

<Common>
- Operating Temperature : -25°C ~ 85°C
- Package : 162ball FBGA Type - 11.5 x 13 x 1.0mmt, 0.5mm pitch

<e·MMC>
- embedded MultiMediaCard System Specification Ver. 4.41 compatible. Detail description is referenced by JEDEC Standard
- SAMSUNG e·MMC supports below special features which are defined in JEDEC

- High Priority Interrupt scheme is supported
- Background operation is supported.

- Full backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-e·MMC systems)
- Data bus sidth :1bit(Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 52MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Dual Data Rate mode is supported
- Power : Interface power → VDD = VCCQm (1.70V ~ 1.95V or 2.7V ~ 3.6V) , Memory power → VDDF = VCCm (2.7V ~ 3.6V)

<LPDDR2>
- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS, $\overline{DQS}$), These are transmitted/ received with data to be used in capturing data at the receiver
- Differential clock inputs (CK and $\overline{CK}$)
- Differential data strobes (DQS and $\overline{DQS}$)
- Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 4 (default), 8 or 16
- Burst Type: Sequential or Interleave
- Read & Write latency : Refer to Figure 47 LPDDR2 AC Timing Table
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- HSUL_12 compatible inputs
- VDD1/VDD2/VDDQ/VDDCA
  : 1.8V/1.2V/1.2V/1.2V
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, center aligned data input
- Auto refresh duty cycle : 3.9us

Items		2Gb
Device Type		S4
Number of Banks		8
Bank Addresses		BA0-BA2
t_{REFI}(us)*2		3.9
x32	Row Addresses	R0-R13
	Column Addresses*1	C0-C8

2. GENERAL DESCRIPTION

The KMN9W000RM is a Multi Chip Package Memory which combines 2GB e·MMC and 2Gbit LPDDR2 S4 SDRAM.

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.41 which is a industry standard.
e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.
There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

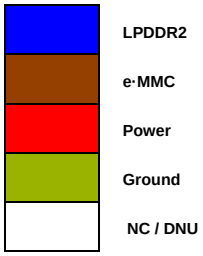
Prior to normal operation, the LPDDR2 must be initialized.

The KMN9W000RM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 162-ball FBGA Type.

3. PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	DAT0m	DAT6m	VDDIm	DAT5m	DAT3m	VCCm	DNU	DNU
B	DNU	VCCm	DAT1m	DAT7m	CLKm	DAT4m	DAT2m	VCCQm	VSSm	DNU
C	RSTm	NC	VSSQm	NC	CMDm	NC				
D	NC	NC	NC	NC	NC	NC				
E	VSSm	NC	NC		VDD2e	VDD1e	DQ31e	DQ29e	DQ26e	DNU
F	VDD1e	VSSe	NC		VSSe	VSSQe	VDDQe	DQ25e	VSSQe	VDDQe
G	VSSe	VDD2e	ZQe		VDDQe	DQ30e	DQ27e	DQS3e	$\overline{\text{DQS}}$3e	VSSQe
H	VSSCAe	CA9e	CA8e		DQ28e	DQ24e	DM3e	DQ15e	VDDQe	VSSQe
J	VDDCAe	CA6e	CA7e		VSSQe	DQ11e	DQ13e	DQ14e	DQ12e	VDDQe
K	VDD2e	CA5e	Vref(CA)e		$\overline{\text{DQS}}$1e	DQS1e	DQ10e	DQ9e	DQ8e	VSSQe
L	VDDCAe	VSSe	$\overline{\text{CK}}$e		DM1e	VDDQe				
M	VSSCAe	NC	CKe		VSSQe	VDDQe	VDD2e	VSSe	Vref(DQ)e	
N	CKEe	NC	NC		DM0e	VDDQe				
P	/CSe	NC	NC		$\overline{\text{DQS}}$0e	DQS0e	DQ5e	DQ6e	DQ7e	VSSQe
R	CA4e	CA3e	CA2e		VSSQe	DQ4e	DQ2e	DQ1e	DQ3e	VDDQe
T	VSSCAe	VDDCAe	CA1e		DQ19e	DQ23e	DM2e	DQ0e	VDDQe	VSSQe
U	VSSe	VDD2e	CA0e		VDDQe	DQ17e	DQ20e	DQS2e	$\overline{\text{DQS}}$2e	VSSQe
V	VDD1e	VSSe	NC		VSSe	VSSQe	VDDQe	DQ22e	VSSQe	VDDQe
W	DNU	NC	NC		VDD2e	VDD1e	DQ16e	DQ18e	DQ21e	DNU
Y	DNU	DNU							DNU	DNU

162FBGA: Top View (Ball Down)



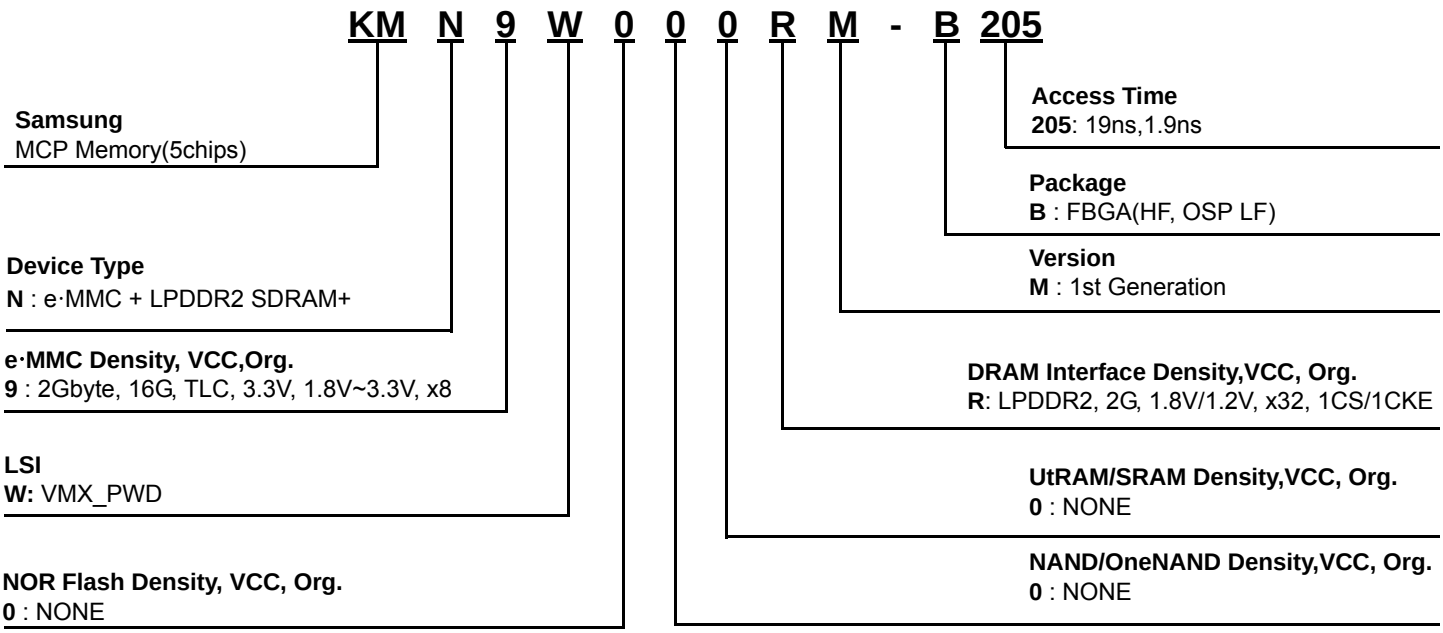
4. PIN DESCRIPTION

Pin Name	Pin Function (e·MMC)
DAT0m ~ DAT7m	Data Input/Output
CLKm	Clock
CMDm	Command
VCCm	Power Supply for Flash
VCCQm	Power Supply for Controller
VDDIm	External capacitance for Internal power stability
VSSm	Ground for Controller/Flash
VSSQm	I/O Ground
RSTm	Reset

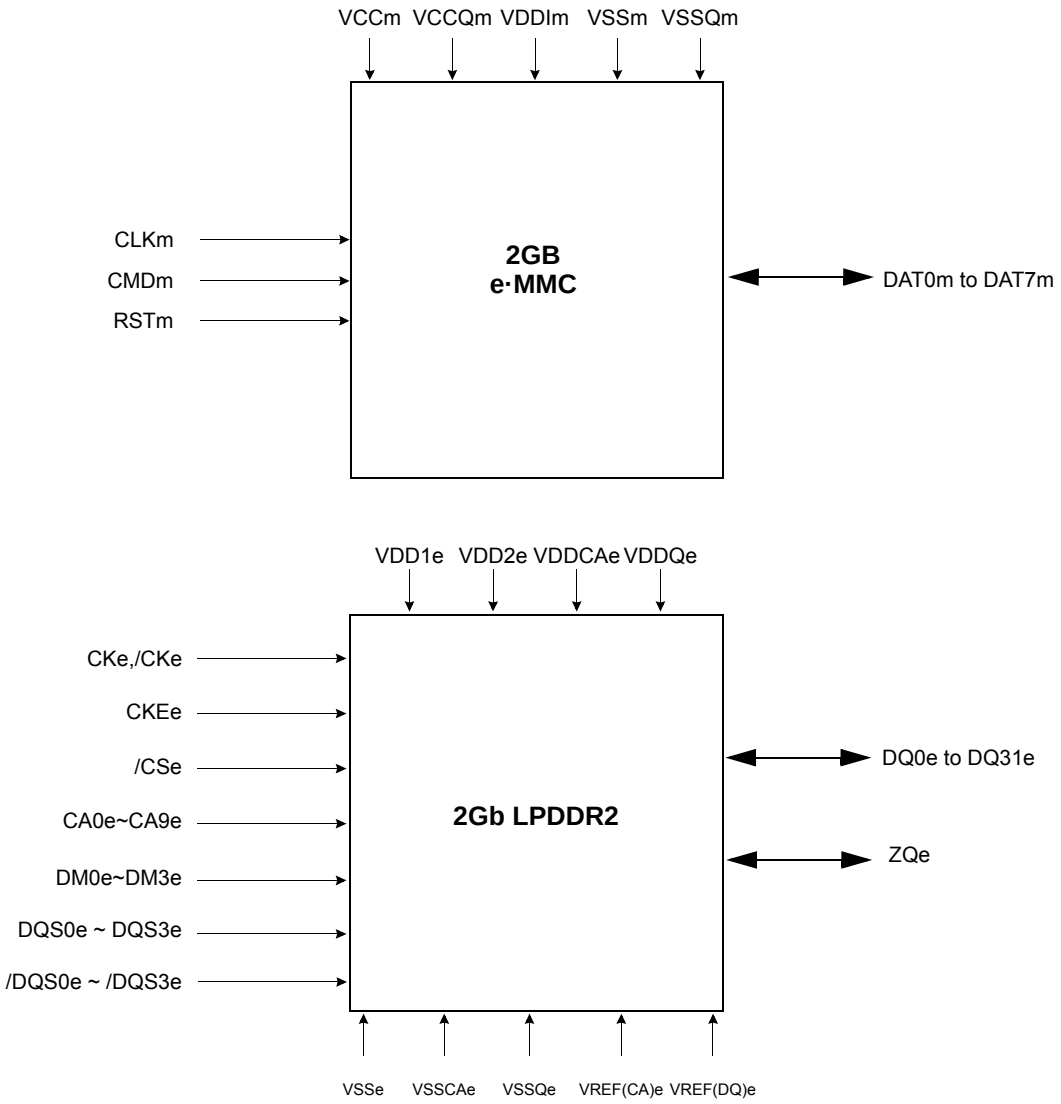
Pin Name	Pin Function
NC	No Connection
DNU	Do Not Use

Pin Name	Pin Function (LPDDR2)
CKe, $\overline{CK}$e	System Differential Clock
CKEe	Clock Enable
$\overline{CS}$e	Chip Selection
CA0e ~ CA9e	Command / Address Inputs
DM0e ~ DM3e	Input Data Mask
DQS0e ~ DQS3e	Data Strobe Bi-directional
$\overline{DQS}$0e ~ $\overline{DQS}$3e	Data Strobe Complementary
DQ0e ~ DQ31e	Data Inputs / Output
VDD1e	Core Power Supply 1
VDD2e	Core Power Supply 2
VDDCAe	Input Receiver Power Supply
VDDQe	I/O Power Supply
VREF(CA)e	Reference Voltage for CA Input Receiver
VREF(DQ)e	Reference Voltage for DQ Input Receiver
VSSe	Ground
VSSCAe	Ground for CA Input Receivers
VSSQe	I/O Ground
ZQe	Reference Pin for Output Drive Strength Calibration

5. ORDERING INFORMATION



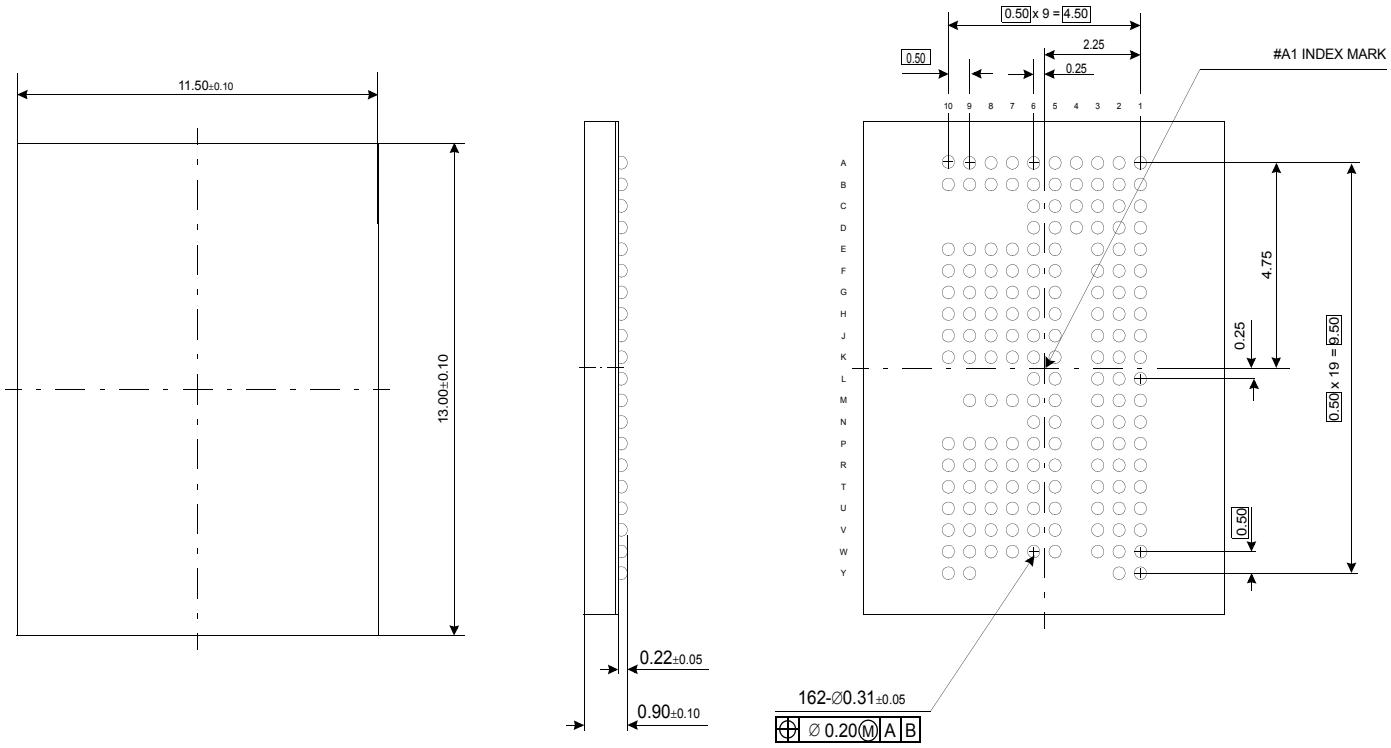
6. FUNCTIONAL BLOCK DIAGRAM



7. PACKAGE DIMENSION

162-Ball Fine pitch Ball Grid Array Package (measured in millimeters)

Units:millimeters/Inches



TOP VIEW

BOTTOM VIEW

2GB e·MMC

1.0 Product Architecture

- e·MMC consists of NAND Flash and Controller. VDD is for Controller power and VDDF is for flash power

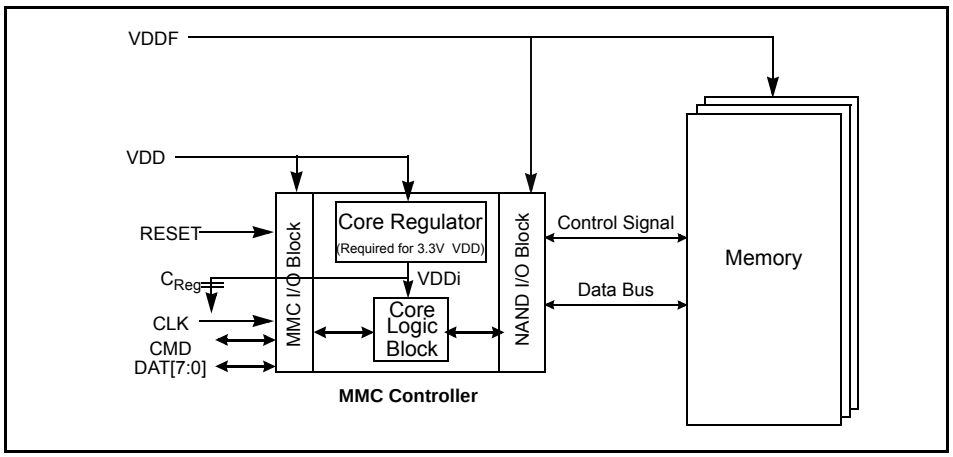


Figure 1. e·MMC Block Diagram

2.0 e.MMC 4.41 features

2.1 Data Write

Host can configure reliability mode to protect existing data per each partition.

This relibility mode has to be set before partitioning is completed.

This reliability setting only impacts the reliability of the main user area and the general purpose partitions.

[Table 1] EXT_CSD value for reliability setting in write operation

Name	Field	Size (Bytes)	Cell Type	EXT_CSD-slice	Value
Data Reliability Configuration	WR_REL_SET	1	R/W	[167]	0x1F
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Explanation of each field in the upper table is mentioned below

[Table 2] Definition of EXT_CSD value for reliability setting

Fields	Definitions
HS_CTRL_REL	0x0: All the WR_DATA_REL parameters in the WR_REL_SET registers are read only bits. 0x1: All the WR_DATA_REL parameters in the WR_REL_SET registers are R/W.
EN_REL_WR	0x0: The device supports the previous definition of reliable write. 0x1: The device supports the enhanced definition of reliable write

The below table shows each field for WE_REL_SET

[Table 3] Description of each field for WE_REL_SET

Name	Field	Bit	Size	Type
Write Data Reliability (user Area)	WR_DATA_REL_USR	0	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 1	WR_DATA_REL_1	1	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 2	WR_DATA_REL_2	2	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 3	WR_DATA_REL_3	3	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 4	WR_DATA_REL_4	4	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Reserved	-	7:5	-	-

2.2 Reliable Write

[Table 4] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Reliable write with EN_REL_WR is 0x1 supports atomicity of sector unit.

The block size defined by SET_BLOCKLEN (CMD16) is ignored and reliable write is executed as only 512 byte length. There is no limit on the size of the reliable write.

[Table 5] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	0x01

2.3 Secure Trim

Secure Trim operation consists of Secure Trim Step1 and Secure Trim Step2.
In Secure Trim Step 1 the host defines the range of write blocks that it would like to mark for the secure purge.

[Table 6] EXT_CSD value for secure trim

Field	Definitions	Value
SEC_TRIM_MULT	Secure Trim Step2 Timeout = 300ms x ERASE_TIMEOUT_MULT x SEC_TRIM_MULT	0x11

Area marked by Secure Trim Step1 is shown as EXT_CSD[181](ERASED_MEM_CONT) before Secure Trim Step2 is completed.

When Secure Trim Step2 is issued, if there is no data marked by Secure Trim Step1, Secure Trim Step2 does not work.

2.4 High Priority Interrupt

High Priority Interrupt is to stop ongoing operation and perform read operation with high priority

Command set for High Priority Interrupt operation is the below

[Table 7] Command List for High Priority Interrupt

CMD Index	Type	Argument	Resp	Abbreviation	Command Description
CMD12	ac	[31:16] – RCA* [15:1] – stuff bits [0] – High Priority Interrupt * *To be used only to send a High Priority Interrupt	R1b	STOP_TRANSMISSION	If High Priority Interrupt flag is set the device shall interrupt its internal operations in a well defined timing

Interruptible commands by read while write operation are the below.

[Table 8] List of Interruptible Command

Commands	Names	Notes
CMD24	WRITE SINGLE BLOCK	-
CMD25	WRITE MULTIPLE BLOCKS	-
CMD25	RELIABLE WRITE	Stopping a reliable write command with 'High Priority Interrupt' flag set turns that command into a reliable write command
CMD38	ERASE	-
	TRIM	-
	SECURE ERASE	-
	SECURE TRIM	-
CMD6	SWITCH	BACKGROUND OPERATION ONLY

[Table 9] EXT_CSD value for HPI

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
HPI features	HPI_FEATURES	1	R	[503]	0x01
Number of correctiy programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out of interrupt busytiming	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x05
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00

[Table 10] Definition of EXT_CSD value for HPI

Fields	Definitions
HPI_FEATURES	Bit 0 means HPI_SUPPORT Bit 0 = 0x0 : High Priority Interrupt mechanism not supported Bit 0 = 0x1 : High Priority Interrupt mechanism supported Bit 1 means HPI_IMPLEMENTATION 0x0 : HPI mechanism implementation based on CMD13 0x1 : HPI mechanism implementation based on CMD12
CORRECTLY_PRG_SECTOR_NUM	This field indicates how many 512B sectors were successfully programmed by the last WRITE_MULTIPLE_BLOCK command (CMD25). CORRECTLY_PRG_SECTORS_NUM=EXT_CSD[242]*2^0+EXT_CSD[243]*2^8 +EXT_CSD[244]*2^16 + EXT_CSD[245]*2^24
PARTITION_SWITCH_TIME	This field indicates the maximum timeout for the SWITCH command (CMD6) when switching partitions by changing PARTITION_ACCESS bits in PARTITION_CONFIG field (EXT_CSD byte [179]). Time is expressed in units of 10 milliseconds
OUT_OF_INTERRUPT_TIME	This field indicates the maximum timeout to close a command interrupted by HPI - time between the end bit of CMD12 / CMD 13 to the DAT0 release by the device.
HPI_MGMT	Bit 0 means HPI_EN 0x0 : HPI mechanism not activated by the host 0x1 : HPI mechanism activated by the host

2.5 Background Operation

When the host is not being serviced, e·MMC can do internal operation by using “Background Operation” command. In this operation which takes long time to complete can be handled later when host ensure enough idle time (In Back ground operation)

Background Operation Sequence is the following

[Table 11] Background Operation Sequence

Function	Command	Description
Background Operation Check	CMD8 Or Card Status Register	If BKOPS_STATUS is not 0 or 6th bit of card status register is set, there are something to be performed by background operation
Background Operation Start	CMD6	Background operation starts by BKOPS_START is set to any value. When background operation is completed BKOPS_STATUS is set to 0 and BKOPS_START is set to 0.
Background Operation Stop	HPI	If the background operation is stopped BKOPS_START is set to 0

[Table 12] EXT_CSD value for Background Operation

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
Background operations Support	BKOPS_SUPPORT	1	R	[502]	0x01
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations hand shake	BKOP_EN	1	R/W	[163]	0x00

[Table 13] Definition of EXT_CSD value for Bakgrourd Operation

Fields	Definitions
BKOPS_SUPPORT	‘0’ means Background operation is not supported ‘1’ means Background operation is supported
BKOPS_ STATUS	‘0’ means No background work pending ‘1’ means pending background work existing. ‘2’ means pending background work existing & performance being impacted. ‘3’ means pending background work existing & critical
BKOPS_START	Background operation start while BKOPS_START is set to any value. ‘0’ means Background operation is enabled.
BKOPS_EN	‘0’ means host does not support background operation ‘1’ means host use background operation manually

[Table 14] Card Status Register for Background Operation

Bits	Identifier	Type	Det Mode	Value	Description	Clear Cond
6	URGENT_BKOPS	S	R	“0” = Not Urgent “1” = Urgent	If set, device needs to perform background operations urgently. Host can check EXT_CSD field BKOPS_STATUS for the detailed level (in case of BKOPS_STATUS is 2 or 3)	A

3.0 Technical Notes

3.1 S/W Agorithm

3.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

3.1.1.1 Boot Area Partition and RPMB Area Partition

Boot Partition size & RPMB Partition Size are set by the following command sequence :

[Table 15] Setting sequence of Boot Area Partition size and RPMB Area Partition size

Function	Command	Description
Partition Size Change Mode	CMD62(0xEFAC62EC)	Enter the Partition Size Change Mode
Partition Size Set Mode	CMD62(0x00CBAEA7)	Partition Size setting mode
Set Boot Partition Size	CMD62(BOOT_SIZE_MULTI)	Boot Partition Size value
Set RPMB Partition Size	CMD62(RPMB_SIZE_MULTI)	RPMB Partition Size value F/W Re-Partition is executed in this step.
Power Cycle		

Boot partition size is calculated as (128KB * BOOT_SIZE_MULTI)
The size of Boot Area Partition 1 and 2 can not be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULTI).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

[Table 16] REL_WR_SEC_C value for write operation on RPMB partition

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is ‘0x00’.

3.1.1.2 Enhanced Partition (Area)

SAMSUNG e·MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies triple size of original set up size. (ex> if master set 1MB for enhanced mode, total 3MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

3.1.2 Write protect management

In order to allow the host to protect data against erase or write, the device shall support write protect commands.

3.1.2.1 User Area Write Protection

TMP_WRITE_PROTECT (CSD[12]) and PERM_WRITE_PROTECT(CSD[13]) registers allow the host to apply write protection to whole device including Boot Partition, RPMB Partition and User Area.

[Table 17] whole device write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

USER_WP (EXT_CSD[171]) register allows the host to apply write protection to all the partitions in the user area.

[Table 18] User area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

The host has the ability to check the write protection status of segments by using the SEND_WRITE_PROT_TYPE command (CMD31). When full card protection is enabled all the segments will be shown as having permanent protection.

3.1.2.2 Boot Partition Write Protection

BOOT_WP (EXT_CSD [173]) register allows the host to apply write protection to Boot Area Partitions.

[Table 19] Boot area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset

An attempt to set both the disable and enable bit for a given protection mode (permanent or power-on) in a single switch command will have no impact and switch error occurs.
Setting both B_PERM_WP_EN and B_PWR_WP_EN will result in the boot area being permanently protected.

3.1.3 Boot operation

Device supports not only boot mode but also alternative boot mode.
Device supports high speed timing and dual data rate during boot

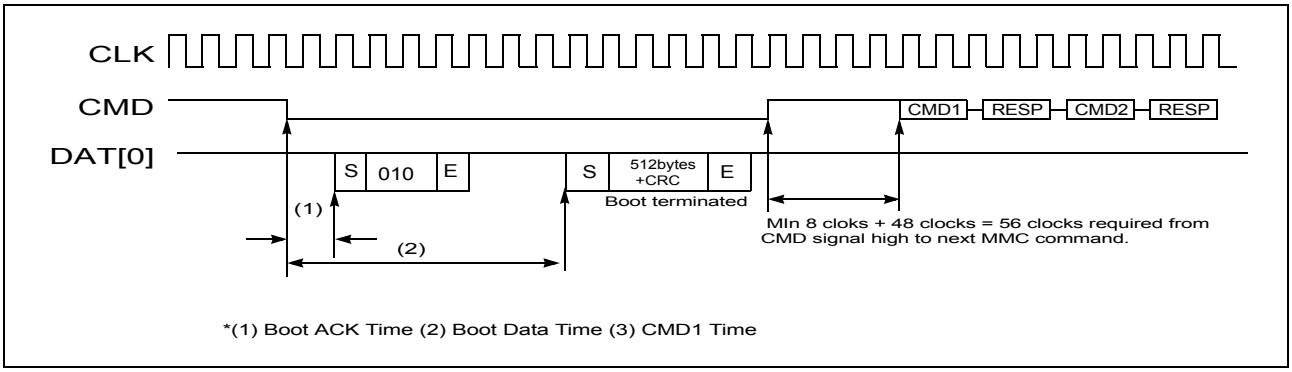


Figure 2. MultiMediaCard state diagram (boot mode)

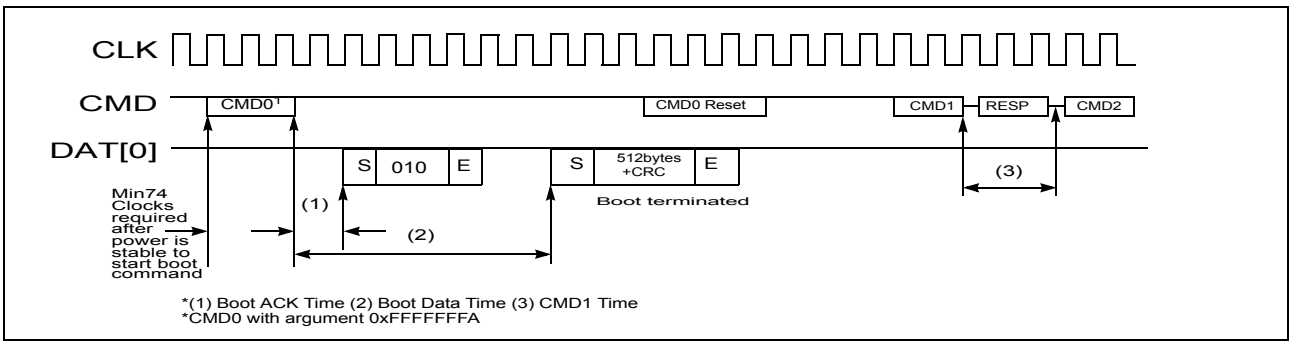


Figure 3. MultiMediaCard state diagram (alternative boot mode)

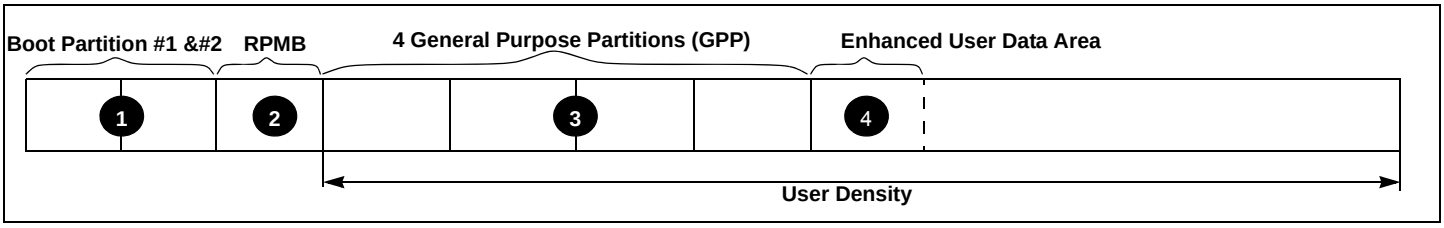
[Table 20] Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 100 ms
(3) Initialization Time[1)]	< 3 secs

NOTE:
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 5.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 140ms

3.1.4 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 96MB in TLC.
This results in decreasing of user density



[Table 21] Capacity according to partition

	Boot partition 1	Boot partition 2	RPMB
Min.	2,048KB	2,048KB	128KB
Max.	4,096KB	4,096KB	4,096KB

[Table 22] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
2 GB	620,756,992 Bytes

[Table 23] User Density Size

Device	User Density Size
2 GB	1,879,048,192 Bytes

3.1.5 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

[Table 24] Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 25] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
GotoSleep Time	< 6 ms	< 1ms

3.1.6 Performance

[Table 26] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
2 GB	70	6

* Test/ Estimation Condition : Bus width x8, 52MHz DDR, 512KB data transfer, w/o file system overhead

4.0 REGISTER VALUE

4.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by all e·MMCs.

[Table 27] OCR Register

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode)
[31]	e·MMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the e·MMC has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

4.2 CID Register

[Table 28] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	---[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	---[2]
Product serial number	PSN	32	[47:16]	---[3]
Manufacturing date	MDT	8	[15:8]	---[4]
CRC7 checksum	CRC	7	[7:1]	---[5]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as e.MMC JEDEC standard
2) PRV is composed of the revision count of controller and the revision count of F/W patch
3) 32-bit unsigned binary integer. (Random Number)

4.2.1 Product name table (In CID Register)

[Table 29] Product name

Part Number	Density	Product Name in CID Register (PNM)
KMN9W000RM-B205	2 GB	0x4E3957524D42

4.3 CSD Register

The Card-Specific Data register provides information on how to access the e·MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 30] CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value
					2GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x0A
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	-	2	R	[75:74]	-
Card size	C_SIZE	12	R	[73:62]	0xDFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06
Card size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	-
Not used, always '1'	-	1	-	[0:0]	-

4.4 Extended CSD Register

The Extended CSD register defines the e·MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e·MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e·MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 31] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value
					2GB
Properties Segment					
Reserved[1]		7	-	[511:505]	-
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Reserved[1]		8	-	[501:494]	-
Firmware Update Support	FW_UPDATE_SUPPORT	1	R	[493]	0x01
Reserved[1]		233	-	[492:260]	-
Device Version	DEVICE_VERSION	1	R	[259]	FW Patch Ver.
Controller Version	CTRL_VERSION	1	R	[258]	0x00
Optimal Erase Size	OPT_ERASE_SIZE	1	R	[257]	0x01
Optimal Write Size	OPT_WRITE_SIZE	1	R	[256]	0x04
Pre EOL Information	PRE_EOL_INFO	1	R	[255]	0x00
Device Lifetime Estimation Value	LIFE_TIME_EST	1	R	[254]	0x00
Firmware Update Status	FW_UPDATE_STATUS	1	R	[253]	0x00
Reserved[1]		4	-	[252:249]	-
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
I st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Reserved[1]		1	-	[240]	-
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Reserved[1]		2	-	[237:236]	-
Minimum Write Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved[1]		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x15
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11

Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved[1]		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x10
Access size	ACC_SIZE	1	R	[225]	0x06
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (VDDF)	S_C_VDDF	1	R	[220]	0x07
Sleep current (VDD)	S_C_VDD	1	R	[219]	0x07
Reserved[1]		1	-	[218]	-
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Reserved[1]		1	-	[216]	-
Sector Count	SEC_COUNT	4	R	[215:212]	0x00
Reserved[1]		1	-	[211]	-
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved[1]		1	-	[204]	-
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	0x00
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	0x00
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	0x00
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x05
Reserved[1]		1	-	[197]	-
Card Type	CARD_TYPE	1	R	[196]	0x07
Reserved[1]		1	-	[195]	-
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved[1]		1	-	[193]	-
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x05
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved[1]		1	-	[190]	-
Command Set Revision	CMD_SET_REV	1	R	[189]	0x00
Reserved[1]		1	-	[188]	-
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved[1]		1	-	[186]	-
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved[1]		1	-	[184]	-
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved[1]		1	-	[182]	-
Erased Memory Content	ERASED_MEM_CONT	1	R	[181]	0x00

Reserved[1]		1	-	[180]	-
Partition configurationn	PARTITION_CONFIG	1	R/W/E& R/W/E_P	[179]	0x00
Boot config proteetion	BOOT_CONFIG_PRPT	1	R/W & R/W/C_P	[178]	0x00
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	0x00
Reserved[1]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Reserved[1]		1	-	[174]	-
Boot area write proection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved[1]		1	-	[172]	-
User area write protection register	USER_WP	1	R/W, R/W/C_P& R/W/E_P	[171]	0x00
Reserved[1]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x01
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x05
Reserved[1]		1	-	[165]	-
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitoning support	RARTITIONING_SUPPORT	1	R	[160]	0x03
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x4A
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Paritioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved[1]		1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMT	1	R/W	[134]	0x00
Firmware Update Mode	FW_UPDATE_MODE	1	W/E_P	[133]	0x00
Reserved[1]		64	-	[132:69]	-
High Performance Mode Configuration	HIGH_PERF_CONFIG	1	R/W/E_P	[68]	0x00
Vendor Config (Auto Background Operation)	AUTO_BKOPS	1	R/W/E	[67]	0x00
Vendor Config (Aligned Optimal Trim/Discard Size)	ALIGNED_OPTIMAL_TRIM_ DISCARD_SIZE	1	R	[66]	0x04
Vendor Config (Optimized Features)	OPTIMIZED_FEATURES	2	R	[65:64]	0x03
Reserved[1]		29	-	[63:35]	-
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Reserved[1]		34	-	[33:0]	-

NOTE :
1) Reserved bits should be read as "0."

5.0 AC PARAMETER

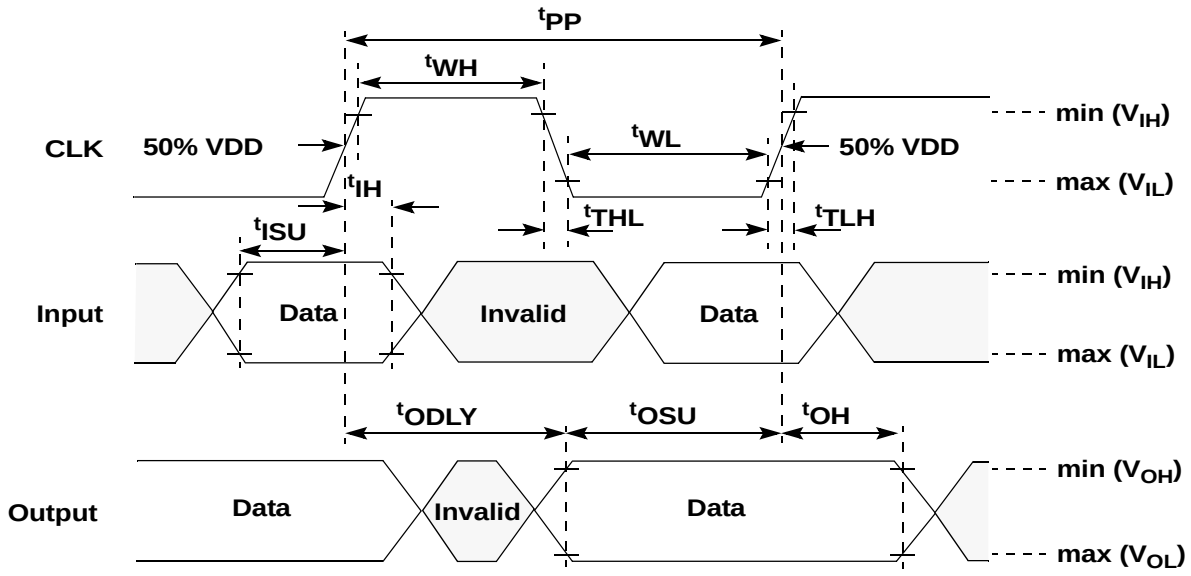
5.1 Time Parameter

[Table 32] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal 1)	140	ms
	After partition setting 2)	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		15	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		1	ms
Power Off Notification (Short) Timeout		100	ms
Power Off Notification (Long) Timeout		600	ms

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 5.4 EXT_CSD register

5.2 Bus Timing Parameter



Data must always be sampled on the rising edge of the clock.

Figure 4. Bus signal levels

[Table 33] Default (under 26MHz)

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[2]					
Clock frequency Data Transfer Mode3	fPP	0[4]	26	MHz	CL <= 30 pF
Clock frequency Identification Mode	f_{OD}	0[4]	400	kHz	
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock high time	t_{WH}	10			C_L <= 30 pF
Clock rise time[5]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF

NOTE :
1) Device must always start with the backward-compatible interface timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VDD.
3) For compatibility with cards that suport the v4.2 standard or earlier verison, host should not use>26MHz before switching to high-speed interface timing.
4) Frequency is periodically sampled and is not 100% tested.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

[Table 34] High-Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[1]					
Clock frequency Data Transfer Mode[2]	f_{PP}	0[3]	52[4)]	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode	f_{OD}	0[3]	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock High time	t_{WH}	6.5		ns	C_L <= 30 pF
Clock rise time[5]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	CL <= 30 pF
Output hold time	t_{OH}	2.5			C_L <= 30 pF
Signal rise time	t_{RISE}		3	ns	C_L <= 30 pF
Signal fall time	t_{FALL}		3	ns	C_L <= 30 pF

NOTE :
1) CLK timing is measured at 50% of VDD.
2) A MultiMediaCard shall support the full frequency range from 0-26MHz, or 0-52MHz
3) Frequency is periodically sampled and is not 100% tested.
4) Device can operate as high-speed card interface timing at 26MHz clock frequency.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).6) Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

5.3 Bus timing for DAT signals during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK.The CMD signal still operates synchronously of the rising edge of CLK and there fore it complies with the bus timing specified in chapter 7.2, Therefore there is no timing change for the CMD signal

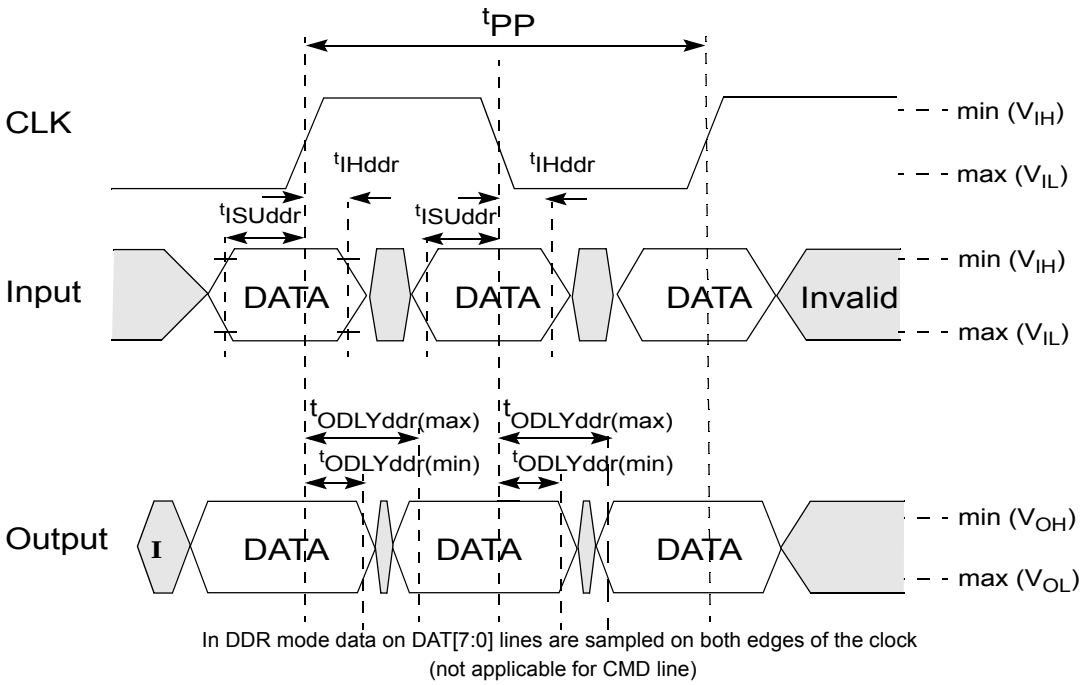


Figure 5. Timing diagram: data input/output in dual data rate mode

5.3.1 Dual data rate interface timings

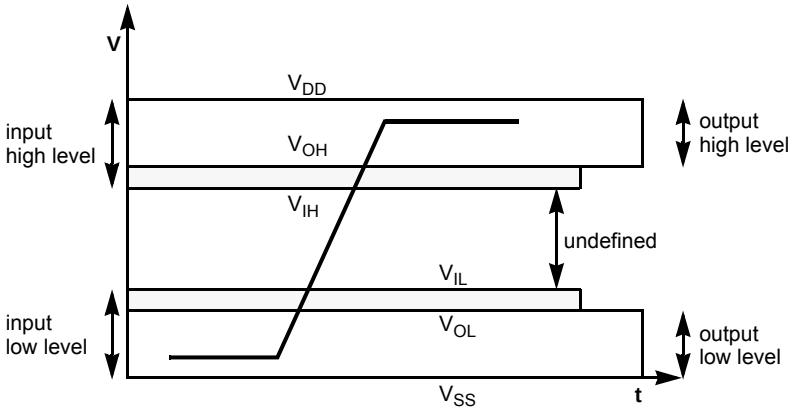
[Table 35] High-speed dual rate interface timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

NOTE :
1) CLK timing is measuted at 50% of VDD
2) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max(V_{IL}), and outputs CMD,DATrise and fall times measured by min(V_{OH}) and max(V_{OL})

5.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



5.4.1 Open-drain mode bus signal level

[Table 36] Open-drain bus signal level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2		V	Note 1)
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

Note:

1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.

The input levels are identical with the push-pull mode bus signal levels.

5.4.2 Push-pull mode bus signal level eMMC

The device input and output voltages shall be within following specified ranges for any V_{DD} of the allowed voltage range.

[Table 37] Push-pull signal level— high-voltage eMMC

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -100 uA@V_{DD} min
Output LOW voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100 uA@V_{DD} min
Input HIGH voltage	V_{IH}	0.625*V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{DD}	V	

[Table 38] Push-pull signal level— 1.70-1.95 V_{CCQ} voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.45V		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{DD} 1)	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{DD} 2)	V	

NOTE:

1) 0.7*V_{DD} for MMC4.3 and older revisions.

2) 0.3*V_{DD} for MMC4.3 and older revisions.

6.0 DC PARAMETER

6.1 Active Power Consumption during operation

[Table 39] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
2 GB	16Gb x 1	150	80	mA

* Power Measurement conditions: Bus configuration =x8 @52MHz DDR
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

6.2 Standby Power Consumption in auto power saving mode and standby state

[Table 40] Standby Power Consumption in auto power saving mode and standby state

Density	NAND Type	CTRL		NAND		Unit
		25°C(Typ)	85°C	25°C(Typ)	85°C	
2 GB	16Gb x 1	120	400	40	85	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
*Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

6.3 Sleep Power Consumption in Sleep State

[Table 41] Sleep Power Consumption in Sleep State

Density	NAND Type	CTRL		NAND	Unit
		25°C(Typ)	85°C		
2 GB	16Gb x 1	120	400	0[1)]	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
1) In auto power saving mode , NAND power can not be turned off .However in sleep mode NAND power can be turned off. If NAND power is alive , NAND power is same with that of the Standby state.

6.4 Supply Voltage

[Table 42] Supply Voltage

Item	Min	Max	Unit
VDD	1.70 (2.7)	1.95 (3.6)	V
VDDF	2.7	3.6	V
Vss	-0.5	0.5	V

6.5 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 43] Bus Signal Line Load

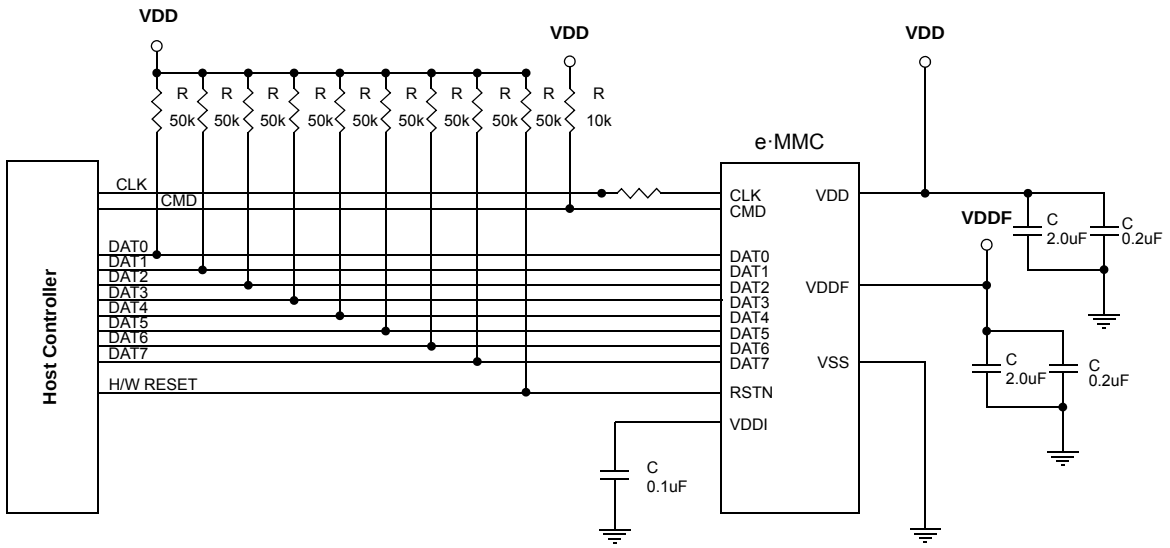
Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single e·MMC capacitance	C_{BGA}			12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

A. e·MMC Connection Guide

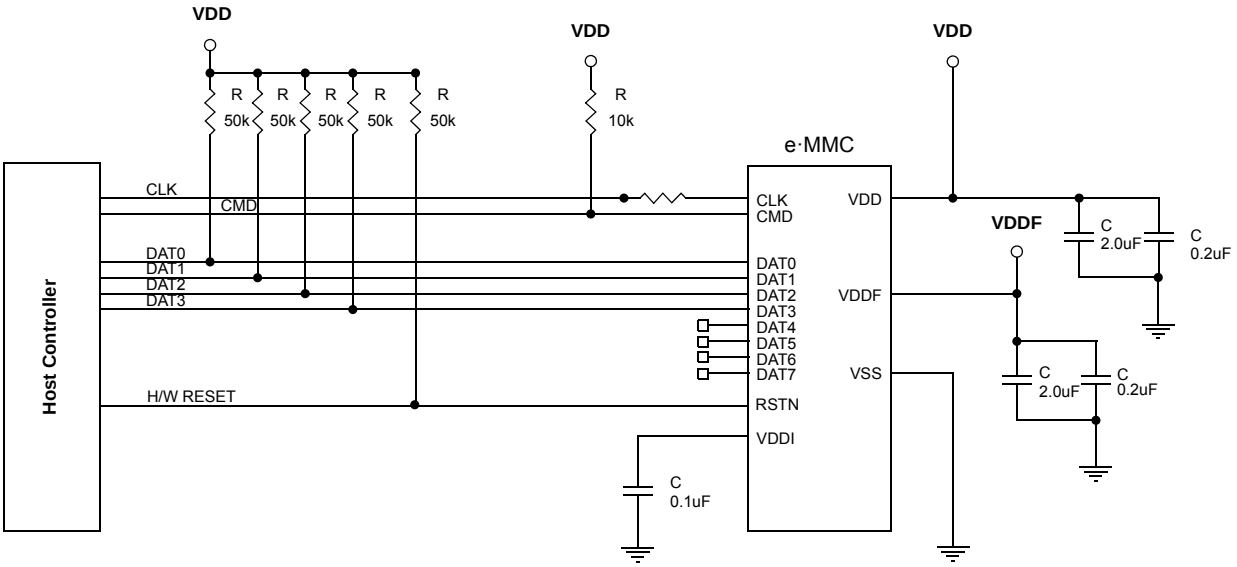
This connection guide is an example for customers to adopt e·MMC more easily

- This appendix is just guideline for e·MMC connection. This value and schematic can be changed depending on the system environment.
- Coupling capacitor should be connected with VDD and VSS as close as possible.
- VDDI Capacitor is min 0.1uF
- Impedance on CLK match is needed.
- 0Ω ~47Ω is available for resistance on CLK line according to a system environment.
- If host does not have a plan to use H/W reset, it is not needed to put 50KΩ pull-up resistance on H/W reset line.
- SAMSUNG recommends user separate VDD and VDDF power.

A.1 x8 support Host connection Guide



A.2 x4 support Host connection Guide



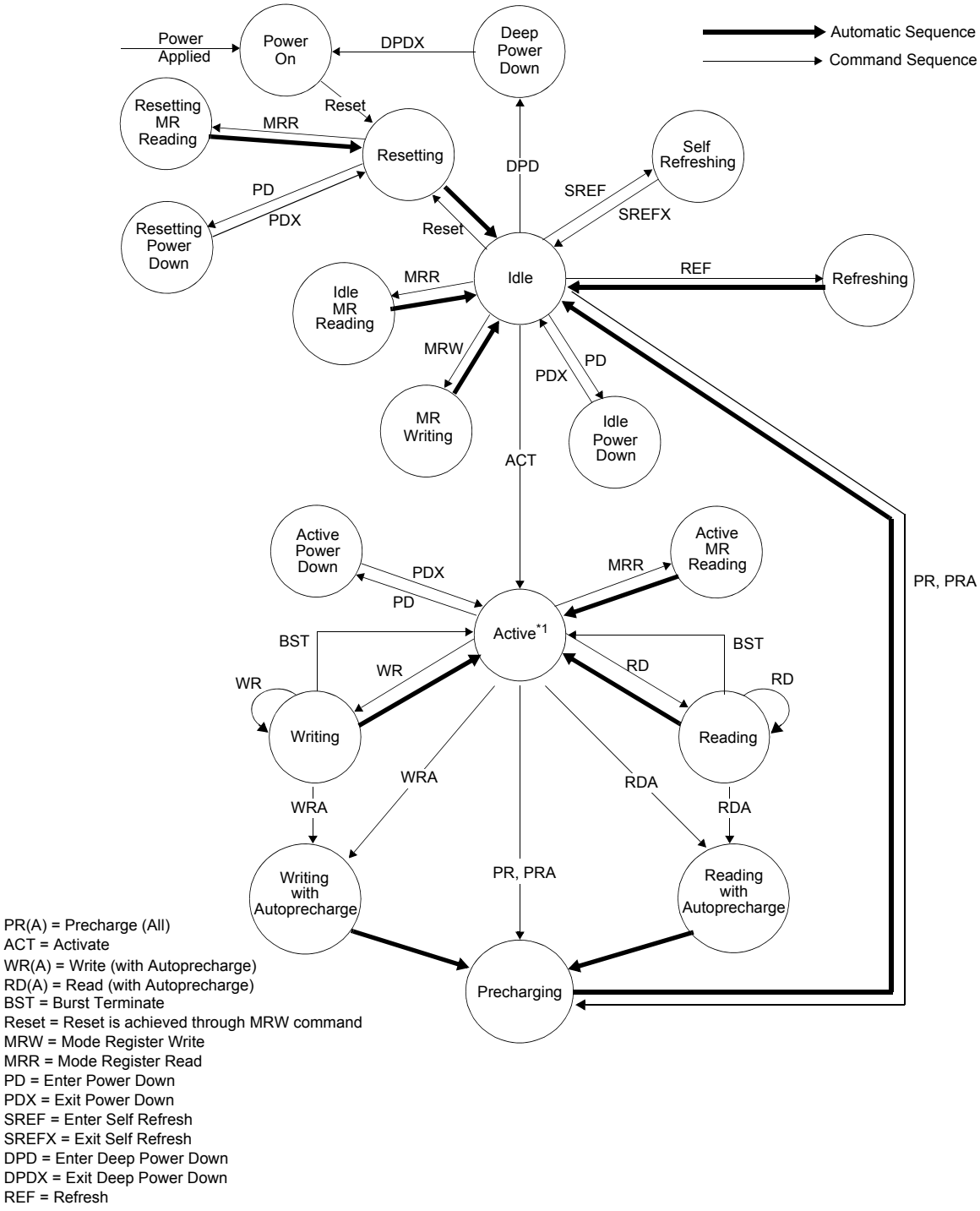
2Gb LPDDR2 S4 SDRAM

1.0 Simplified LPDDR2-S4 State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].



PR(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
BST = Burst Terminate
Reset = Reset is achieved through MRW command
MRW = Mode Register Write
MRR = Mode Register Read
PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
DPD = Enter Deep Power Down
DPDX = Exit Deep Power Down
REF = Refresh

Figure 1. LPDDR2-S4: Simplified Bus Interface State Diagram

NOTE :
1) For LPDDR2-SDRAM in the Idle state, all banks are precharged.

1.1 Mode Register Definition

1.1.1 Mode Register Assignment and Definition in LPDDR2 SDRAM

Table 1 shows the 16 common mode registers for LPDDR2 SDRAM and NVM. Table 2 shows only LPDDR2 SDRAM mode registers and Table 3 shows only LPDDR2 NVM mode registers. Additionally Table 4 shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

[Table 1] Mode Register Assignment in LPDDR2 SDRAM (Common part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01_H	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature 2	W	(RFU)					RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11:15	$0B_H$~$0F_H$	(reserved)		(RFU)							

[Table 2] Mode Register Assignment in LPDDR2 SDRAM (SDRAM part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_Bank	W	Bank Mask							
17	11_H	PASR_Seg	W	Segment Mask							
18-19	12_H-13_H	(Reserved)		(RFU)							

[Table 3] Mode Register Assignment in LPDDR2 SDRAM (NVM Part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20:31	14_H~$1F_H$	(Do Not Use)									

[Table 4] Mode Register Assignment in LPDDR2 SDRAM (DQ Calibration and Reset Command)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	**20_H**	DQ Calibration Pattern A	R	See "DQ Calibration" on Operations & Timing Diagram.							
33:39	**21_H~27_H**	(Do Not Use)									
40	**28_H**	DQ Calibration Pattern B	R	See "DQ Calibration" on Operations & Timing Diagram.							
41:47	**29_H~$2F_H$**	(Do Not Use)									
48:62	**30_H~$3E_H$**	(Reserved)		(RFU)							
63	**$3F_H$**	Reset	W	X							
64:126	**40_H~$7E_H$**	(Reserved)		(RFU)							
127	**$7F_H$**	(Do Not Use)									
128:190	**80_H~BE_H**	(Reserved for Vendor Use)		(RFU)							
191	**BF_H**	(Do Not Use)									
192:254	**$C0_H$~FE_H**	(Reserved for Vendor Use)		(RFU)							
255	**FF_H**	(Do Not Use)									

The following notes apply to Table 1, Table 2, Table 3, and Table 4:

NOTE :
1) RFU bits shall be set to '0' during Mode Register writes.
2) RFU bits shall be read as '0' during Mode Register reads.
3) All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, $\overline{DQS}$ shall be toggled.
4) All Mode Registers that are specified as RFU shall not be written.
5) Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		(RFU)	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP<0>	0_B: DAI complete 1_B: DAI still in progress
DI (Device Information)	Read-only	OP<1>	0_B: S4 SDRAM 1_B: Do Not Use
RZQI (Built in Self Test for RZQ Information) 1)	Read-only	OP4:OP3	00_B: RZQ self test not supported 01_B: ZQ-pin may connect to VDDCA or float 10_B: ZQ-pin may short to GND 11_B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

NOTE :
1) RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2) If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3] = 01 or OP[4:3] =10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3) In the case of possible assembly error (either OP[4:3]=01 per Note 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4) In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-ohm +/- 1%).

MR1_Device Feature 1 (MA<7:0> = 01_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	010_B: BL4 (default) 011_B: BL8 100_B: BL16 **All others:** Reserved
BT*1	Write-only	OP<3>	0_B: Sequential (default) 1_B: Interleaved
WC	Write-only	OP<4>	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
nWR*2	Write-only	OP<7:5>	001_B: nWR=3 (default) 010_B: nWR=4 011_B: nWR=5 100_B: nWR=6 101_B: nWR=7 110_B: nWR=8 **All others:** Reserved

NOTE :
1) BL 16, interleaved is not an official combination to be supported.
2) Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

[Table 5] Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		**illegal (not allowed)**															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		**illegal (not allowed)**															
X	X	X	0_B	nw	any		**illegal (not allowed)**															

NOTE :
1) C0 input is not present on CA bus. It is implied zero.
2) For BL=4, the burst address represents C1 - C0.
3) For BL=8, the burst address represents C2 - C0.
4) For BL=16, the burst address represents C3 - C0.
5) For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 6 below for the respective density and bus width combinations.

[Table 6] LPDDR2-S4 Non Wrap Restrictions

2Gb	
Not across full page boundary	
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
x32	None

NOTE :
1) Non-wrap BL=4 data-orders shown above are prohibited.

MR2_Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B:** RL3 / WL1(default) **0010_B:** RL4 / WL2 **0011_B:** RL5 / WL2 **0100_B:** RL6 / WL3 **0101_B:** RL7 / WL4 **0110_B:** RL8 / WL4 **All others:** Reserved

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** Reserved **0001_B:** 34.3-ohm typical **0010_B:** 40-ohm typical (default) **0011_B:** 48-ohm typical **0100_B:** 60-ohm typical **0101_B:** Reserved for 68.6-ohm typical **0110_B:** 80-ohm typical **0111_B:** 120-ohm typical **All others:** Reserved

MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010_B:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011_B:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85'C) **100_B:** Reserved **101_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

NOTE :
1) A Mode Register Read from MR4 will reset OP7 to '0'.
2) OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
3) If OP2 equals '1', the device temperature is greater than 85'C.
4) OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5) LPDDR2 might not operate properly when OP[2:0] = 000_B or 111_B
6) For specified operating temperature range and maximum operating temperature refer to Table 15.
7) LPDDR2-S4 devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 45. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8) See "Temperature Sensor" on [Command Definition & Timing Diagram] for information on the recommended frequency of reading MR4.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP<7:0>	**0000 0000_B :** Reserved **0000 0001_B :** Samsung **0000 0010_B :** Do Not Use **0000 0011_B :** Do Not Use **0000 0100_B :** Do Not Use **0000 0101_B :** Do Not Use **0000 0110_B :** Do Not Use **0000 0111_B :** Do Not Use **0000 1000_B :** Do Not Use **0000 1001_B :** Do Not Use **0000 1010_B :** Reserved **0000 1011_B :** Do Not Use **0000 1100_B :** Do Not Use **0000 1101_B :** Do Not Use **0000 1110_B :** Do Not Use **0000 1111_B :** Do Not Use **1111 1110_B :** Do Not Use **All others :** Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**00000001_B:** B-version

NOTE :
1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**00000000_B:** A-version

NOTE :
1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = $08B_H$) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**00_B:** S4 SDRAM **01_B:** Reserved **10_B:** Do Not Use **11_B:** Reserved
Density	Read-only	OP<5:2>	**0000_B:** 64Mb **0001_B:** 128Mb **0010_B:** 256Mb **0011_B:** 512Mb **0100_B:** 1Gb **0101_B:** 2Gb **0110_B:** 4Gb **0111_B:** 8Gb **1000_B:** 16Gb **1001_B:** 32Gb **all others:** reserved
I/O width	Read-only	OP<7:6>	**00_B:** x32 **01_B:** x16 **10_B:** x8 **11_B:** Do Not Use

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

NOTE :
1) Host processor shall not write MR10 with “Reserved” values
2) LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3) See AC timing table for the calibration latency
4) If ZQ is connected to V_{SSCA} through R_{ZQ}, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command" on [Command Definition & Timing Diagram]) or default calibration (through the ZQreset command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5) LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
6) The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR_11:15_(Reserved) (MA<7:0> = $0B_H$-$0F_H$):

MR_16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask (4-Bank or 8-Bank)							

S4 SDRAM:

Bank <7:0> Mask 1)	Write-only	OP<7:0>	**0_B:** refresh enable to the bank (=unmasked, default) **1_B:** refresh blocked (=masked)

NOTE :
1) For 4 bank S4 SDRAM, only OP<3:0> are used.

OP	Bank Mask	4 Bank	8 Bank
0	XXXXXXX1	Bank 0	Bank 0
1	XXXXXX1X	Bank 1	Bank 1
2	XXXXX1XX	Bank 2	Bank 2
3	XXXX1XXX	Bank 3	Bank 3
4	XXX1XXXX	-	Bank 4
5	XX1XXXXX	-	Bank 5
6	X1XXXXXX	-	Bank 6
7	1XXXXXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	**0_B:** refresh enable to the segment (=unmasked, default) **1_B:** refresh blocked (=masked)

			1Gb	2Gb/4Gb	8Gb
Segment	**OP**	**Segment Mask**	**R12:10**	**R13:11**	**R14:12**
0	0	XXXXXXX1	**000_B**		
1	1	XXXXXX1X	**001_B**		
2	2	XXXXX1XX	**010_B**		
3	3	XXXX1XXX	**011_B**		
4	4	XXX1XXXX	**100_B**		
5	5	XX1XXXXX	**101_B**		
6	6	X1XXXXXX	**110_B**		
7	7	1XXXXXXX	**111_B**		

NOTE :
1) This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment

MR18-19_(Reserved) (MA<7:0> = 012_H - 013_H):

MR20-31_(Do Not Use) (MA<7:0> = 14_H-$1F_H$):

MR32_DQ Calibration Pattern A (MA<7:0>=20_H):
Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration" on Operations & Timing Diagram.

MR33:39_(Do Not Use) (MA<7:0> = 21_H-27_H):

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):
Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration" on Operations & Timing Diagram.

MR41:47_(Do Not Use) (MA<7:0> = 29_H-$2F_H$):

MR48:62_(Reserved) (MA<7:0> = 30_H-$3E_H$):

MR63_Reset (MA<7:0> = $3F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE :
1) For additional information on MRW RESET see "Mode Register Write Command" on [Command Definition & Timing Diagram].

MR64:126_(Reserved) (MA<7:0> = 40_H-$7E_H$):

MR127_(Do Not Use) (MA<7:0> = $7F_H$):

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 80_H-BE_H):

MR191_(Do Not Use) (MA<7:0> = BF_H):

MR192:254_(Reserved for Vendor Use) (MA<7:0> = $C0_H$-FE_H):

MR255:(Do Not Use) (MA<7:0> = FF_H):

2.0 TRUTH TABLES

2.1 Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

2.1.1 Command truth table

[Table 7] Command truth table

SDRAM Command	SDR Command Pins			DDR CA pins (10)										
	CKE		$\overline{CS}$	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	X								↓
Refresh (per bank)[10]	H	H	L	L	L	H	L	X						↑
				X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
				X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
				X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	X		BA0	BA1	BA2	↑
				X										↓
BST	H	H	L	H	H	L	L	X						↑
				X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
				X										↓
NOP	H	H	L	H	H	H	X							↑
				X										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
				X										↓
NOP	H	H	H	X										↑
				X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
				X										↓
Enter Power Down	H	L	H	X										↑
				X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
				X										↓

NOTE:
1) All LPDDR2 commands are defined by states of $\overline{CS}$, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2) For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3) AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4) “X” means “H or L (but a defined logic level)”
5) Self refresh exit and Deep Power Down exit are asynchronous.
6) V_{Ref} must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
7) CAxr refers to command/address bit “x” on the rising edge of clock.
8) $\underline{CA}$xf refers to command/address bit “x” on the falling edge of clock.
9) $\overline{CS}$ and CKE are sampled at the rising edge of clock.
10) Per Bank Refresh is only allowed in devices with 8 banks.
11) The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
12) AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

2.2 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

[Table 8] LPDDR2-S4 : CKE Table

Device Current State*3	CKE_{n-1}*1	CKE_n*1	$\overline{CS}$*2	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Deep Power Down	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

NOTE :

1) "CKE_n" is the logic state of CKE at clock rising edge n; "CKE_{n-1}" was the state of CKE at the previous clock edge.
2) "$\overline{CS}$" is the logic state of $\overline{CS}$ at the clock rising edge n;
3) "Current state" is the state of the LPDDR2 device immediately prior to clock edge n.
4) "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6) Power Down exit time (t_{XP}) should elapse before a command other than NOP is issued.
7) Self-Refresh exit time (t_{XSR}) should elapse before a command other than NOP is issued.
8) The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9) The clock must toggle at least once during the t_{XP} period.
10) The clock must toggle at least once during the t_{XSR} time.
11) 'X' means 'Don't care'.
12) Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

[Table 9] Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
- Idle: The bank or banks have been precharged, and tRP has been met.
- Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
- Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
- Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4) The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and Figure 9, and according to Figure 10.
- Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
- Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
- Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
- Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5) The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
- Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
- Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
- Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
- Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
- Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
- MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
- Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6) Bank-specific; requires that the bank is idle and no bursts are in progress.
7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
8) Not bank-specific reset command is achieved through Mode Register Write command.
9) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10) A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11) The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12) A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
13) Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.
14) A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
15) If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

[Table 10] Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
 - Idle: the bank has been precharged, and tRP has been met.
 - Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
 - Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4) Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5) A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6) The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
 - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
 - Resetting MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Resetting state.
 - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
 - MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
7) t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8) Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10) MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
11) MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.
12) Not bank-specific; requires that all banks are idle and no bursts are in progress.
13) The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
14) A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.
15) Read with Auto Precharge enabled and Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Precharge & Auto Precharge clarification on Timing spec are followed.
16) A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17) Reset command is achieved through Mode Register Write command.
18) BST is allowed only if a Read or Write burst is ongoing.Data mask truth table.

2.3 Data mask truth table

Table 11 provides the data mask truth table.

[Table 11] DM truth table

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

NOTE :
1) Used to mask write data, provided coincident with the corresponding data

3.0 ABSOLUTE MAXIMUM DC RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 12] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	5

NOTE :

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2) See “Power-Ramp” section in "Power-up, Initialization, and Power-Off" on [Command Definition & Timing Diagram] for relationships between power supplies.

3) $V_{RefDQ} \leq 0.6$ x VDDQ; however, V_{RefDQ} may be $\geq$ VDDQ provided that $V_{RefDQ} \leq 300$mV.

4) $V_{RefCA} \leq 0.6$ x VDDCA; however, V_{RefCA} may be $\geq$ VDDCA provided that $V_{RefCA} \leq 300$mV.

5) Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

4.0 AC & DC OPERATING CONDITIONS

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Recommended DC Operating Conditions

4.1 Recommended DC Operating Conditions

[Table 13] Recommended LPDDR2-S4 DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

NOTE :
1) VDD1 uses significantly less power than VDD2

4.2 Input Leakage Current

[Table 14] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, $\overline{CS}$, CK, $\overline{CK}$ Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	I_L	-2	2	uA	2
V_{Ref} supply leakage current V_{RefDQ} = VDDQ/2 or V_{RefCA} = VDDCA/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	1

NOTE :
1) The minimum limit requirement is for testing purposes. The leakage current on V_{RefCA} and V_{RefDQ} pins should be minimal.
2) Although DM is for input only, the DM leakage shall match the DQ and DQS/$\overline{DQS}$ output leakage specification.

4.3 Operating Temperature Range

[Table 15] Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	^oC

NOTE :
1) Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85^{o}C when the temperature sensor indicates a temperature of less than 85^{o}C.

5.0 AC AND DC INPUT MEASUREMENT LEVELS

5.1 AC and DC Logic Input Levels for Single-Ended Signals

5.1.1 AC and DC Input Levels for Single-Ended CA and $\overline{CS}$ Signals

[Table 16] Single-Ended AC and DC Input Levels for CA and $\overline{CS}$ inputs

Symbol	Parameter	LPDDR2-1066		Unit	Notes
		Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	V	1
V_{RefCA}(DC)	Reference Voltage for CA and $\overline{CS}$ inputs	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

NOTE :
1) For CA and $\overline{CS}$ input only pins. $V_{Ref} = V_{RefCA}$(DC).
2) See 6.5 Overshoot and Undershoot Specifications.
3) The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from V_{RefCA}(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4) For reference: approx. VDDCA/2 +/- 12 mV.

5.2 AC and DC Input Levels for CKE

[Table 17] Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1

NOTE :
1) See 6.5 Overshoot and Undershoot Specifications.

5.2.1 AC and DC Input Levels for Single-Ended Data Signals

[Table 18] Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066		Unit	Notes
		Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	V	1
V_{RefDQ}(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

NOTE :
1) For DQ input only pins. Vref = V_{RefDQ}(DC).
2) See 6.5 Overshoot and Undershoot Specifications
3) The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from V_{RefDQ}(DC) by more than +/-1% VDDQ (for reference: approx. +/ - 12 mV).
4) For reference: approx. VDDQ/2 +/- 12 mV.

5.3 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 2 Illustration of VRef(DC) tolerance and VRef ac-noise limits. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ}. $V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 16 Single-Ended AC and DC Input Levels for CA and CS inputs. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref}(DC)$ by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

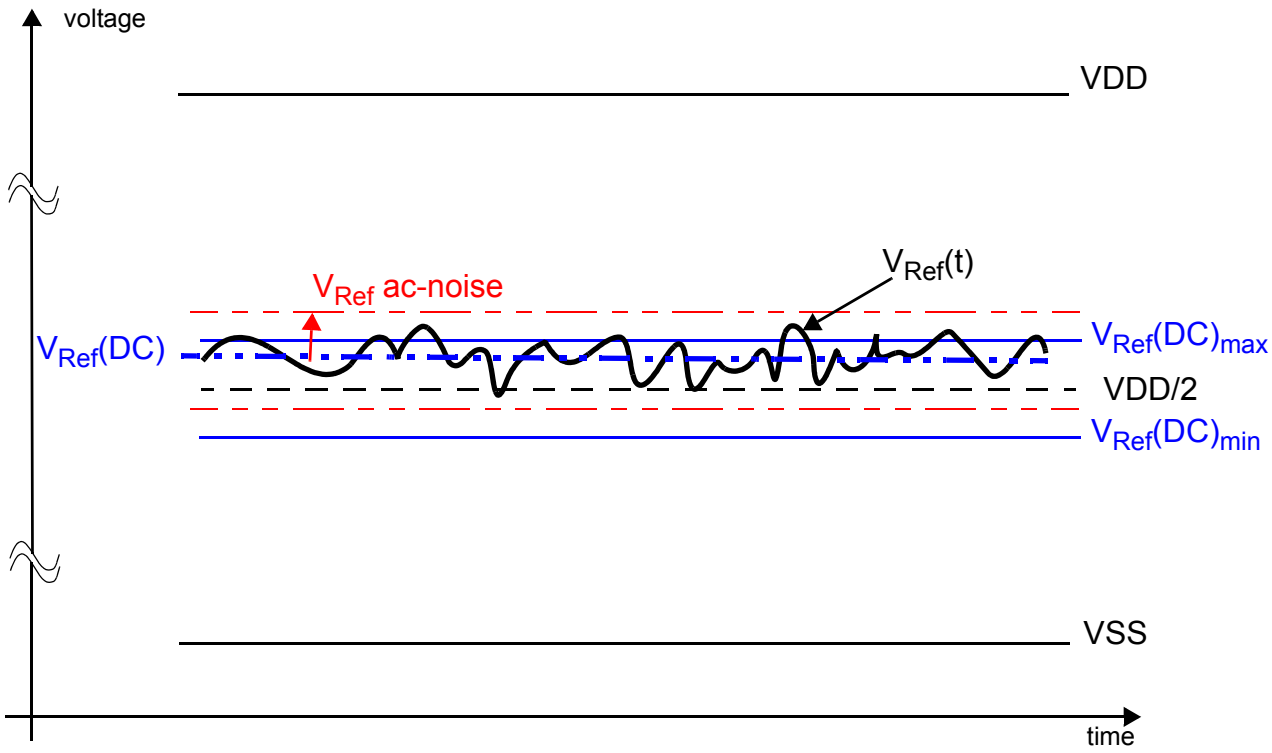


Figure 2. Illustration of V_{Ref}(DC) tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{Ref}.

"V_{Ref} " shall be understood as V_{Ref}(DC), as defined in Figure 2 Illustration of VRef(DC) tolerance and VRef ac-noise limits.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with V_{Ref} outside these specified levels so long as V_{Ref} is maintained between 0.44 x V_{DDQ} (or V_{DDCA}) and 0.56 x V_{DDQ} (or V_{DDCA}) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous V_{Ref} (see Table 16 Single-Ended AC and DC Input Levels for CA and CS inputs and Table 18 Single-Ended AC and DC Input Levels for DQ and DM) Therefore, System timing and voltage budgets need to account for V_{Ref} deviations outside if this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

5.4 Input Signal

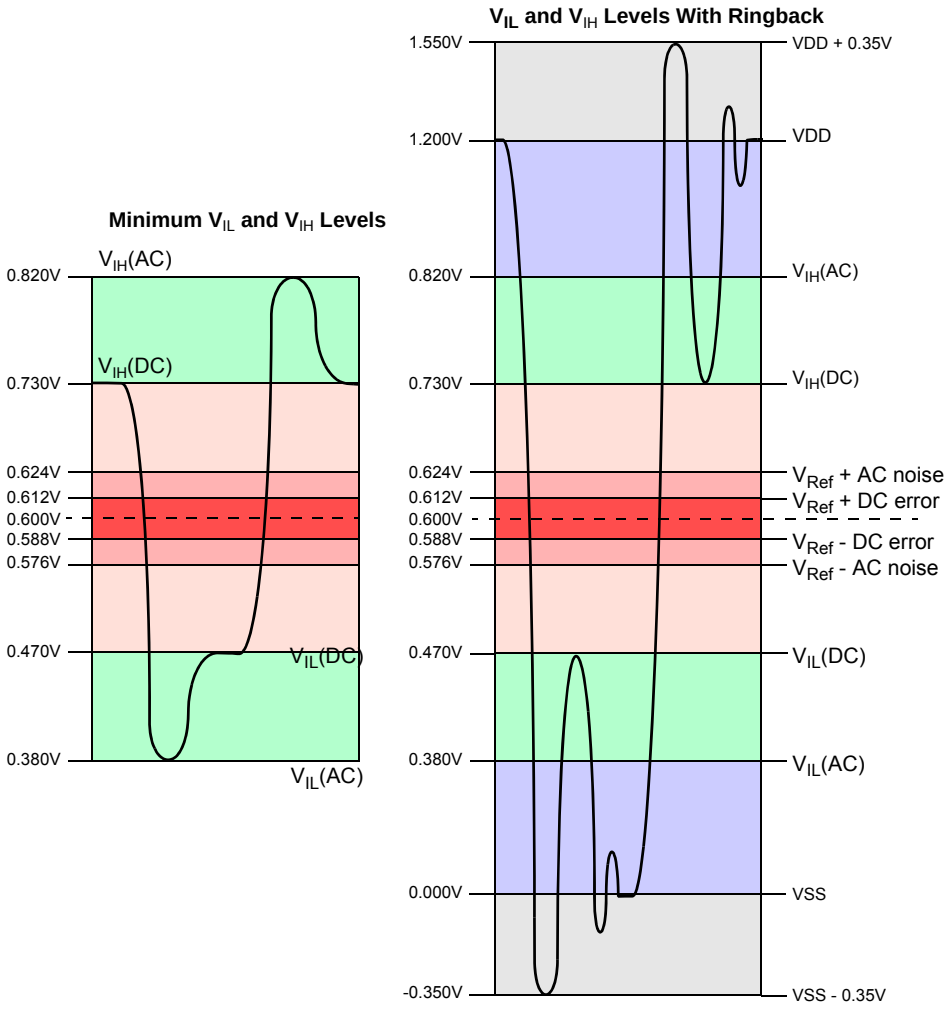


Figure 3. LPDDR2-1066 Input Signal

NOTE :

1) Numbers reflect nominal values

2) For CA0-9, CK, $\overline{CK}$, and $\overline{CS}$, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.

3) For CA0-9, CK, $\overline{CK}$, and $\overline{CS}$, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ

5.5 AC and DC Logic Input Levels for Differential Signals

5.5.1 Differential signal definition

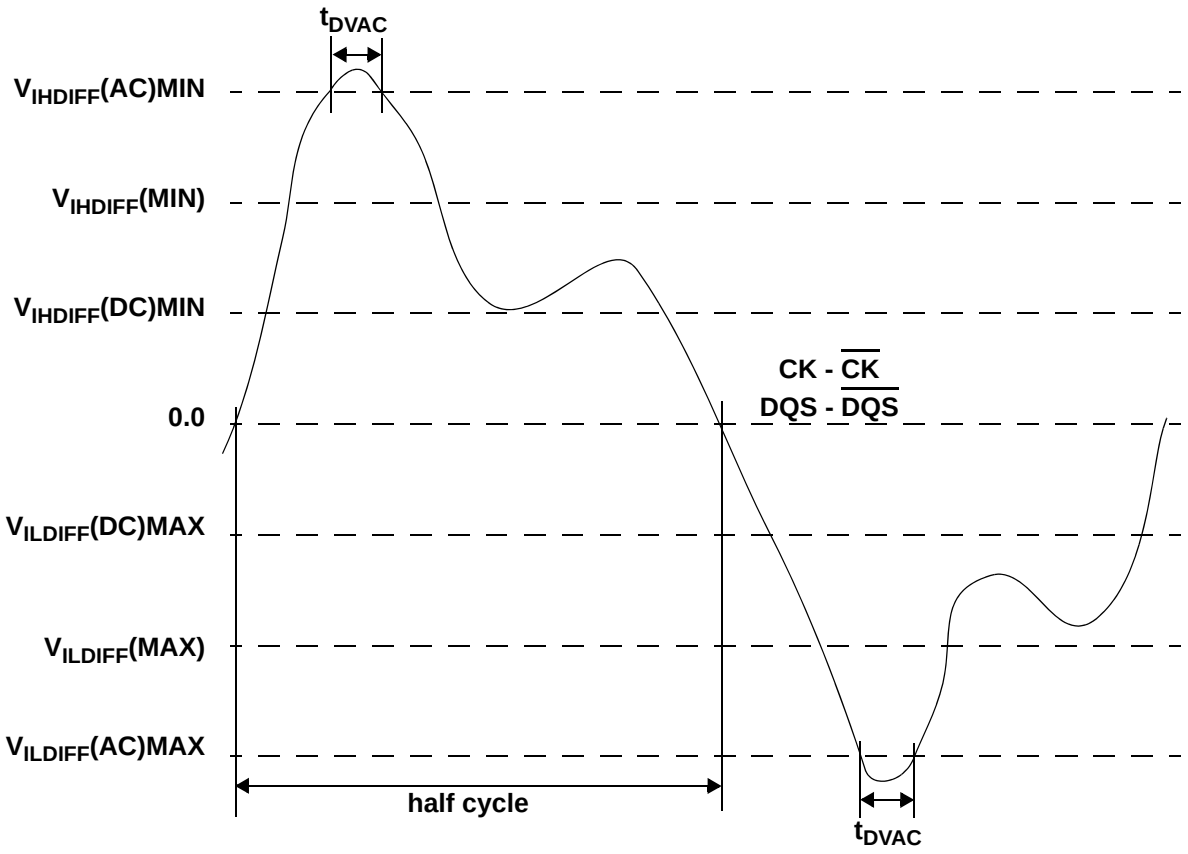


Figure 4. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

5.5.2 Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS - $\overline{DQS}$)

[Table 19] Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066		Unit	Notes
		Min	Max		
V_{IHdiff}(DC)	Differential input high	2 x (V_{IH}(DC) - Vref)	Note 3	V	1
V_{ILdiff}(DC)	Differential input logic low	Note 3	2 x (V_{IL}(dc) - Vref)	V	1
V_{IHdiff}(AC)	Differential input high ac	2 x (V_{IH}(AC) - Vref)	Note 3	V	2
V_{ILdiff}(AC)	Differential input low ac	Note 3	2 x (V_{IL}(ac) - Vref)	V	2

NOTE :
1) Used to define a differential signal slew-rate.
2) For CK - $\overline{CK}$ use V_{IH}/V_{IL}(AC) of CA and V_{RefCA}; for DQS - $\overline{DQS}$, use V_{IH}/V_{IL}(AC) of DQs and V_{RefDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3) These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, and $\overline{DQS}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 10.
4) For CK and $\overline{CK}$, Vref = V_{RefCA}(DC). For DQS and $\overline{DQS}$, Vref = V_{RefDQ}(DC).

[Table 20] Allowed time before ring back (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH}/Ldiff(AC)\|$ = 440mV	tDVAC [ps] @ $\|V_{IH}/Ldiff(AC)\|$ = 600mV
	min	min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

5.5.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, or $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{CK}$ shall meet V_{SEL}(AC)min / V_{SEL}(AC)max in every half-cycle.

DQS, $\overline{DQS}$ shall meet V_{SEH}(AC)min / V_{SEH}(AC)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

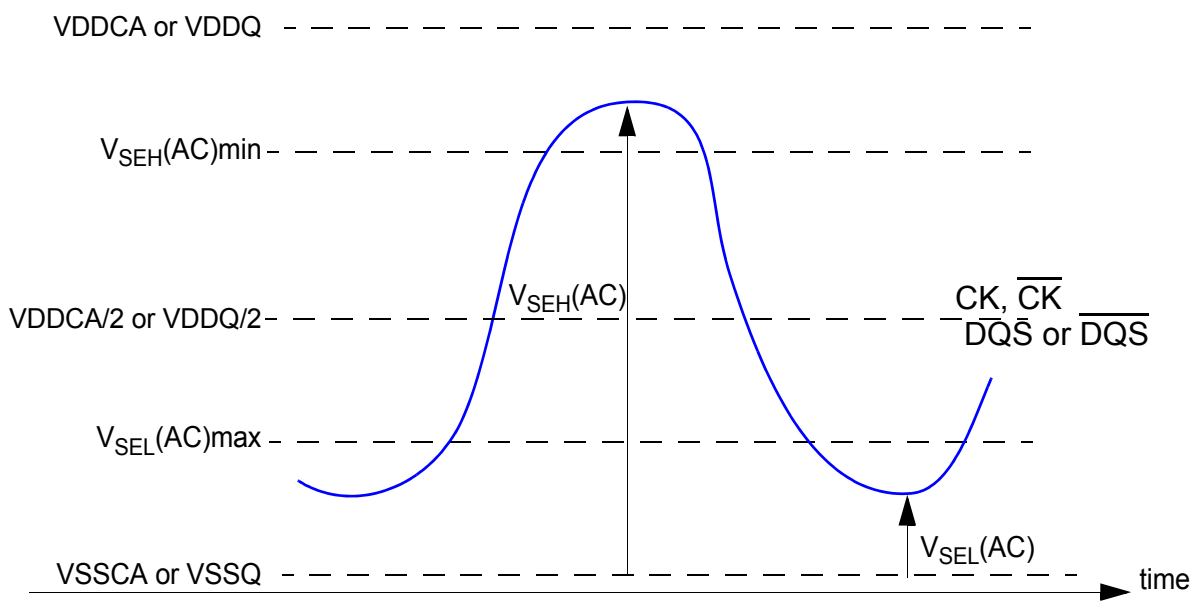


Figure 5. Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS, $\overline{DQS}$ and VDDCA/2 for CK, $\overline{CK}$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}(AC)max, V_{SEH}(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The single ended requirements for CK, $\overline{CK}$ and DQS, $\overline{DQS}$ are found in Table 16 Single-Ended AC and DC Input Levels for CA and CS inputs and Table 18 Single-Ended AC and DC Input Levels for DQ and DM, respectively.

[Table 21] Single-ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$

Symbol	Parameter	LPDDR2-1066		Unit	Notes
		Min	Max		
V_{SEH} (AC)	Single-ended high-level for strobes	(VDDQ/2)+0.220	Note 3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	(VDDCA/2)+0.220	Note 3	V	1, 2
V_{SEL} (AC)	Single-ended low-level for strobes	Note 3	(VDDQ/2)-0.220	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note 3	(VDDCA/2)-0.220	V	1, 2

NOTE :

1) For CK, $\overline{CK}$ use V_{SEH}/V_{SEL}(AC) of CA; for strobes (DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$) use V_{IH}/V_{IL}(AC) of DQs.

2) V_{IH}(AC)/V_{IL}(AC) for DQs is based on V_{RefDQ}; V_{SEH}(AC)/V_{SEL}(AC) for CA is based on V_{RefCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

3) These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS0, $\overline{DQS0}$, DQS1, $\overline{DQS1}$, DQS2, $\overline{DQS2}$, DQS3, $\overline{DQS3}$ need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to Figure 6.5

5.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in Table 21. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid-level between of VDD and VSS.

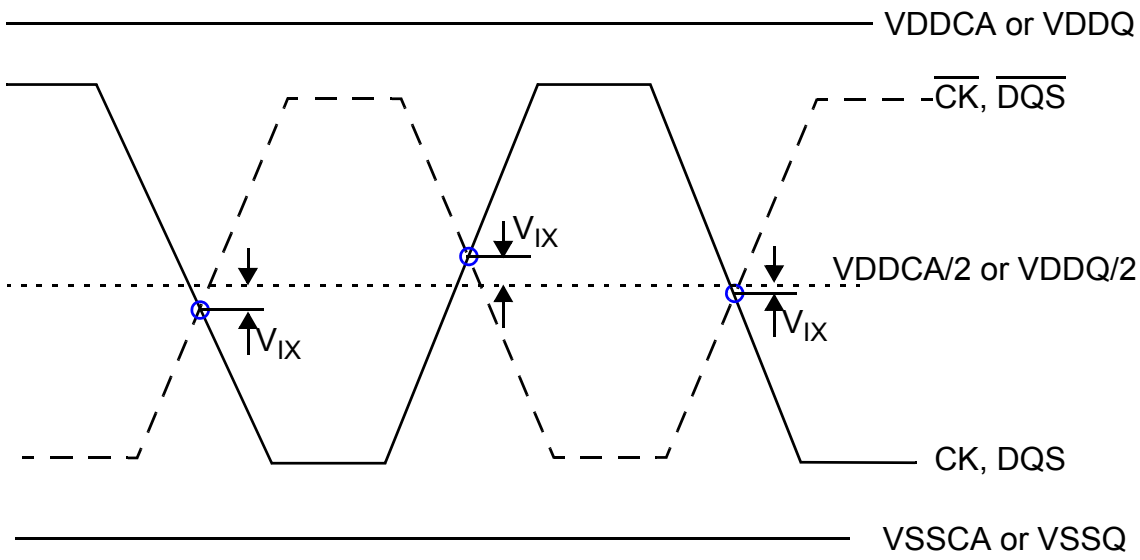


Figure 6. Vix Definition

[Table 22] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066		Unit	Notes
		Min	Max		
V_{IXCA}	Differential Input Cross Point Voltage relative to VDDCA/2 for CK, $\overline{CK}$	- 120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS, $\overline{DQS}$	- 120	120	mV	1,2

NOTE :
1)The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2) For CK and $\overline{CK}$, Vref = V_{RefCA}(DC). For DQS and $\overline{DQS}$, Vref = V_{RefDQ}(DC).

5.7 Slew Rate Definitions for Single-Ended Input Signals

See 11.5 CA and CS Setup, Hold and Derating for single-ended slew rate definitions for address and command signals.

See 11.6 Data Setup, Hold and Slew Rate Deratingfor single-ended slew rate definitions for data signals.

5.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in Table 23 and Figure 7 Differential Input Slew Rate Definition for DQS, DQS and CK, CK.

[Table 23] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge (CK - $\overline{CK}$ and DQS - $\overline{DQS}$).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$

NOTE :
1) The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.

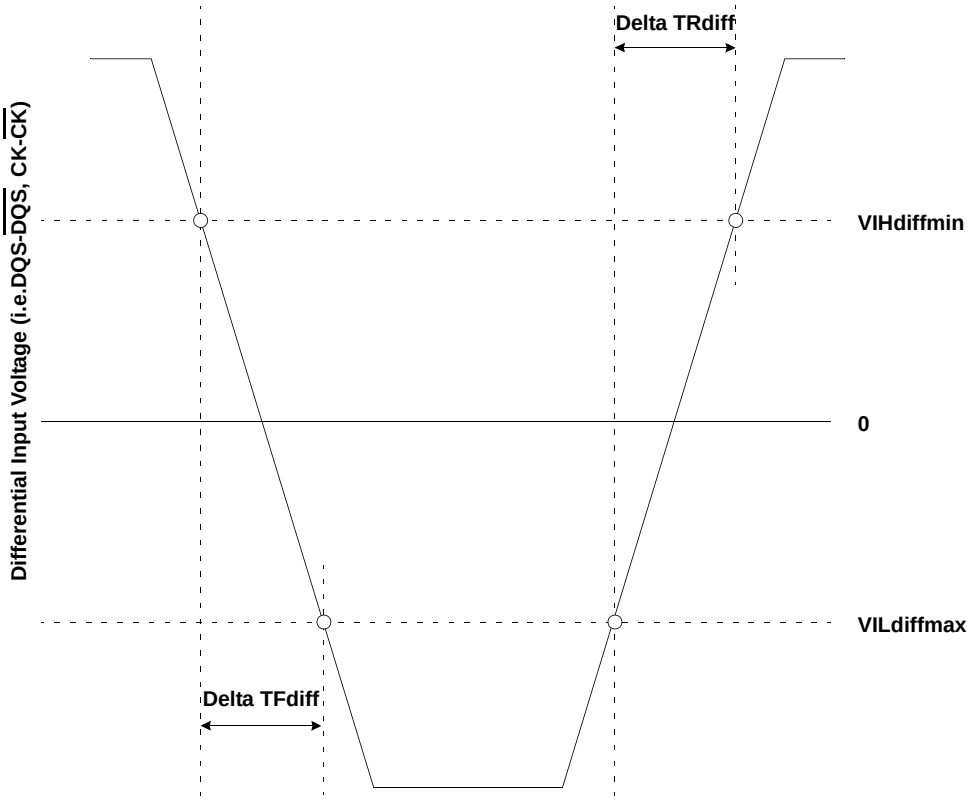


Figure 7. Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

6.0 AC AND DC OUTPUT MEASUREMENT LEVELS

6.1 Single Ended AC and DC Output Levels

Table 24 shows the output levels used for measurements of single ended signals.

[Table 24] Single-ended AC and DC Output Levels

Symbol	Parameter		LPDDR2-1066	Unit	Notes
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH}(AC)$	DC output high measurement level (for IV curve linearity)		V_{Ref} + 0.12	V	
$V_{OL}(AC)$	DC output low measurement level (for IV curve linearity)		V_{Ref} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS, $\overline{DQS}$) (DQs are disabled; 0V ≤ VOUT ≤ VDDQ	Min	-5	uA	
		Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	

NOTE :
1) IOH = -0.1mA.
2) IOL = 0.1mA.

6.2 Differential AC and DC Output Levels

Table 25 shows the output levels used for measurements of differential signals (DQS, $\overline{DQS}$).

[Table 25] Differential AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066	Unit	Notes
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	2

NOTE :
1) IOH = -0.1mA.
2) IOL = 0.1mA.

6.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals as shown in Table 26 and Figure 8.

[Table 26] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / DeltaTFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

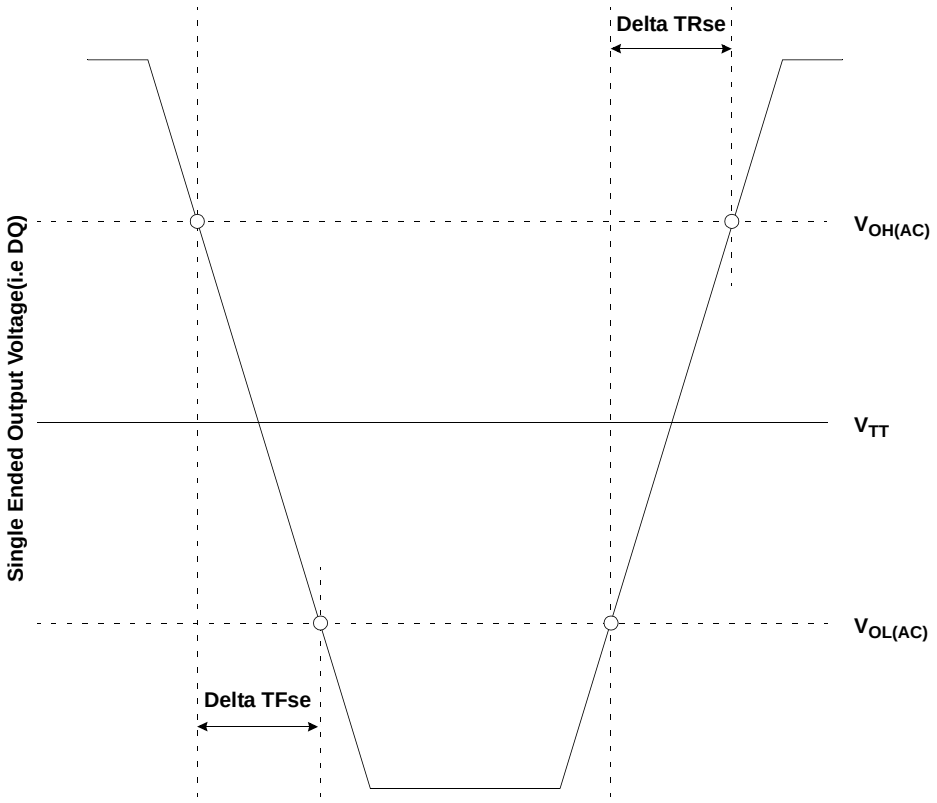


Figure 8. Single Ended Output Slew Rate Definition

[Table 27] Output Slew Rate (single-ended)

Parameter	Symbol	LPDDR2-1066		Units
		Min	Max	
Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω +/- 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals				

NOTE :
1) Measured with output reference load.
2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3) The output slew rate for falling and rising edges is defined and measured between VOL(DC) and VOH(DC).
4) Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

6.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOH-diff(AC) for differential signals as shown in Table 28 and Figure 9 Differential Output Slew Rate Definition.

[Table 28] Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC) - V_{OLdiff}(AC)]$ / DeltaTFdiff

NOTE :
1)Output slew rate is verified by design and characterization, and may not be subject to production test.

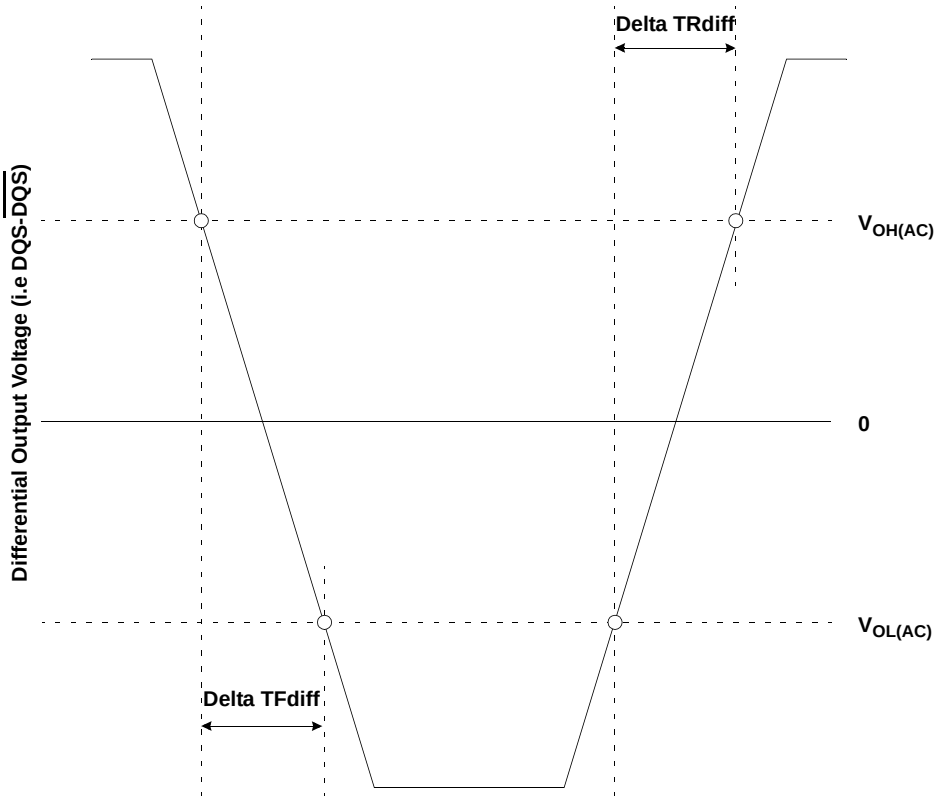


Figure 9. Differential Output Slew Rate Definition

[Table 29] Differential Output Slew Rate

Parameter	Symbol	LPDDR2-1066		Units
		Min	Max	
Differential Output Slew Rate (RON = 40Ω +/- 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω +/- 30%)	SRQdiff	2.0	5.0	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals				

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3) Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

6.5 Overshoot and Undershoot Specifications

[Table 30] AC Overshoot/Undershoot Specification

Parameter		1066	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 10 Overshoot and Undershoot Definition)	Max	0.35	V
Maximum peak amplitude allowed for undershoot area. (See Figure 10 Overshoot and Undershoot Definition)	Max	0.35	V
Maximum area above VDD. (See Figure 10 Overshoot and Undershoot Definition)	Max	0.15	V-ns
Maximum area below VSS. (See Figure 10 Overshoot and Undershoot Definition)	Max	0.15	V-ns

NOTE :
1) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
2) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.
3) Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.

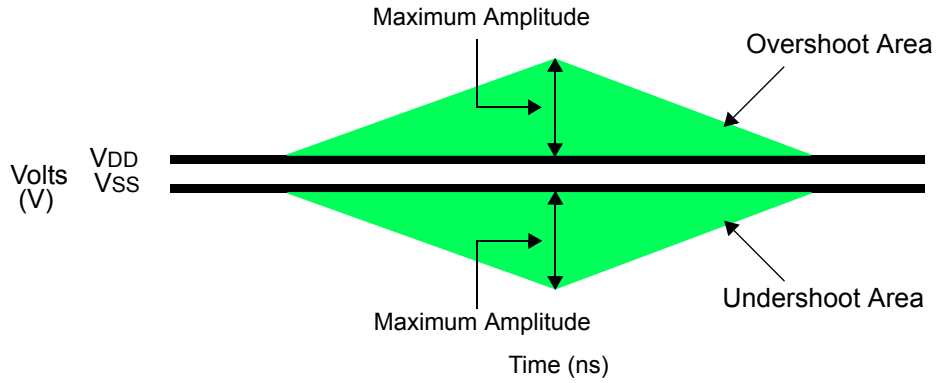


Figure 10. Overshoot and Undershoot Definition

NOTE :
1) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VDD stands for VDDCA. For DQ, DM, DQS, and $\overline{DQS}$, VDD stands for VDDQ.
2) For CA0-9, CK, $\overline{CK}$, $\overline{CS}$, and CKE, VSS stands for VSSCA. For DQ, DM, DQS, and $\overline{DQS}$, VSS stands for VSSQ.

7.0 OUTPUT BUFFER CHARACTERISTICS

7.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

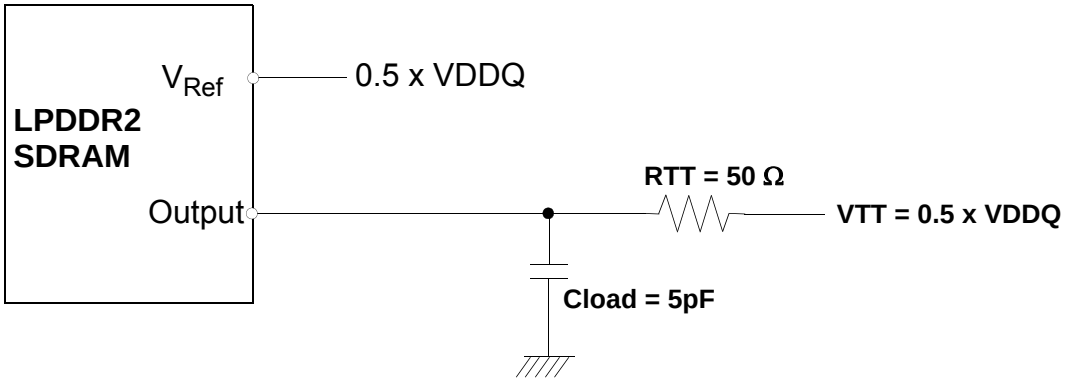


Figure 11. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

NOTE :

1) All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

8.0 RON_{PU} AND RON_{PD} RESISTOR DEFINITION

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE :
1)This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE :
1) This is under the condition that RON_{PU} is turned off

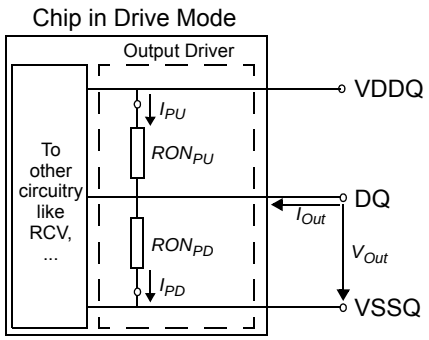


Figure 12. Output Driver: Definition of Voltages and Currents

8.1 RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω

[Table 31] Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0Ω	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	MMPUPD		-15.00		+15.00	%	1,2,3,4,5

NOTE :
1) Across entire operating temperature range, after calibration.
2) RZQ = 240Ω.
3) The tolerance limits are specified after calibration with stable voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4) Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.
5) Measurement definition for mismatch between pull-up and pull-down,
MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0

8.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

[Table 32] Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	$85 - (dRONdT \times \Delta T) - (dRONdV \times \Delta V)$	$115 + (dRONdT \times \Delta T) - (dRONdV \times \Delta V)$	%	1,2
RONPU					

NOTE :

1) $\Delta T = T - T$ (@ calibration), $\Delta V = V - V$ (@ calibration)
2) dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

[Table 33] Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

8.3 RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

[Table 34] Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1
120.0Ω	RON120PD	0.5 x VDDQ	84	120	156	Ω	1
	RON120PU	0.5 x VDDQ	84	120	156	Ω	1

NOTE:
1) Across entire operating temperature range, without calibration.

8.4 RZQ I-V Curve

[Table 35] RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

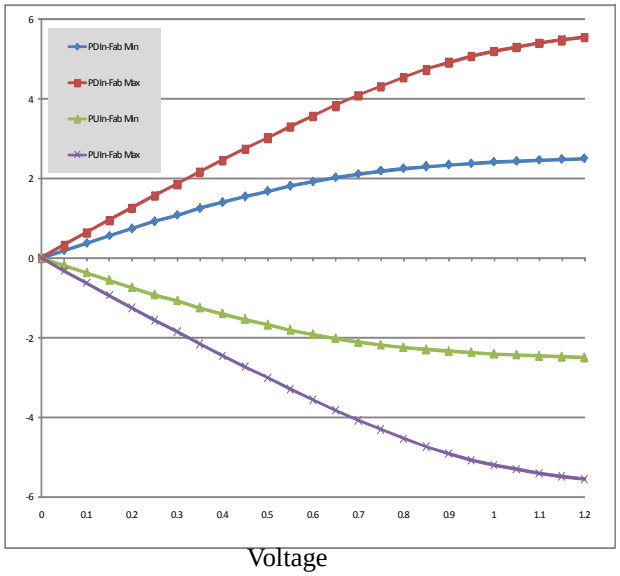


Figure 13. RON = 240 Ohms IV Curve after ZQReset

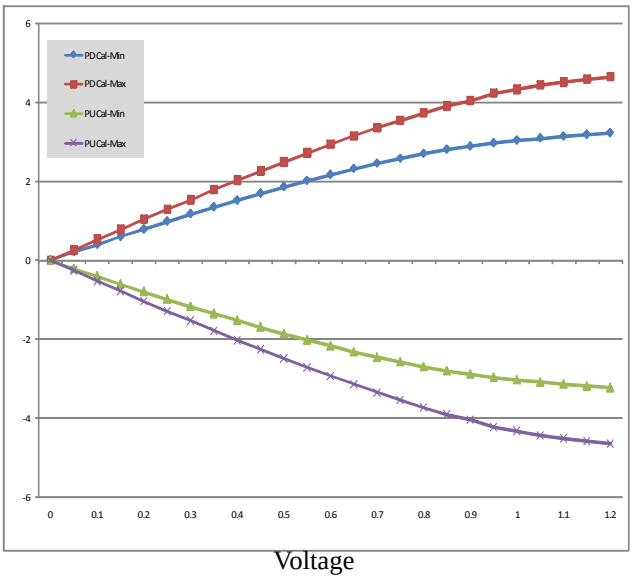


Figure 14. RON = 240 Ohms IV Curve after Calibration

9.0 INPUT/OUTPUT CAPACITANCE

[Table 36] Input/output capacitance

Parameter	Symbol		LPDDR2 1066	Units	Notes
Input capacitance, CK and $\overline{CK}$	CCK	Min	1.0	pF	1,2
		Max	3.0	pF	1,2
Input capacitance delta, CK and $\overline{CK}$	CDCK	Min	0.0	pF	1,2,3
		Max	0.20	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0	pF	1,2,4
		Max	3.0	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.5	pF	1,2,5
		Max	0.5	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	Min	1.25	pF	1,2,6,7
		Max	3.5	pF	1,2,6,7
Input/output capacitance delta, DQS, $\overline{DQS}$	CDDQS	Min	0.0	pF	1,2,7,8
		Max	0.25	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	pF	1,2,7,9
		Max	0.5	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0.0	pF	1,2
		Max	3.5	pF	1,2

(TOPER; V_{DDQ} = 1.14-1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, LPDDR2-S4B V_{DD2} = 1.14-1.3V)

NOTE :
1) This parameter applies to both die and package.
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating.
3) Absolute value of CCK - $\overline{CCK}$.
4) CI applies to $\overline{CS}$, CKE, CA0-CA9.
5) CDI = CI - 0.5 * (CCK + $\overline{CCK}$)
6) DM loading matches DQ and DQS.
7) MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
8) Absolute value of CDQS and C$\overline{DQS}$.
9) CDIO = CIO - 0.5 * (CDQS + C$\overline{DQS}$) in byte-lane.

10.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

10.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX

HIGH: $V_{IN} \geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 37 and Table 38.

[Table 37] Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)	CK (RISING) / $\overline{CK}$ (FALLING)	CK (FALLING) / $\overline{CK}$ (RISING)
Cycle	N		N+1		N+2		N+3	
$\overline{CS}$	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE :
1) $\overline{CS}$ must always be driven HIGH.
2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3) The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

[Table 38] Definition of Switching for IDD4R

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

[Table 39] Definition of Switching for IDD4W

Clock	CKE	$\overline{CS}$	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	HHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

NOTE :
1) Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2) Data masking (DM) must always be driven LOW.
3) The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

10.2 IDD Specifications

IDD values are for the entire operating voltage range and the standard and extended temperature ranges, unless otherwise noted.

[Table 40] LPDDR2 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Units	Notes
Operating one bank active-precharge current $t_{CK} = t_{CK(avg)min}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD0_1$	VDD1	mA	3
	$IDD0_2$	VDD2	mA	3
	$IDD0_{IN}$	VDDCA + VDDQ	mA	3,4
Idle power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is LOW; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2P_1$	VDD1	mA	3
	$IDD2P_2$	VDD2	mA	3
	$IDD2P_{IN}$	VDDCA + VDDQ	mA	3,4
Idle power-down standby current with clock stop: CK =LOW, $\overline{CK}$ =HIGH; CKE is LOW; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2PS_1$	VDD1	mA	3
	$IDD2PS_2$	VDD2	mA	3
	$IDD2PS_{IN}$	VDDCA + VDDQ	mA	3,4
Idle non power-down standby current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH; $\overline{CS}$ is HIGH; All banks idle; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2N_1$	VDD1	mA	3
	$IDD2N_2$	VDD2	mA	3
	$IDD2N_{IN}$	VDDCA + VDDQ	mA	3,4
Idle non power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; CKE is HIGH; $\overline{CS}$ is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD2NS_1$	VDD1	mA	3
	$IDD2NS_2$	VDD2	mA	3
	$IDD2NS_{IN}$	VDDCA + VDDQ	mA	3,4

Parameter/Condition	Symbol	Power Supply	Units	Notes
Active power-down standby current: $t_{CK} = t_{CK(avg)min}$; $\overline{CKE}$ is LOW; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3P_1$	VDD1	mA	3
	$IDD3P_2$	VDD2	mA	3
	$IDD3P_{IN}$	VDDCA + VDDQ	mA	3,4
Active power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; $\overline{CKE}$ is LOW; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3PS_1$	VDD1	mA	3
	$IDD3PS_2$	VDD2	mA	3
	$IDD3PS_{IN}$	VDDCA + VDDQ	mA	3,4
Active non power-down standby current: $t_{CK} = t_{CK(avg)min}$; $\overline{CKE}$ is HIGH; $\overline{CS}$ is HIGH; One bank active; Address bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3N_1$	VDD1	mA	3
	$IDD3N_2$	VDD2	mA	3
	$IDD3N_{IN}$	VDDCA + VDDQ	mA	3,4
Active non power-down standby current with clock stop: CK=LOW, $\overline{CK}$=HIGH; $\overline{CKE}$ is HIGH; $\overline{CS}$ is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	$IDD3NS_1$	VDD1	mA	3
	$IDD3NS_2$	VDD2	mA	3
	$IDD3NS_{IN}$	VDDCA + VDDQ	mA	3,4
Operating burst read current: $t_{CK} = t_{CK(avg)min}$; $\overline{CS}$ is HIGH between valid commands; One bank active; BL = 4; RL = RLmin; Address bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	VDD1	mA	3
	$IDD4R_2$	VDD2	mA	3
	$IDD4R_{IN}$	VDDCA	mA	3
	$IDD4R_Q$	VDDQ	mA	3,6
Operating burst write current: $t_{CK} = t_{CK(avg)min}$; $\overline{CS}$ is HIGH between valid commands; One bank active; BL = 4; WL = WLmin; Address bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	mA	3
	$IDD4W_2$	VDD2	mA	3
	$IDD4W_{IN}$	VDDCA + VDDQ	mA	3,4
All Bank Refresh Burst current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5_1$	VDD1	mA	3
	$IDD5_2$	VDD2	mA	3
	$IDD5_{IN}$	VDDCA + VDDQ	mA	3,4
All Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5AB_1$	VDD1	mA	3
	$IDD5AB_2$	VDD2	mA	3
	$IDD5AB_{IN}$	VDDCA + VDDQ	mA	3,4
Per Bank Refresh Average current: $t_{CK} = t_{CK(avg)min}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; Address bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5PB_1$	VDD1	mA	1,3
	$IDD5PB_2$	VDD2	mA	1,3
	$IDD5PB_{IN}$	VDDCA + VDDQ	mA	1,3,4

Parameter/Condition	Symbol	Power Supply	Units	Notes
Self refresh current (Standard Temperature Range): CK=LOW, $\overline{CK}$=HIGH; CKE is LOW; Address bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-Refresh Rate;	$IDD6_1$	VDD1	mA	2,3,8,9,10
	$IDD6_2$	VDD2	mA	2,3,8,9,10
	$IDD6_{IN}$	VDDCA + VDDQ	mA	2,3,4,8,9, 10
Deep Power-Down current: Address bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	VDD1	uA	3,11,12
	$IDD8_2$	VDD2	uA	3,11,12
	$IDD8_{IN}$	VDDCA + VDDQ	uA	3,4,11,12

NOTE :

1) Per Bank Refresh only applicable for LPDDR2-S4 devices of 1Gb or higher densities.
2) This is the general definition that applies to full array Self Refresh. Refer to Table 42 IDD6 Partial Array Self-Refresh Current for details of Partial Array Self Refresh IDD6 specification.
3) IDD values published are the maximum of the distribution of the arithmetic mean.
4) Measured currents are the summation of VDDQ and VDDCA.
5) To calculate total current consumption, the currents of all active operations must be considered.
6) Guaranteed by design with Un-termination and 5pF output loading cap.
7) IDD current specifications are tested after the device is properly initialized.
8) In addition, supplier data sheets may include additional Self Refresh IDD values for temperature subranges within the Standard or Extended Temperature Ranges.
9) 1x Self-Refresh Rate is the rate at which the LPDDR2-S4 device is refreshed internally during Self-Refresh in the Standard Temperature range.
10) IDD6 85°C is guaranteed, IDD6 45°C is typical values.
11) IDD8 85°C is guaranteed, IDD8 45°C is typical values.
12) DPD (Deep Power Down) function is an optional feature, and it will be enabled upon request.
Please contact Samsung for more information.

10.3 IDD Spec Table

[Table 41] IDD Specification for 2Gb LPDDR2-S4B

Symbol		Power Supply	VDD2=1.2V (S4B) 64M x32 1066Mbps	Units	Notes
IDD0	$IDD0_1$	VDD1	7	mA	3
	$IDD0_2$	VDD2	45	mA	3
	$IDD0_{IN}$	VDDCA + VDDQ	5	mA	3,4
IDD2P	$IDD2P_1$	VDD1	0.3	mA	3
	$IDD2P_2$	VDD2	0.8	mA	3
	$IDD2P_{IN}$	VDDCA + VDDQ	0.1	mA	3,4
IDD2PS	$IDD2PS_1$	VDD1	0.3	mA	3
	$IDD2PS_2$	VDD2	0.8	mA	3
	$IDD2PS_{IN}$	VDDCA + VDDQ	0.1	mA	3,4
IDD2N	$IDD2N_1$	VDD1	1	mA	3
	$IDD2N_2$	VDD2	12	mA	3
	$IDD2N_{IN}$	VDDCA + VDDQ	5	mA	3,4
IDD2NS	$IDD2NS_1$	VDD1	1	mA	3
	$IDD2NS_2$	VDD2	5	mA	3
	$IDD2NS_{IN}$	VDDCA + VDDQ	5	mA	3,4
IDD3P	$IDD3P_1$	VDD1	2	mA	3
	$IDD3P_2$	VDD2	4	mA	3
	$IDD3P_{IN}$	VDDCA + VDDQ	0.1	mA	3,4
IDD3PS	$IDD3PS_1$	VDD1	2	mA	3
	$IDD3PS_2$	VDD2	4	mA	3
	$IDD3PS_{IN}$	VDDCA + VDDQ	0.1	mA	3,4
IDD3N	$IDD3N_1$	VDD1	2	mA	3
	$IDD3N_2$	VDD2	16	mA	3
	$IDD3N_{IN}$	VDDCA + VDDQ	5	mA	3,4
IDD3NS	$IDD3NS_1$	VDD1	2	mA	3
	$IDD3NS_2$	VDD2	7	mA	3
	$IDD3NS_{IN}$	VDDCA + VDDQ	5	mA	3,4
IDD4R	$IDD4R_1$	VDD1	2	mA	3
	$IDD4R_2$	VDD2	160	mA	3
	$IDD4R_{IN}$	VDDCA	5	mA	3
	$IDD4R_Q$	VDDQ	140	mA	3,6
IDD4W	$IDD4W_1$	VDD1	2	mA	3
	$IDD4W_2$	VDD2	170	mA	3
	$IDD4W_{IN}$	VDDCA + VDDQ	13	mA	3,4

Symbol			Power Supply	VDD2=1.2V (S4B) 64M x32 1066Mbps	Units	Notes
IDD5	$IDD5_1$		VDD1	10	mA	3
	$IDD5_2$		VDD2	90	mA	3
	$IDD5_{IN}$		VDDCA + VDDQ	5	mA	3,4
IDD5AB	$IDD5AB_1$		VDD1	2	mA	3
	$IDD5AB_2$		VDD2	10	mA	3
	$IDD5AB_{IN}$		VDDCA + VDDQ	5	mA	3,4
IDD5PB	$IDD5PB_1$		VDD1	2	mA	1,3
	$IDD5PB_2$		VDD2	20	mA	1,3
	$IDD5PB_{IN}$		VDDCA + VDDQ	5	mA	1,3,4
IDD6	$IDD6_1$	45°C	VDD1	0.12	mA	2,3,8,9,10
		85°C		0.5		
	$IDD6_2$	45°C	VDD2	0.32	mA	2,3,8,9,10
		85°C		1.7		
	$IDD6_{IN}$	45°C	VDDCA + VDDQ	0.01	mA	2,3,4,8,9,10
		85°C		0.1		
IDD8	$IDD8_1$	45°C	VDD1	5	uA	3,11,12
		85°C		20		
	$IDD8_2$	45°C	VDD2	10	uA	3,11,12
		85°C		50		
	$IDD8_{IN}$	45°C	VDDCA + VDDQ	5	uA	3,4,11,12
		85°C		20		

NOTE :
1) See Table 40 LPDDR2 IDD Specification Parameters and Operating Conditions for notes.

[Table 42] IDD6 Partial Array Self-Refresh Current

Parameter			2Gb LPDDR2-S4B 45°C	2Gb LPDDR2-S4B 85°C	Unit
IDD6 Partial Array Self-Refresh Current (max)	Full Array	VDD1	120	500	uA
		VDD2	320	1700	
		VDDCA + VDDQ	10	100	
	1/2 Array[3)]	VDD1	110	400	uA
		VDD2	220	1200	
		VDDCA + VDDQ	10	100	
	1/4 Array[3)]	VDD1	100	350	uA
		VDD2	160	900	
		VDDCA + VDDQ	10	100	
	1/8 Array[3)]	VDD1	95	320	uA
		VDD2	140	750	
		VDDCA + VDDQ	10	100	

NOTE :
1) IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.
2) IDD6 85°C is guaranteed, IDD6 45°C is typical values.
3) PASR(Partial Array Self-Refresh) function will be supported upon request. Please contact Samsung for more information.

11.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

11.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

11.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

11.1.2 Definition for tCK(abs)

t_{CK}(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. t_{CK}(abs) is not subject to production test.

11.1.3 Definition for tCH(avg) and tCL(avg)

t_{CH}(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

t_{CL}(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

11.1.4 Definition for tJIT(per)

t_{JIT}(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

t_{JIT}(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.

t_{JIT}(per),act is the actual clock jitter for a given system.

t_{JIT}(per),allowed is the specified allowed clock period jitter.

t_{JIT}(per) is not subject to production test.

11.1.5 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$t_{JIT}(cc)$ = Max of $|\{tCK_{i+1} - tCK_i\}|$.

$t_{JIT}(cc)$ defines the cycle to cycle jitter.

$t_{JIT}(cc)$ is not subject to production test.

11.1.6 Definition for tERR(nper)

$t_{ERR}(nper)$ is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).

$t_{ERR}(nper)$,act is the actual clock jitter over n cycles for a given system.

$t_{ERR}(nper)$,allowed is the specified allowed clock period jitter over n cycles.

$t_{ERR}(nper)$ is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

$t_{ERR}(nper)$,min can be calculated by the formula shown below:

$$tERR(nper), min = (1+0.68\ LN(n)) \times tJIT(per), min$$

$t_{ERR}(nper)$,max can be calculated by the formula shown below

$$tERR(nper), max = (1+0.68\ LN(n)) \times tJIT(per), max$$

Using these equations, $t_{ERR}(nper)$ tables can be generated for each $t_{JIT}(per)$,act value.

11.1.7 Definition for duty cycle jitter tJIT(duty)

$t_{JIT}(duty)$ is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN ((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

$$tJIT(duty), max = MAX ((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

11.1.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times

[Table 43] Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg).min + tJIT(per).min	ps
Absolute Clock HIGH Pulse Width	t_{CH}(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	t_{CL}(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

NOTE :
1) tCK(avg),min is expressed is ps for this table.
2) tJIT(duty),min is a negative value.

11.2 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 45 LPDDR2 AC Timing Table and how to determine cycle time de-rating and clock cycle de-rating.

11.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

NOTE :
1) tFAW is only applied in devices with 8 banks.

11.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

11.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter

11.2.2 Clock jitter effects on Command/Address timing parameters

(tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.3 Clock jitter effects on Read timing parameters

11.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max= + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500= .8628 tCK(avg)

11.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

11.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min – 0.05

tQSL(abs)min = tCL(abs)min – 0.05

These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @LPDDR2 device pin =

min { (tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

11.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

11.2.4 Clock jitter effects on Write timing parameters

11.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn, $\overline{DQSn}$: n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx, $\overline{DQSx}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

11.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx, $\overline{DQSx}$) crossing to the subsequent clock signal (CK/$\overline{CK}$) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max= + 193 ps, then

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

11.3 LPDDR2-S4 Refresh Requirement per Device Density

[Table 44] LPDDR2-S4 Refresh Requirement Parameters (per density)

Parameter		Symbol	2 Gb	Unit
Number of Banks			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Required number of REFRESH commands (min)		R	8,192	
average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns
Burst Refresh Window = 4 x 8 x t_{RFCab}		t_{REFBW}	4.16	us

11.4 AC Timings

[Table 45] LPDDR2 AC Timing Table

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	Unit
Max. Frequency*4		~		533	MHz
Clock Timing					
Average Clock Period	t_{CK}(avg)	min		1.875	ns
		max		100	
Average high pulse width	t_{CH}(avg)	min		0.45	t_{CK}(avg)
		max		0.55	
Average low pulse width	t_{CL}(avg)	min		0.45	t_{CK}(avg)
		max		0.55	
Absolute Clock Period	t_{CK}(abs)	min		t_{CK}(avg)min -/+ t_{JIT}(per), min	ps
Absolute clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	min		0.43	t_{CK}(avg)
		max		0.57	
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	min		0.43	t_{CK}(avg)
		max		0.57	
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	min		-90	ps
		max		90	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t_{JIT}(cc), allowed	max		180	ps
Duty cycle Jitter (with allowed jitter)	t_{JIT}(duty), allowed	min		min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) * t_{CK}(avg)	ps
		max		max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) * t_{CK}(avg)	ps
Cumulative error across 2 cycles	t_{ERR}(2per), allowed	min		-132	ps
		max		132	
Cumulative error across 3 cycles	t_{ERR}(3per), allowed	min		-157	ps
		max		157	
Cumulative error across 4 cycles	t_{ERR}(4per), allowed	min		-175	ps
		max		175	
Cumulative error across 5 cycles	$t_{ERR(5per)}$, allowed	min		-188	ps
		max		188	
Cumulative error across 6 cycles	$t_{ERR(6per)}$, allowed	min		-200	ps
		max		200	
Cumulative error across 7 cycles	$t_{ERR(7per)}$, allowed	min		-209	ps
		max		209	
Cumulative error across 8 cycles	$t_{ERR(8per)}$, allowed	min		-217	ps
		max		217	
Cumulative error across 9 cycles	$t_{ERR(9per)}$, allowed	min		-224	ps
		max		224	
Cumulative error across 10 cycles	$t_{ERR(10per)}$, allowed	min		-231	ps
		max		231	

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	Unit
Cumulative error across 11 cycles	$t_{ERR(11per)}$, allowed	min		-237	ps
		max		237	
Cumulative error across 12 cycles	$t_{ERR(12per)}$, allowed	min		-242	ps
		max		242	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	$t_{ERR(nper)}$, allowed	min		tERR(nper), allowed, min = (1 + 0.68ln(n)) * tJIT(per), allowed, min	ps
		max		tERR(nper), allowed, max = (1 + 0.68ln(n)) * tJIT(per), allowed, max	
ZQ Calibration Parameters					
Initialization Calibration Time*14	t_{ZQINIT}	min		1	us
Full Calibration Time*14	t_{ZQCL}	min	6	360	ns
Short Calibration Time*14	t_{ZQCS}	min	6	90	ns
Calibration Reset Time*14	$t_{ZQRESET}$	min	3	50	ns
Read Parameters*11					
DQS output access time from CK/CK#	t_{DQSCK}	min		2500	ps
		max		5500	
DQSCK Delta Short*15	$t_{DQSCKDS}$	max		330	ps
DQSCK Delta Medium*16	$t_{DQSCKDM}$	max		680	ps
DQSCK Delta Long*17	$t_{DQSCKDL}$	max		920	ps
DQS - DQ skew	t_{DQSQ}	max		200	ps
Data hold skew factor	t_{QHS}	max		230	ps
DQS Output High Pulse Width	t_{QSH}	min		t_{CH}(abs) - 0.05	t_{CK}(avg)
DQS Output Low Pulse Width	t_{QSL}	min		t_{CL}(abs) - 0.05	t_{CK}(avg)
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})	t_{CK}(avg)
DQ / DQS output hold time from DQS	t_{QH}	min		t_{QHP} - t_{QHS}	ps
Read preamble*11,*12	t_{RPRE}	min		0.9	t_{CK}(avg)
Read postamble*11,*13	t_{RPST}	min		t_{CL}(abs) - 0.05	t_{CK}(avg)
DQS low-Z from clock*11	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)}$ - 300	ps
DQ low-Z from clock*11	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)}$ - (1.4 * $t_{QHS(MAX)}$)	ps
DQS high-Z from clock*11	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)}$ - 100	ps
DQ high-Z from clock*11	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)}$ + (1.4 * $t_{DQSQ(MAX)}$)	ps
Write Parameters*11					
DQ and DM input hold time (Vref based)	t_{DH}	min		210	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		210	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35	t_{CK}(avg)
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75	t_{CK}(avg)
		max		1.25	
DQS input high-level width	t_{DQSH}	min		0.4	t_{CK}(avg)

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	Unit
DQS input low-level width	t_{DQSL}	min		0.4	t_{CK}(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2	t_{CK}(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2	t_{CK}(avg)
Write postamble	t_{WPST}	min		0.4	t_{CK}(avg)
Write preamble	t_{WPRE}	min		0.35	t_{CK}(avg)
CKE Input Parameters					
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3	t_{CK}(avg)
CKE input setup time	t_{ISCKE} *2	min		0.25	t_{CK}(avg)
CKE input hold time	t_{IHCKE} *3	min		0.25	t_{CK}(avg)
Command Address Input Parameters*11					
Address and control input setup time	t_{IS} *1	min		220	ps
Address and control input hold time	t_{IH} *1	min		220	ps
Address and control input pulse width	t_{IPW}	min		0.40	t_{CK}(avg)
Boot Parameters (10 MHz - 55 MHz)*5,7,8					
Clock Cycle Time	t_{CKb}	max	-	100	ns
		min		18	
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5	ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5	ns
Address & Control Input Setup Time	t_{ISb}	min	-	1150	ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150	ps
DQS Output Data Access Time from CK/$\overline{CK}$	t_{DQSCKb}	min	-	2.0	ns
		max		10.0	
Data Strobe Edge to Output Data Edge t_{DQSQb} - 1.2	t_{DQSQb}	max	-	1.2	ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2	ns
Mode Register Parameters					
MODE REGISTER Write command period	t_{MRW}	min	5	5	t_{CK}(avg)
Mode Register Read command period	t_{MRR}	min	2	2	t_{CK}(avg)
LPDDR2 SDRAM Core Parameters*9					
Read Latency	RL	min	3	8	t_{CK}(avg)
Write Latency	WL	min	1	4	t_{CK}(avg)
ACTIVE to ACTIVE command period	t_{RC}	min		t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)	ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15	ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab} + 10	ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5	ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2	t_{CK}(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5	ns
RAS to CAS Delay	t_{RCD}	min	3	18	ns
Row Precharge Time (single bank)	t_{RPpb}	min	3	18	ns
Row Precharge Time (all banks)	t_{RPab} 4-bank	min	3	18	ns

Parameter	Symbol	min max	min t_{CK}	LPDDR2 1066	Unit
Row Precharge Time (all banks)	t_{RPab} 8-bank	min	3	21	ns
Row Active Time	t_{RAS}	min	3	42	ns
		max	-	70	us
Write Recovery Time	t_{WR}	min	3	15	ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5	ns
Active bank A to Active bank B	t_{RRD}	min	2	10	ns
Four Bank Activate Window	t_{FAW}	min	8	50	ns
Minimum Deep Power Down Time	t_{DPD}	min		500	us
LPDDR2 Temperature De-Rating					
t_{DQSCK} De-Rating	t_{DQSCK} (Derated)	max		6000	ps
Core Timings Temperature De-Rating for SDRAM	t_{RCD} (Derated)	min		t_{RCD} + 1.875	ns
	t_{RC} (Derated)	min		t_{RC} + 1.875	ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875	ns
	t_{RP} (Derated)	min		t_{RP} + 1.875	ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875	ns

NOTE :
1) Input set-up/hold time for signal(CA0 ~ 9, $\overline{CS}$)
2) CKE input setup time is measured from CKE reaching high/low voltage level to CK/$\overline{CK}$ crossing.
3) CKE input hold time is measured from CK/$\overline{CK}$ crossing to CKE reaching high/low voltage level.
4) Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5) To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in the Table 45 LPDDR2 AC Timing Table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6) Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7) The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in Figure 1.1.
8) The output skew parameters are measured with Ron default settings into the reference load.
9) The min tCK column applies only when tCK is greater than 6ns for LPDDR2-S4 devices. In this case, both min tCK values and analog timing (ns) shall be satisfied.
10) All AC timings assume an input slew rate of 1V/ns.
11) Read, Write, and Input Setup and Hold values are referenced to Vref.
12) For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 15 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

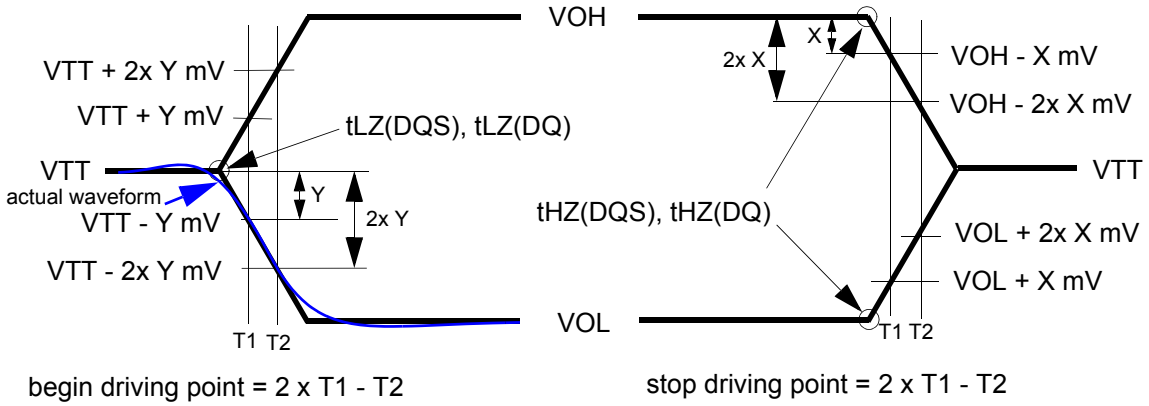


Figure 15. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-$\overline{DQS}$.

13) Measured from the start driving of DQS - $\overline{DQS}$ to the start driving the first rising strobe edge.
14) Measured from the start driving the last falling strobe edge to the stop driving DQS - $\overline{DQS}$.

15) tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
16) tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
17) tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
18) tFAW is only applied in devices with 8 banks.

11.5 CA and $\overline{CS}$ Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 46) to the ΔtIS and ΔtIH derating value (see Table 47) respectively.

Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IH}(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of Vil(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{Ref}(DC) to ac region', use nominal slew rate for derating value (see Figure 16 Illustration of nominal slew rate and tVAC for setup time tIS for CA and CS with respect to clock.). If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{Ref}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 18 Illustration of tangent line for setup time tIS for CA and CS with respect to clock).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(DC)max and the first crossing of V_{Ref}(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(DC)min and the first crossing of V_{Ref}(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{Ref}(DC) region', use nominal slew rate for derating value (see Figure 17 Illustration of nominal slew rate for hold time tIH for CA and CS with respect to clock). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{Ref}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{Ref}(DC) level is used for derating value (see Figure 19 Illustration of tangent line for hold time tIH for CA and CS with respect to clock).

For a valid transition the input signal has to remain above/below $V_{IH/IL}$(AC) for some time t_{VAC} (see Table 48).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in Table 47, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 46] CA and $\overline{CS}$ Setup and Hold Base-Values for 1V/ns

unit [ps]	LPDDR2	reference
	1066	
tIS(base)	0	VIH/L(ac)=VRef(dc)+-220mV
tIH(base)	90	VIH/L(dc)=VRef(dc)+-130mV

NOTE :
1) ac/dc referenced for 1V/ns CA and $\overline{CS}$ slew rate and 2V/ns differential CK-$\overline{CK}$ slew rate.

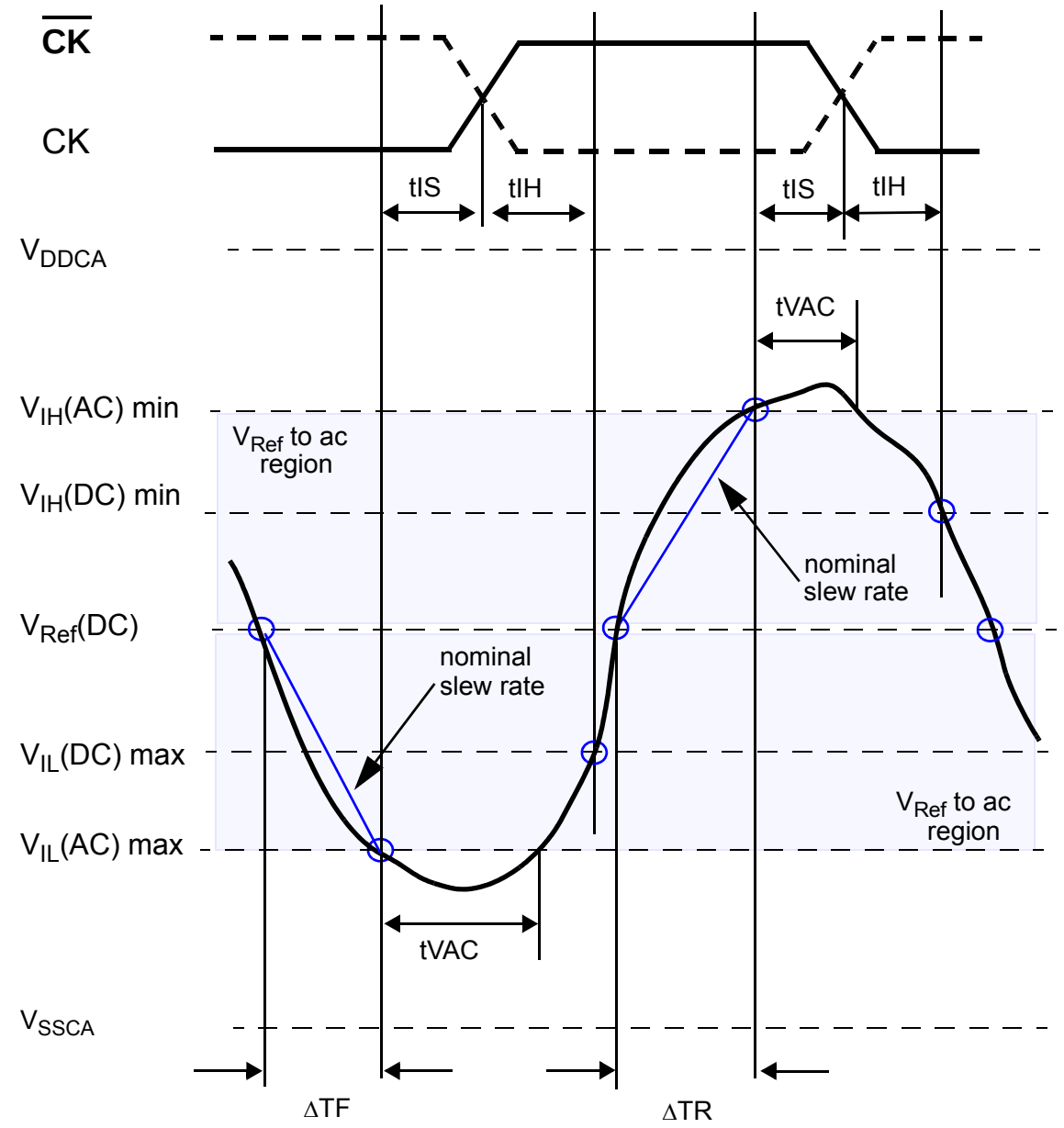
[Table 47] Derating values LPDDR2 tIS/tIH - ac/dc based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based AC220 Threshold -> V_{IH}(AC)=V_{Ref}(DC)+220mV, V_{IL}(AC)=V_{Ref}(DC)-220mV DC100 Threshold -> V_{IH}(DC)=V_{Ref}(DC)+130mV, V_{IL}(DC)=V_{Ref}(DC)-130mV																	
		CK,$\overline{CK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

NOTE :
1) Cell contents shaded in red are defined as 'not supported'

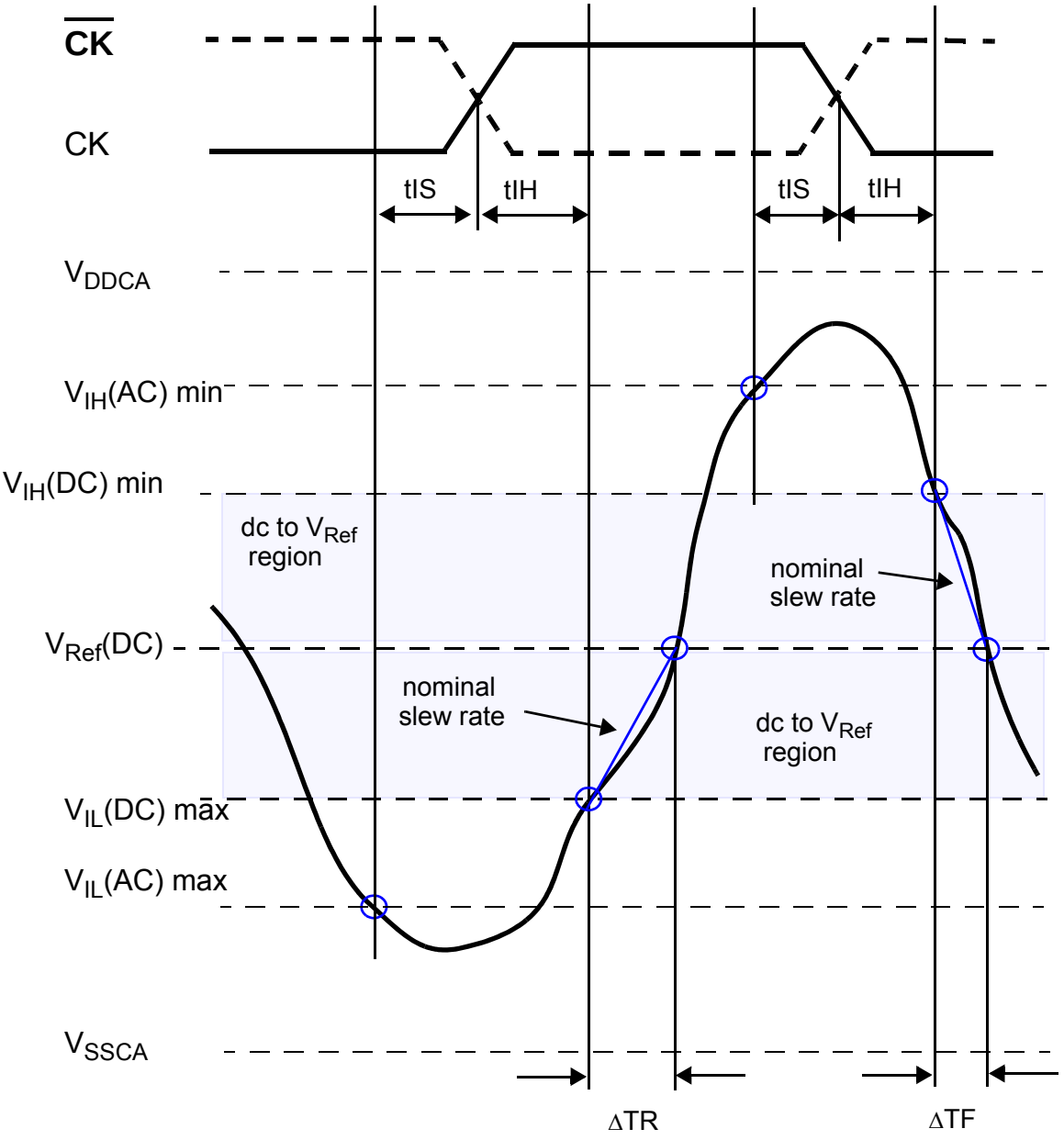
[Table 48] Required time t_{VAC} above V_{IH}(AC) {below V_{IL}(AC)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-



$$\text{Setup Slew Rate}_{\text{Falling Signal}} = \frac{V_{Ref}(DC) - V_{IL}(AC)max}{\Delta TF} \qquad \text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IH}(AC)min - V_{Ref}(DC)}{\Delta TR}$$

Figure 16. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and $\overline{CS}$ with respect to clock.



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{Ref}(DC)}{\Delta TF}$$

Figure 17. Illustration of nominal slew rate for hold time t_{IH} for CA and $\overline{CS}$ with respect to clock

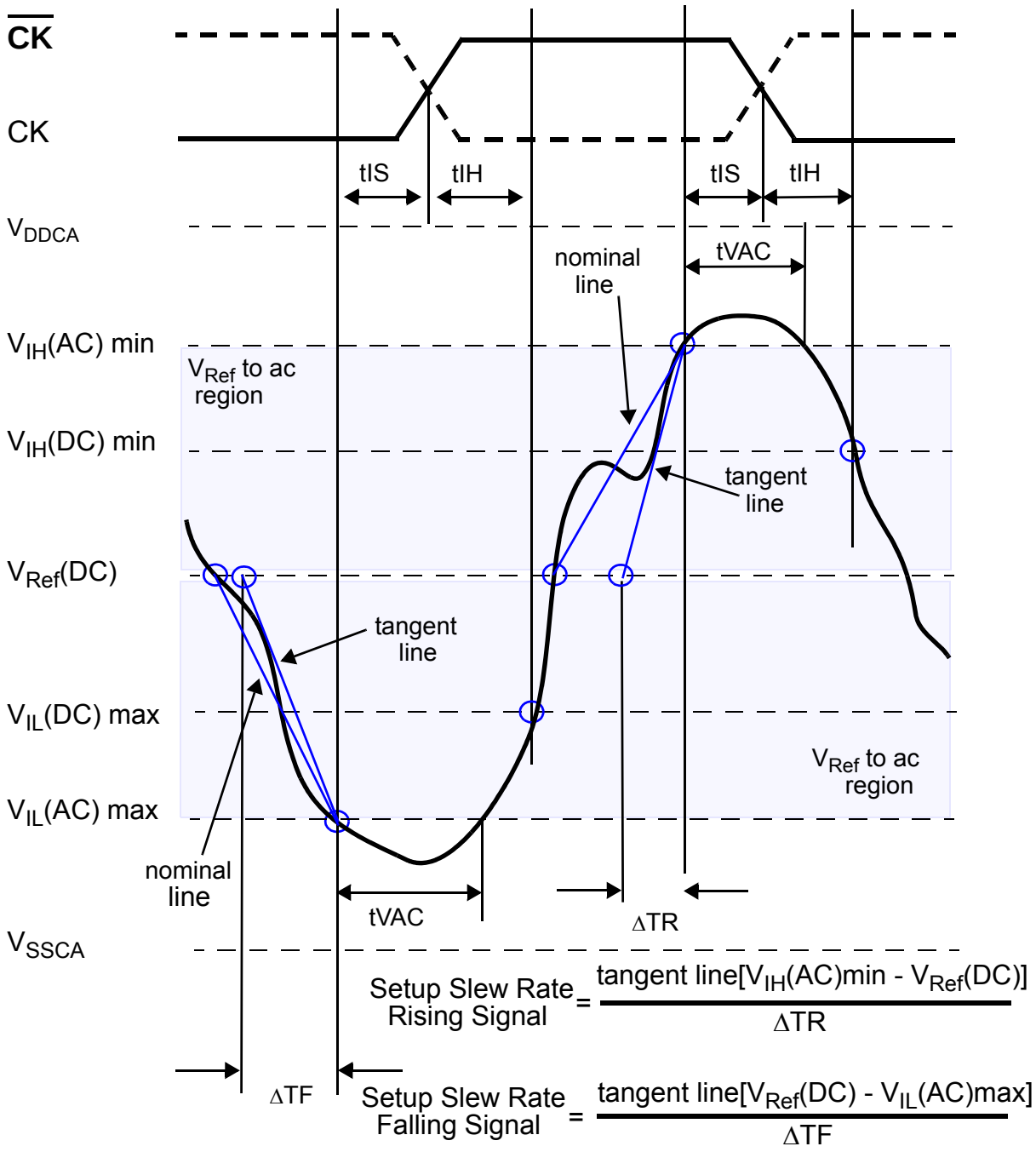
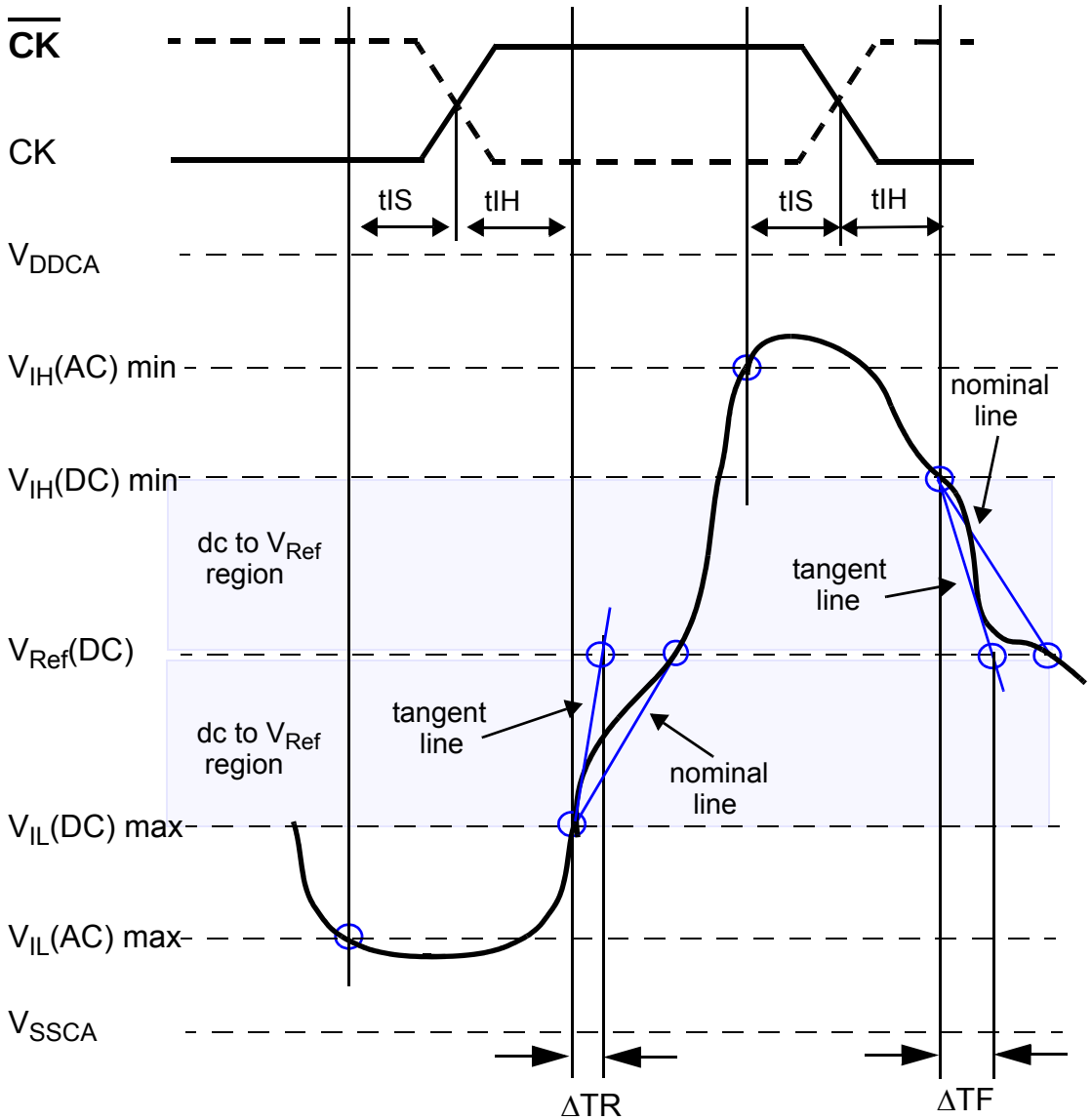


Figure 18. Illustration of tangent line for setup time t_{IS} for CA and $\overline{CS}$ with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)max \text{]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)min - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 19. Illustration of tangent line for hold time t_{IH} for CA and $\overline{CS}$ with respect to clock

11.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 49) to the ΔtDS and ΔtDH (see Table 50) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IH}(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{Ref}(DC) and the first crossing of V_{IL}(AC)max (see Figure 20 Illustration of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe). If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{Ref}(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{Ref}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 22 Illustration of tangent line for setup time tDS for DQ with respect to strobe).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC)max and the first crossing of V_{Ref}(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of V_{Ref}(DC) (see Figure 21 Illustration of nominal slew rate for hold time tDH for DQ with respect to strobe). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to V_{Ref}(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{Ref}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{Ref}(DC) level is used for derating value (see Figure 23 Illustration of tangent line for hold time tDH for DQ with respect to strobe).

For a valid transition the input signal has to remain above/below $V_{IH/IL}$(AC) for some time t_{VAC} (see Table 51).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization

[Table 49] Data Setup and Hold Base-Values

[ps]	LPDDR2	reference
	1066	
tDS(base)	-10	VIH/L(ac)=VRef(dc)+-220mV
tDH(base)	80	VIH/L(dc)=VRef(dc)+-130mV

NOTE :
1) ac/dc referenced for 1V/ns CA slew rate and 2V/ns differential DQS-$\overline{DQS}$ slew rate.

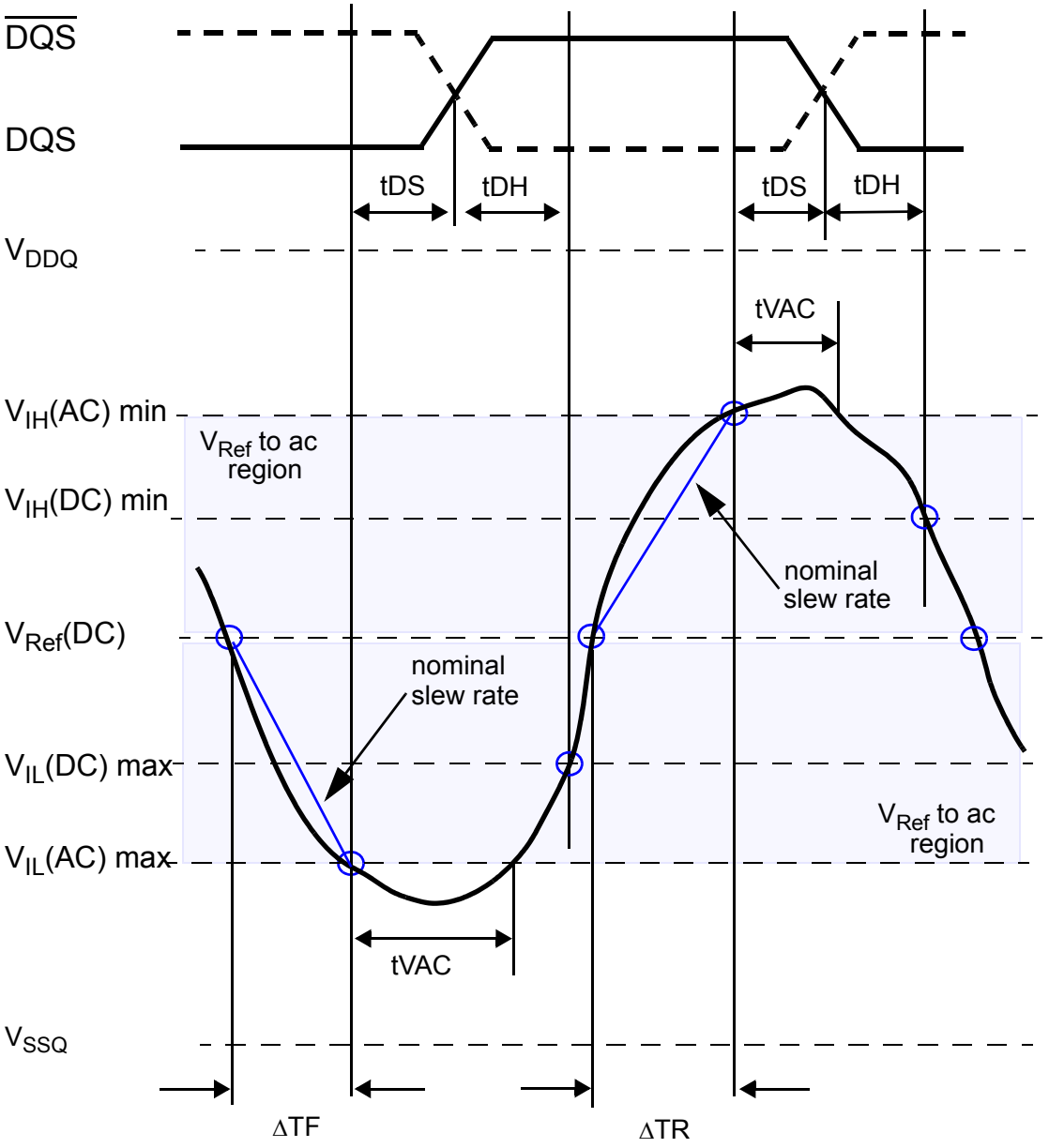
[Table 50] Derating values LPDDR2 tDS/tDH - ac/dc based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based[1)] AC220 Threshold -> $V_{IH}(AC)=V_{Ref}(DC)+220mV$, $V_{IL}(AC)=V_{Ref}(DC)-220mV$ DC130 Threshold -> $V_{IH}(DC)=V_{Ref}(DC)+130mV$, $V_{IL}(DC)=V_{Ref}(DC)-130mV$																	
		DQS, $\overline{DQS}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

NOTE :
1) Cell contents shaded in red are defined as 'not supported'.

[Table 51] Required time t_{VAC} above $V_{IH}(AC)$ {below $V_{IL}(AC)$} for valid transition

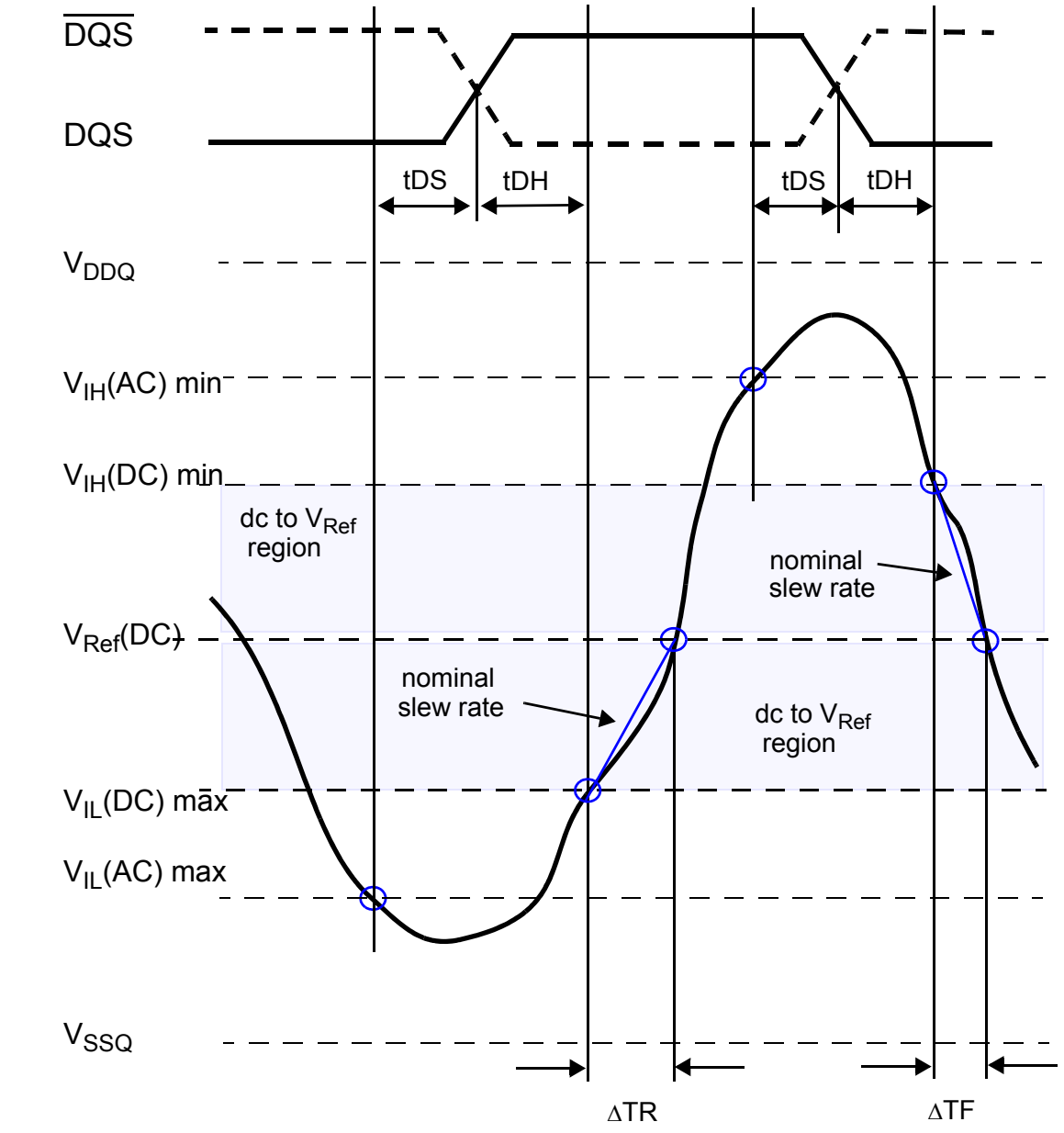
Slew Rate [V/ns]	t_{VAC} @ 220mV [ps]	
	min	max
> 2.0	175	-
2.0	170	-
1.5	167	-
1.0	163	-
0.9	162	-
0.8	161	-
0.7	159	-
0.6	155	-
0.5	150	-
< 0.5	150	-



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{Ref}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{Ref}(DC)}{\Delta TR}$$

Figure 20. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{Ref}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{Ref}(DC)}{\Delta TF}$$

Figure 21. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

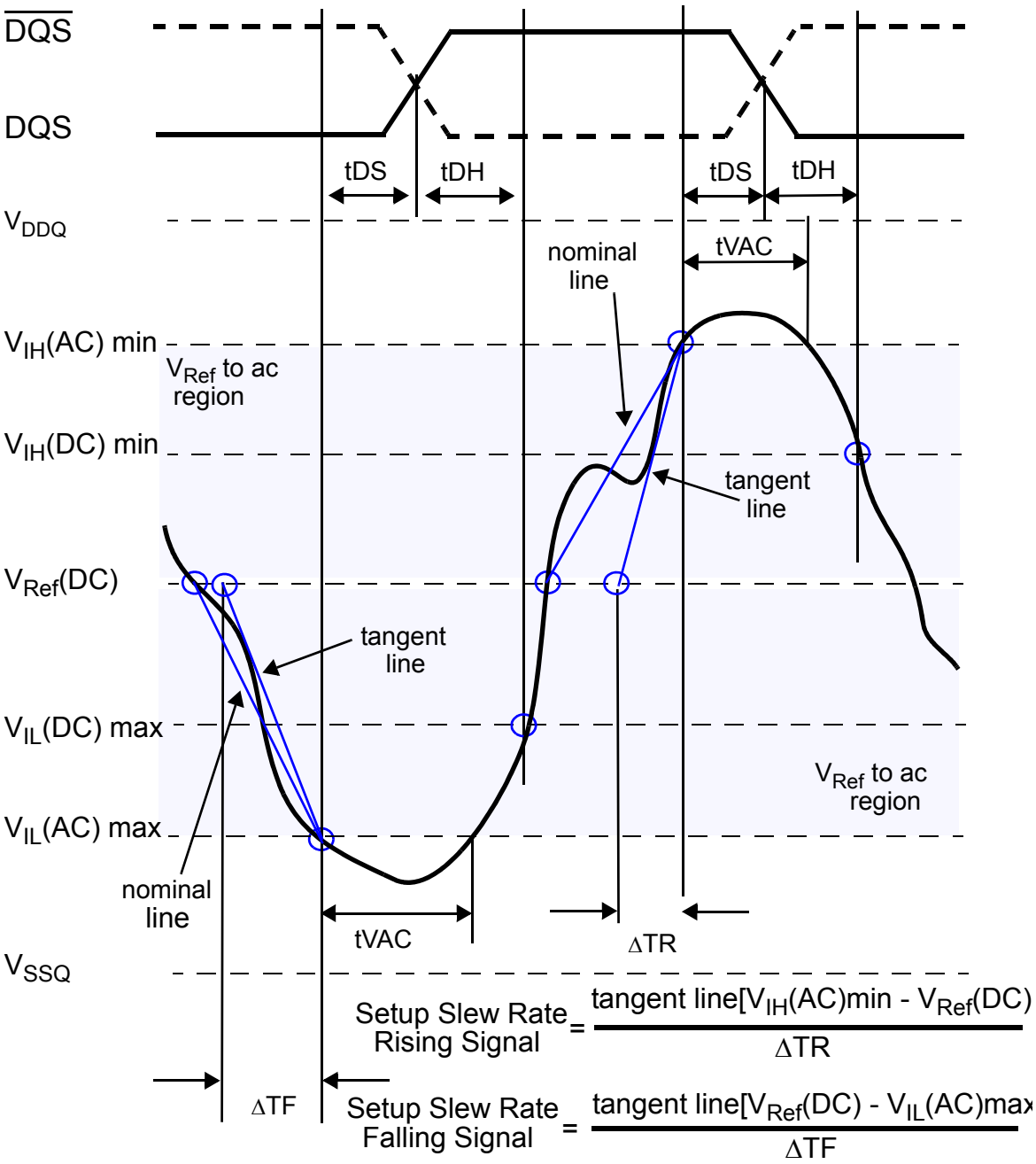
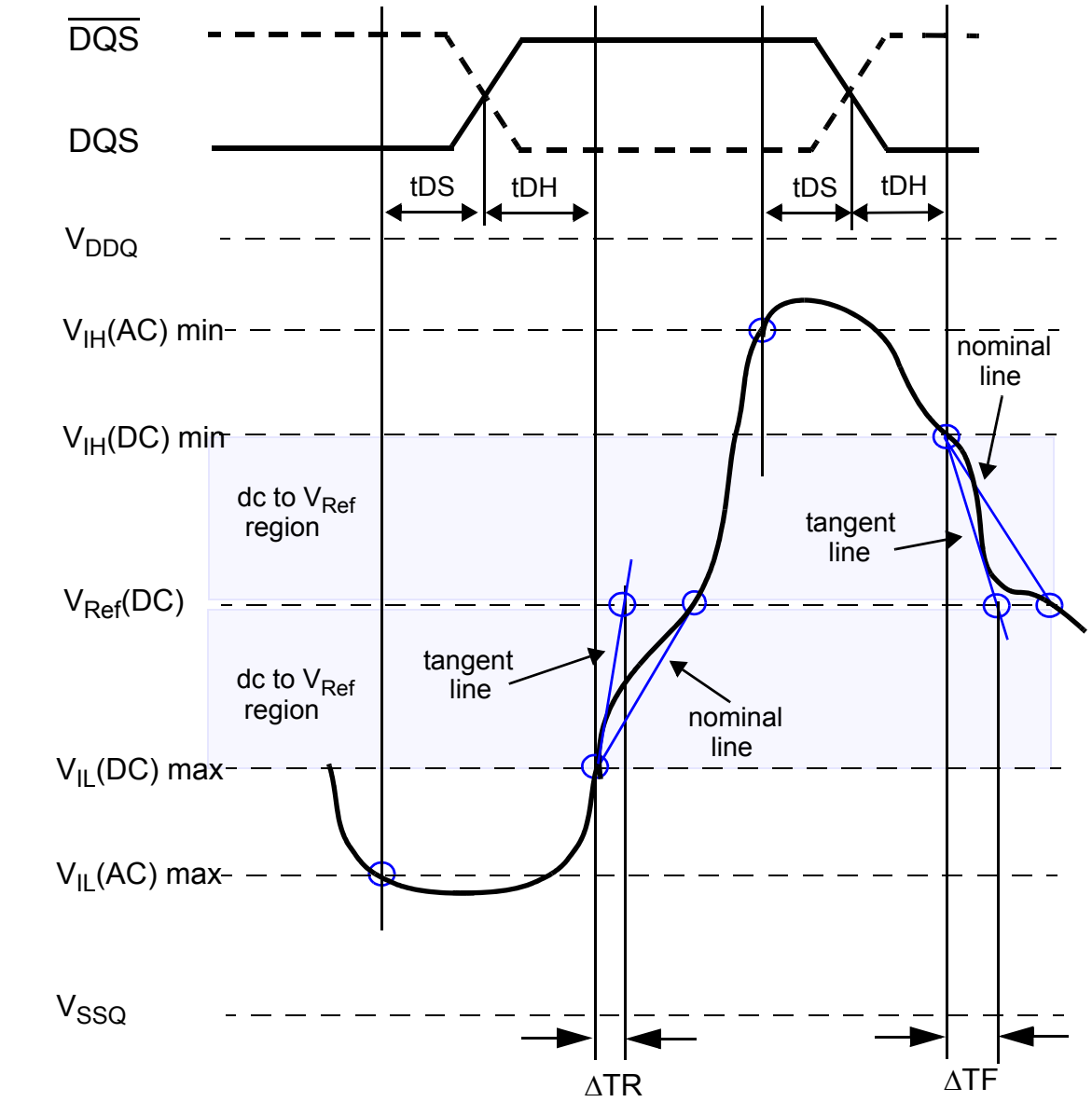


Figure 22. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [} V_{Ref}(DC) - V_{IL}(DC)max \text{]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [} V_{IH}(DC)min - V_{Ref}(DC) \text{]}}{\Delta TF}$$

Figure 23. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

LPDDR2 SDRAM Command Definitions and Timing Diagrams

LPDDR2 SDRAM Command Definitions and Timing Diagrams

1.0 POWER-UP, INITIALIZATION, AND POWER-OFF

LPDDR2 must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

1.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S4 devices.

1.1.1 Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=< 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.
On or before the completion of the power ramp (Tb) CKE must be held low.
DQ, DM, DQS, and $\overline{\text{DQS}}$ voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CK, $\overline{\text{CK}}$, $\overline{\text{CS}}$ and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

The following conditions apply:
Ta is the point where *any* power supply first reaches 300mV.
After Ta is reached, VDD1 must be greater than VDD2 - 200mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200mV.
After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200mV.
After Ta is reached, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.
The above conditions apply between Ta and power-off (controlled or uncontrolled).
Tb is the point when all supply voltages are within their respective min/max operating conditions.
Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.
For supply and reference voltage operating conditions, see Recommended LPDDR2 DC Operating Conditions on specific datasheet.
Power ramp duration t_{INIT0} (Tb - Ta) must be no greater than 20ms.

1.1.2 CKE and clock

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, $\overline{\text{CS}}$ and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 ns to 100 ns) if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 us. (Td).

1.1.3 Reset command

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least t_{INIT4} = 1 us while keeping CKE asserted and issuing NOP commands.

1.1.4 Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.
Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see Chapter 14).
The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.
As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.
After the DAI-bit (MR0, “DAI”) is set to zero “DAI complete“ by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0.
All SDRAM devices will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

1.1.5 ZQ Calibration:

After t_{INIT5} (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. The MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

1.1.6 Normal Operation:

After t_{ZQINIT} (Tg), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.
The LPDDR2 device will now be in IDLE state and ready for any valid command.
After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section Chapter 16 of this specification.

[Table 1] Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	100		ns	Minimum CKE low time after completion of power ramp
t_{INIT2}	5		tCK	Minimum stable clock before first CKE high
t_{INIT3}	200		µs	Minimum Idle time after first CKE assertion
t_{INIT4}	1		µs	Minimum Idle time after Reset command.
t_{INIT5}		10	µs	Maximum duration of Device Auto-Initialization
t_{ZQINIT}	1		µs	ZQ Initial Calibration
t_{CKb}	18	100	ns	Clock cycle time during boot

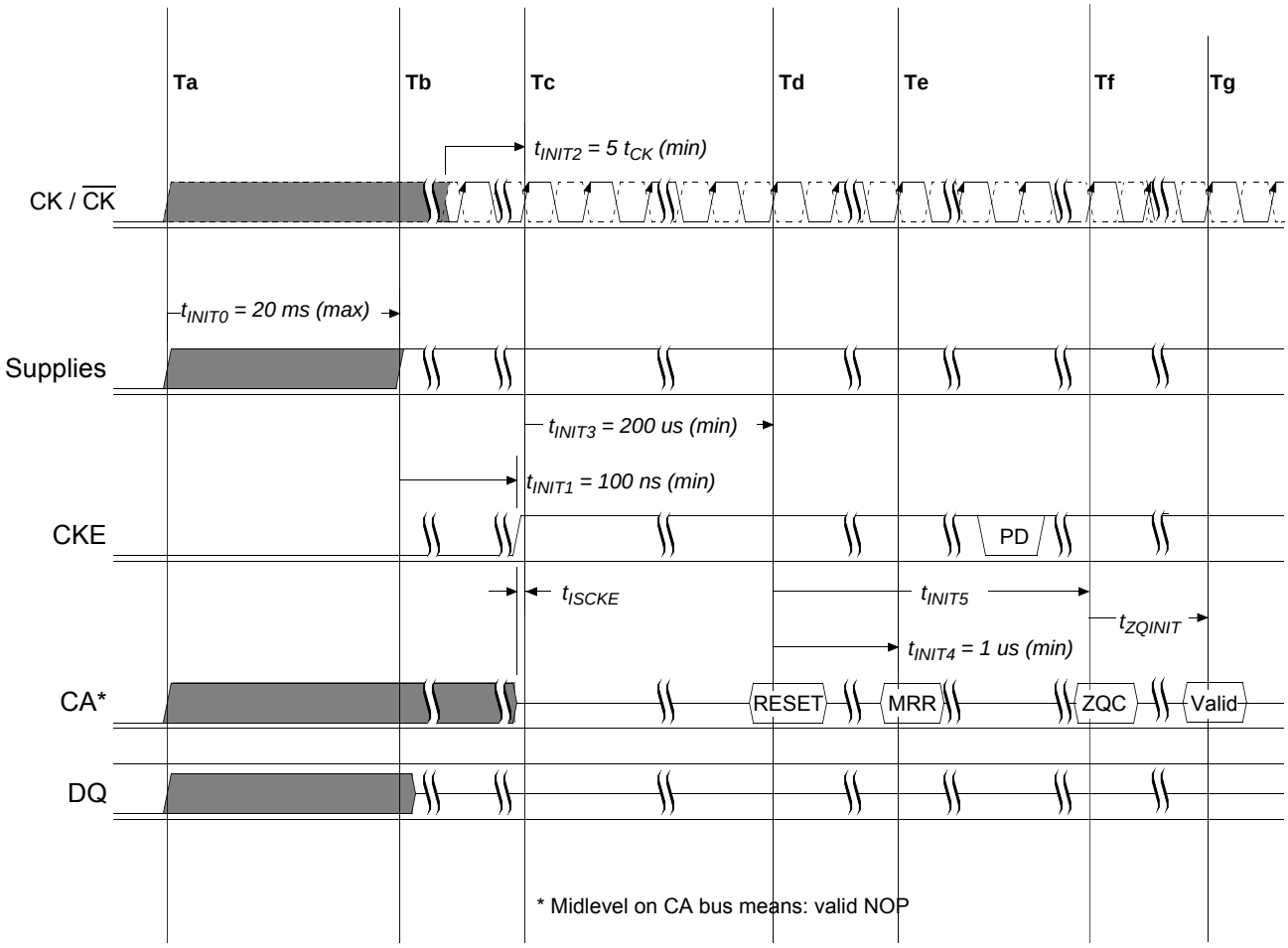


Figure 1: Power Ramp and Initialization Sequence

1.2 Initialization after Reset (without Power ramp):

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

1.3 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory.

While removing power, CKE shall be held at a logic low level (=< 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS, and $\overline{DQS}$ voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK, $\overline{CK}$,$\overline{CS}$ and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

Tx is the point where *any* power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where *all* power supply first reaches 300mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDCA - 200mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended LPDDR2 DC Operating Conditions on specific datasheet..

[Table 2] Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

1.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition. Unless specified otherwise, these steps are mandatory.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300mV. After Tz, the device is powered off.

The time between Tx and Tz(t_{POFF}) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

2.0 ACTIVATE COMMAND

2.1 LPDDR2-S4: Activate Command

The SDRAM Activate command is issued by holding $\overline{CS}$ LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time t_{RCD} after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD}.

Any system or application incorporating random access memory products should be properly designed, tested and qulifided to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

• 8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW}[ns] by t_{CK}[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (t_{FAW} / t_{CK}) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of t_{FAW}.

• 8-bank device Precharge All Allowance : t_{RP} for a Precharge All command for an 8-bank device shall equal t_{RPab}, which is greater than t_{RPpb}.

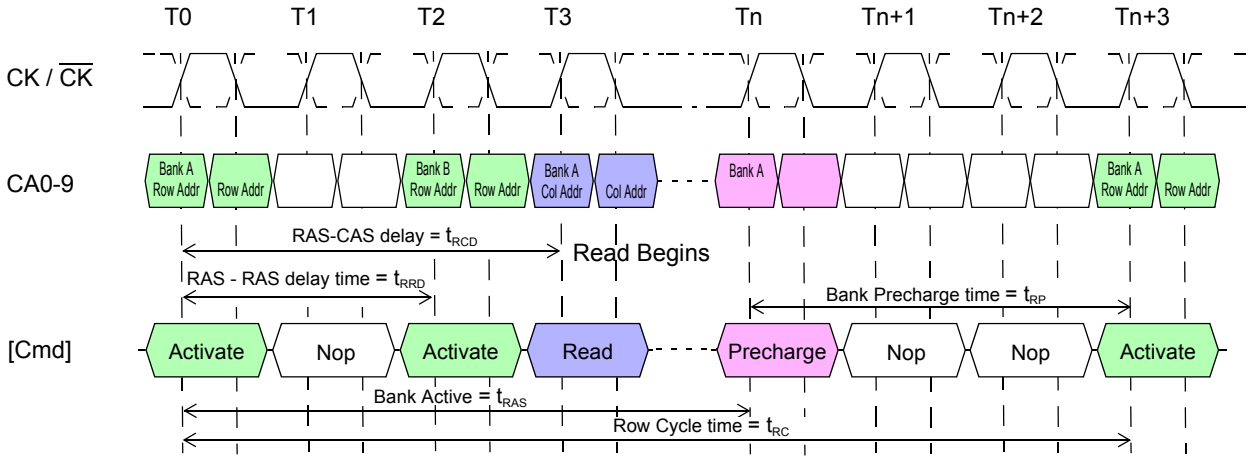


Figure 2: LPDDR2-S4: Activate command cycle: t_{RCD} = 3, t_{RP} = 3, t_{RRD} = 2

NOTE :
1) A Precharge-All command uses t_{RPab} timing, while a Single Bank Precharge command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an All-bank Precharge or a Single Bank Precharge.

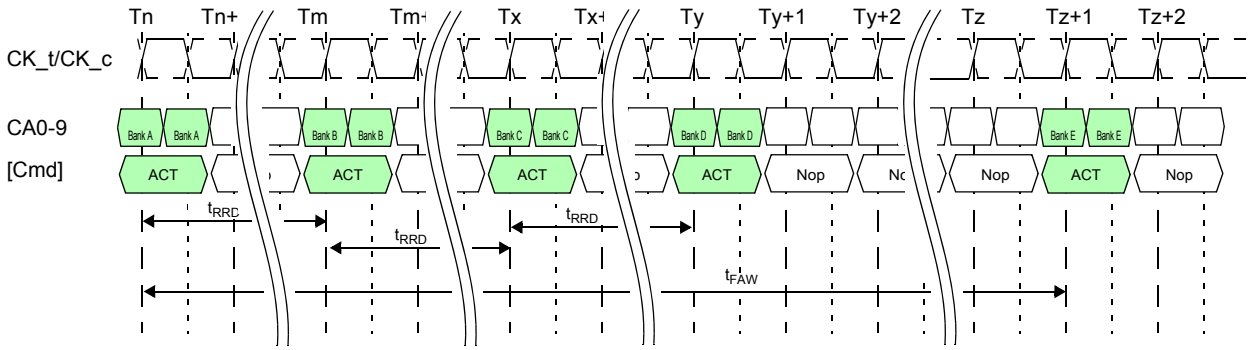


Figure 3: LPDDR2-S4: t_{FAW} timing

NOTE :
1) For 8-bank devices only. No more than 4 banks may be activated in a rolling t_{FAW} window.

3.0 LPDDR2 COMMAND INPUT SETUP AND HOLD TIMING

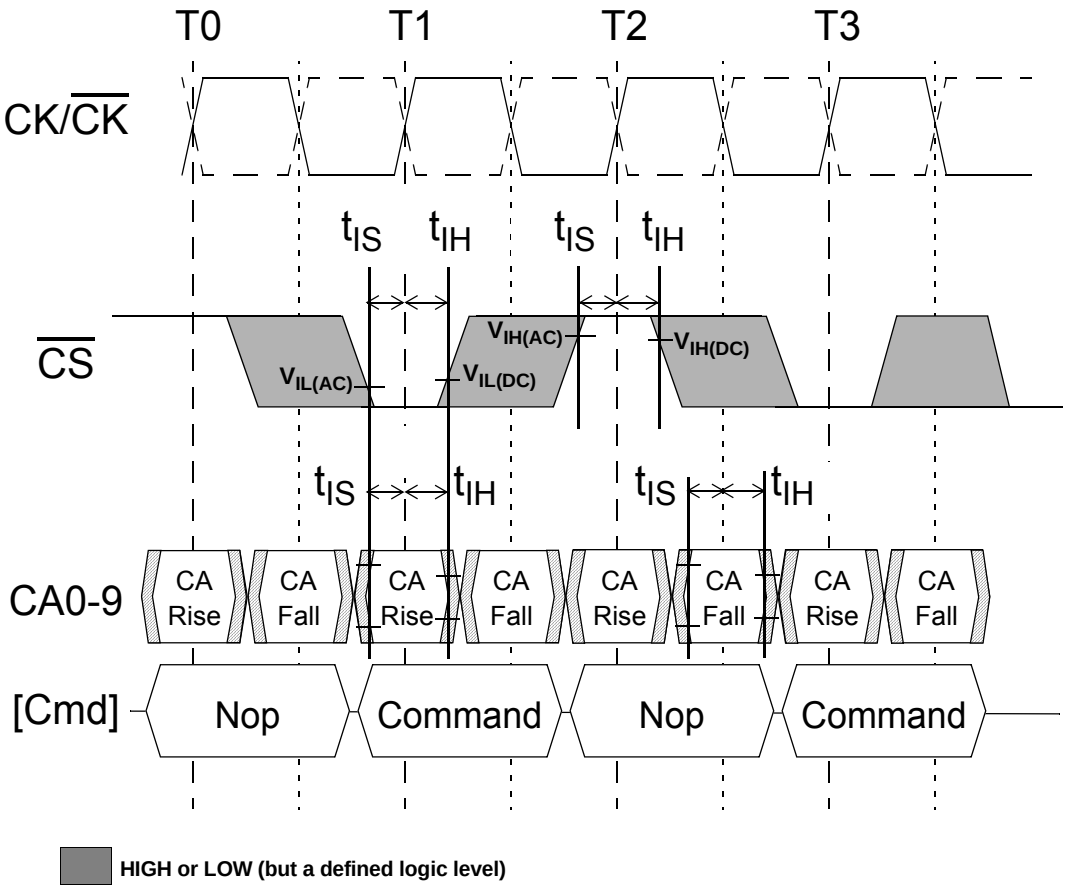


Figure 4: LPDDR2 : Command Input Setup and Hold Timing

NOTE :
1) Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

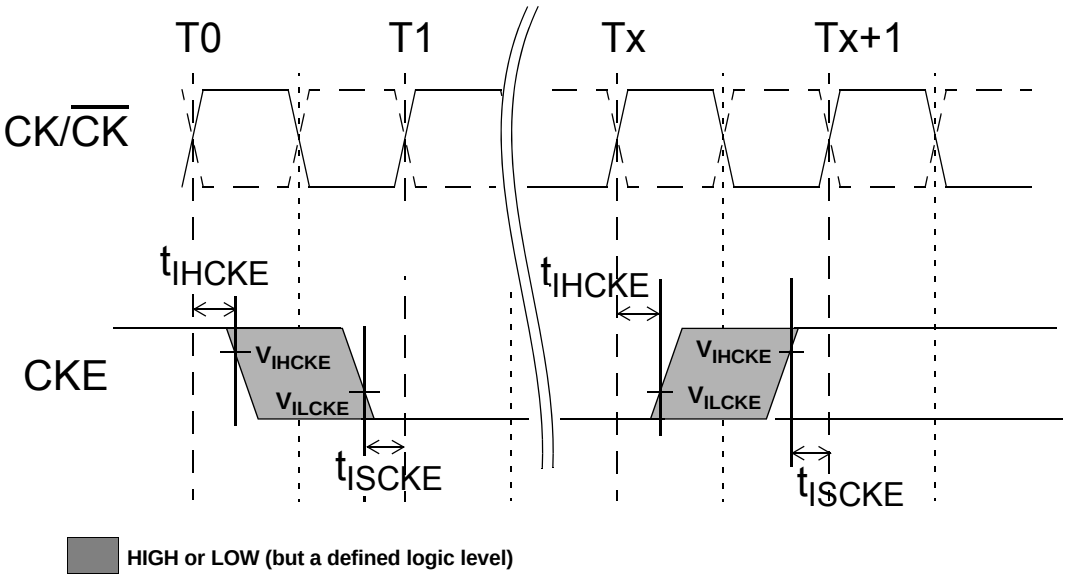


Figure 5: LPDDR2 : CKE Input Setup and Hold Timing

NOTE :
1) After CKE is registered LOW, CKE signal level shall be maintained below VIL CKE for tCKE specification (LOW pulse width).
2) After CKE is registered HIGH, CKE signal level shall be maintained above VIH CKE for tCKE specification (HIGH pulse width).

4.0 READ AND WRITE ACCESS MODES

4.1 LPDDR2-S4: Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{CS}$ LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a read operation (CA2 HIGH) or a write operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and t_{CCD} is met.

5.0 BURST READ COMMAND

The Burst Read command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the t_{DQSCK} delay is measured. The first valid datum is available RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW t_{RPRE} before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

Timings for the data strobe are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$.

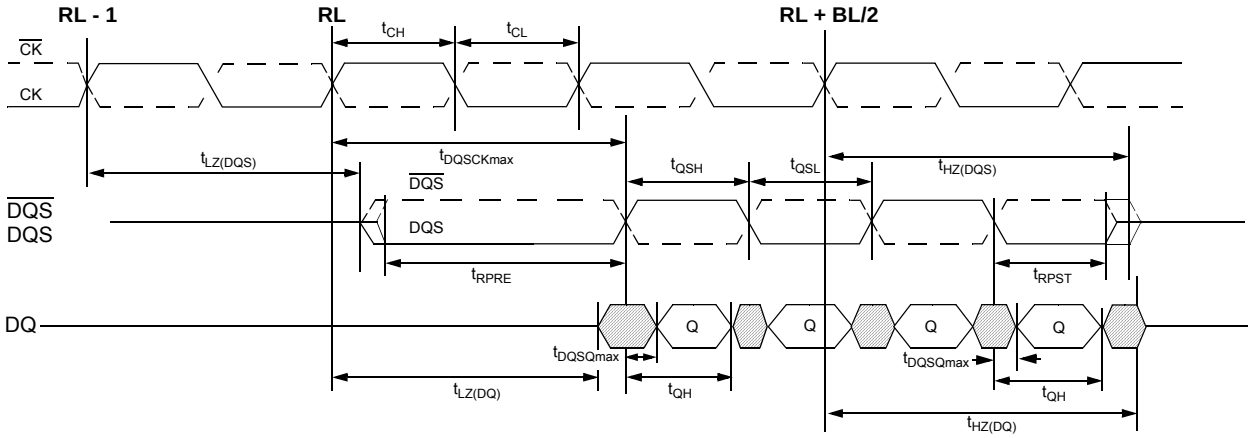


Figure 6: Data output (read) timing ($t_{DQSCKmax}$)

NOTE :
1) t_{DQSCK} may span multiple clock periods.
2) An effective Burst Length of 4 is shown.

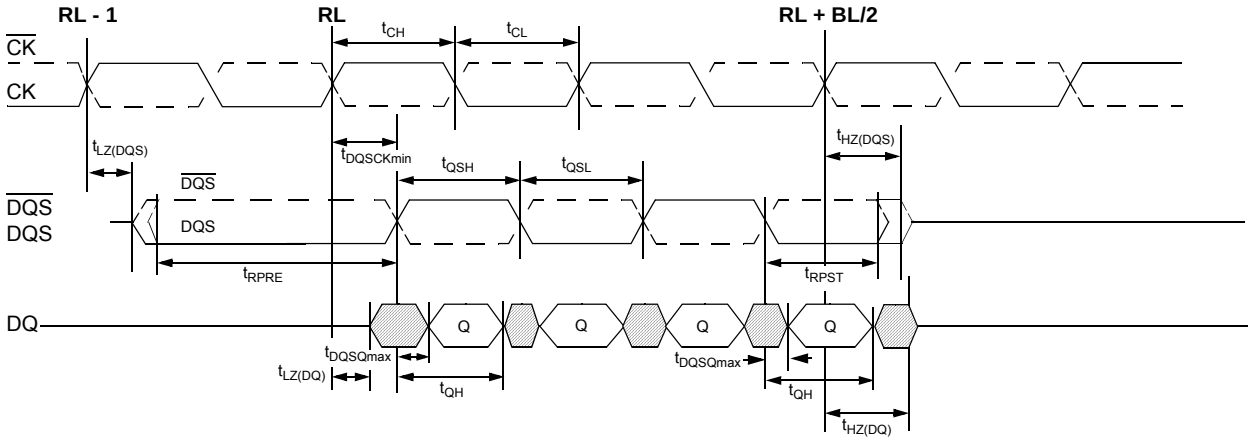


Figure 7: Data output (read) timing ($t_{DQSCKmin}$)

NOTE :
1) An effective Burst Length of 4 is shown.

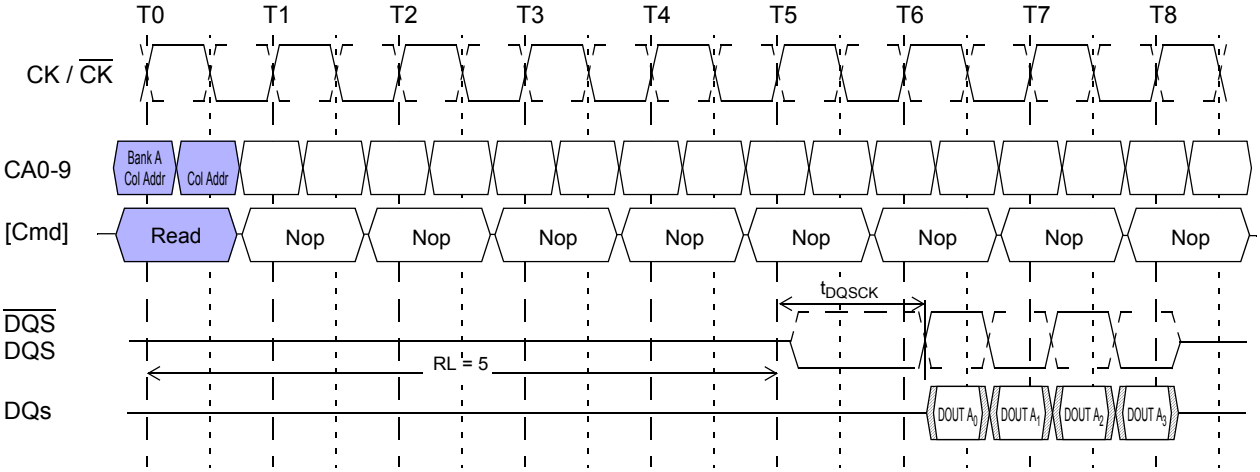


Figure 8: LPDDR2-S4: Burst read: RL = 5, BL = 4, $t_{DQSCK} > t_{CK}$

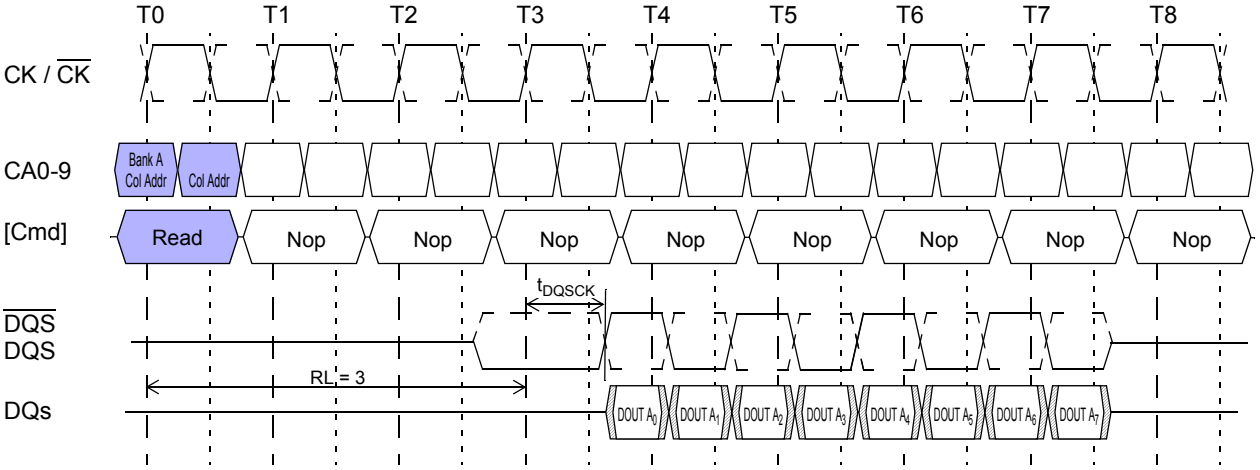


Figure 9: LPDDR2-S4: Burst read: RL = 3, BL = 8, $t_{DQSCK} < t_{CK}$

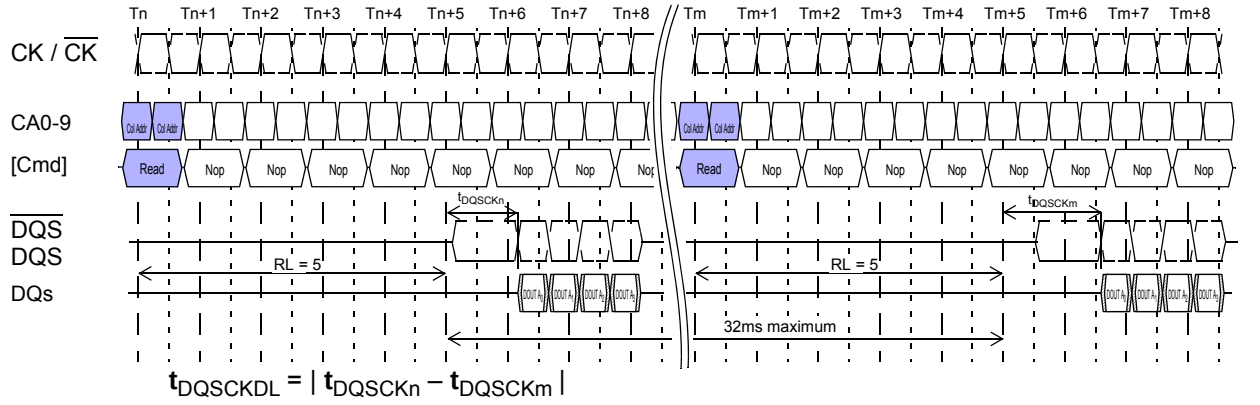


Figure 10: LPDDR2: $t_{DQSCKDL}$ timing

NOTE :

1) $t_{DQSCKDLmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair within any 32ms rolling window.

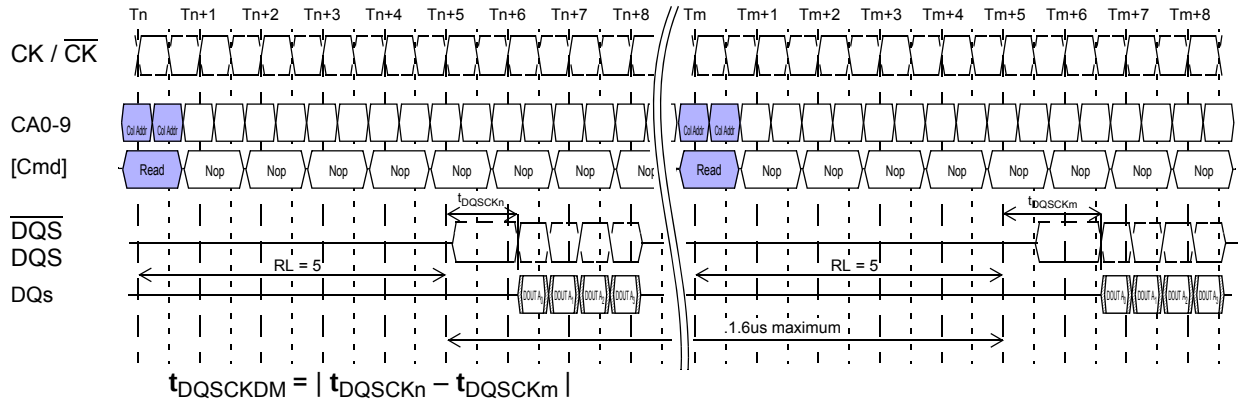


Figure 11: LPDDR2: $t_{DQSCKDM}$ timing

NOTE :
1) $t_{DQSCKDMmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn},t_{DQSCKm}} pair within any 1.6us rolling window.

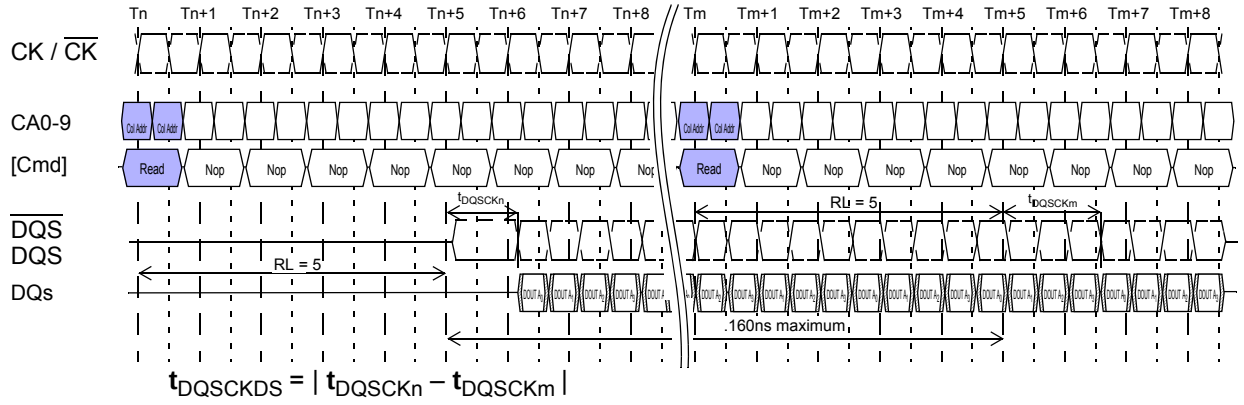


Figure 12: LPDDR2: $t_{DQSCKDS}$ timing

NOTE :
1) $t_{DQSCKDSmax}$ is defined as the maximum of ABS(t_{DQSCKn} - t_{DQSCKm}) for any {t_{DQSCKn} ,t_{DQSCKm}} pair for reads within a consectutive burst within any 160ns rolling window.

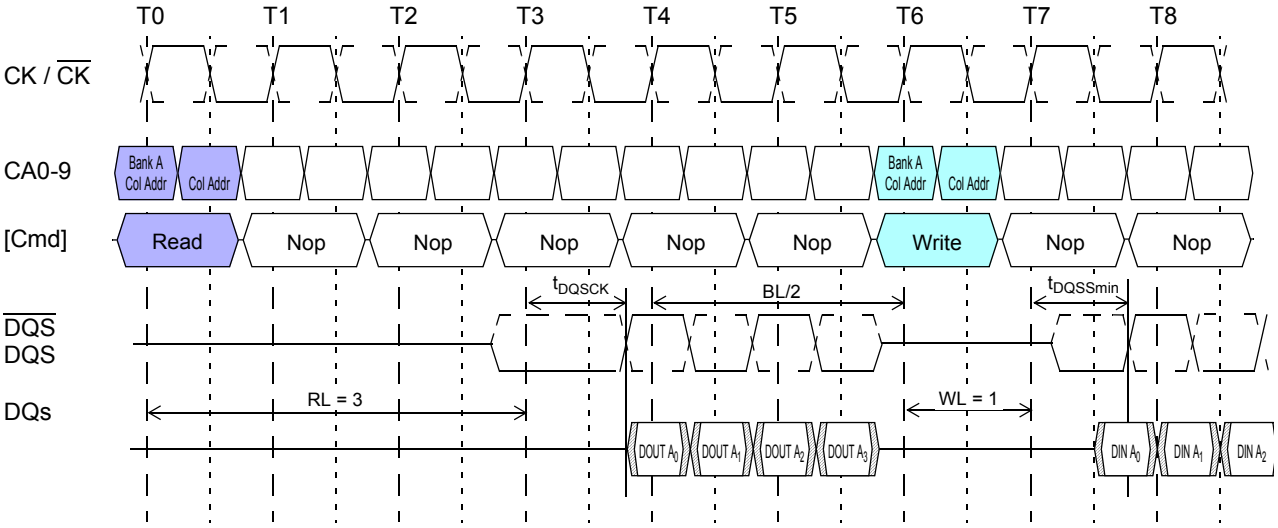


Figure 13: LPDDR2-S4: Burst read followed by burst write: RL = 3, WL = 1, BL = 4

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(t_{DQSCK}max/t_{CK}) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

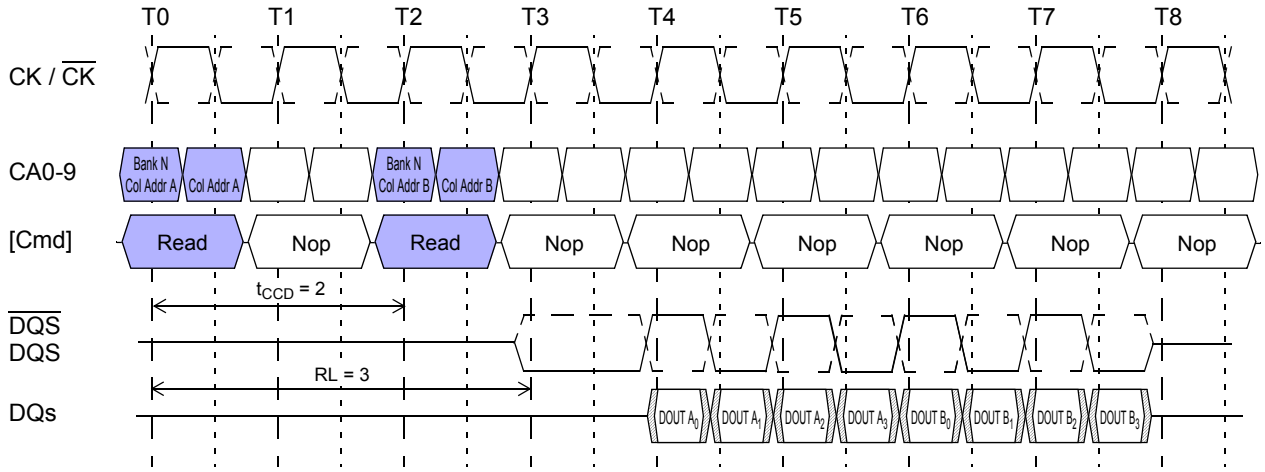


Figure 14: LPDDR2-S4: Seamless burst read: RL = 3, BL = 4, t_{CCD} = 2

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

5.1 Reads interrupted by a read

For LPDDR2-S4 devices, burst read can be interrupted by another read on even clock cycles after the Read command provided that t_{CCD} is met.

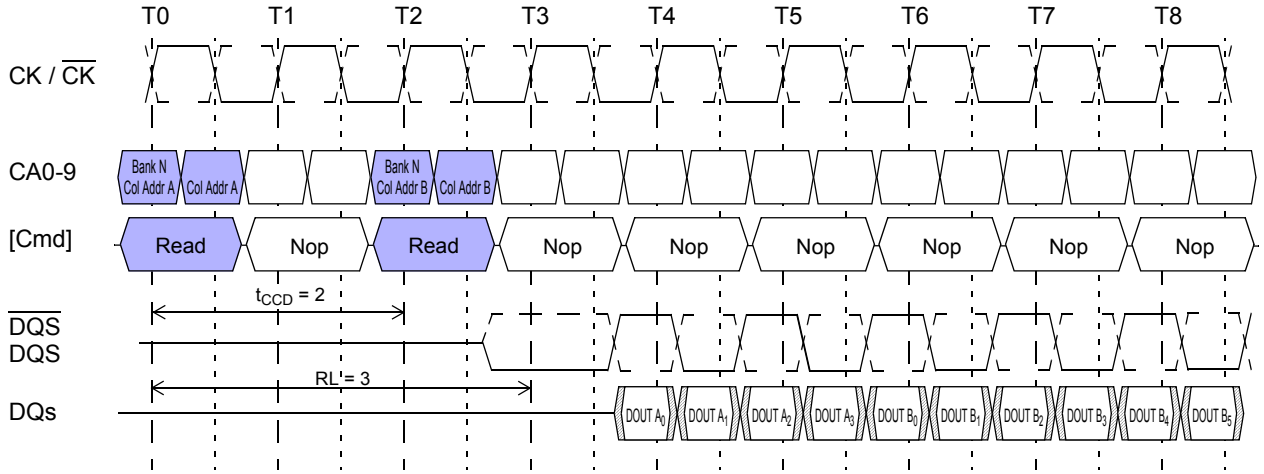


Figure 15: LPDDR2-S4: Read burst interrupt example: RL = 3, BL = 8, t_{CCD} = 2

NOTE :
1) For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2) For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that t_{CCD} is met.
3) Reads can only be interrupted by other reads or the BST command.
4) Read burst interruption is allowed to any bank inside DRAM.
5) Read burst with Auto-Precharge is not allowed to be interrupted.
6) The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

6.0 BURST WRITE OPERATION

The Burst Write command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the t_{DQSS} delay is measured. The first valid datum shall be driven WL * t_{CK} + t_{DQSS} from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW t_{WPRE} prior to the data input. The data bits of the burst cycle must be applied to the DQ pins t_{DS} prior to the respective edge of the DQS, $\overline{DQS}$ and held valid until t_{DH} after that edge. The burst data are sampled on successive edges of the DQS $\overline{DQS}$ until the burst length is completed, which is 4, 8, or 16 bit burst.

For LPDDR2-SDRAM devices, t_{WR} must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

Input timings are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$.

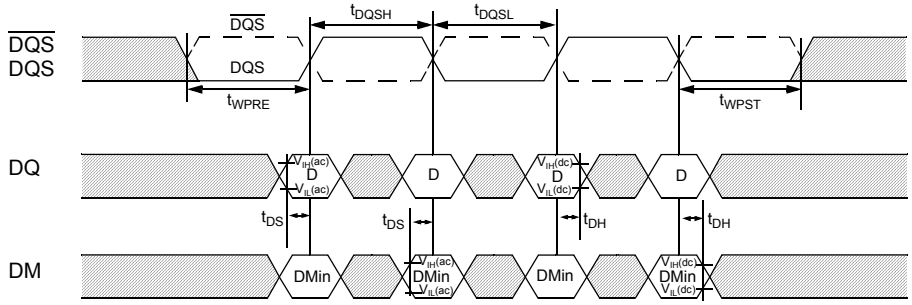


Figure 16: Data input (write) timing

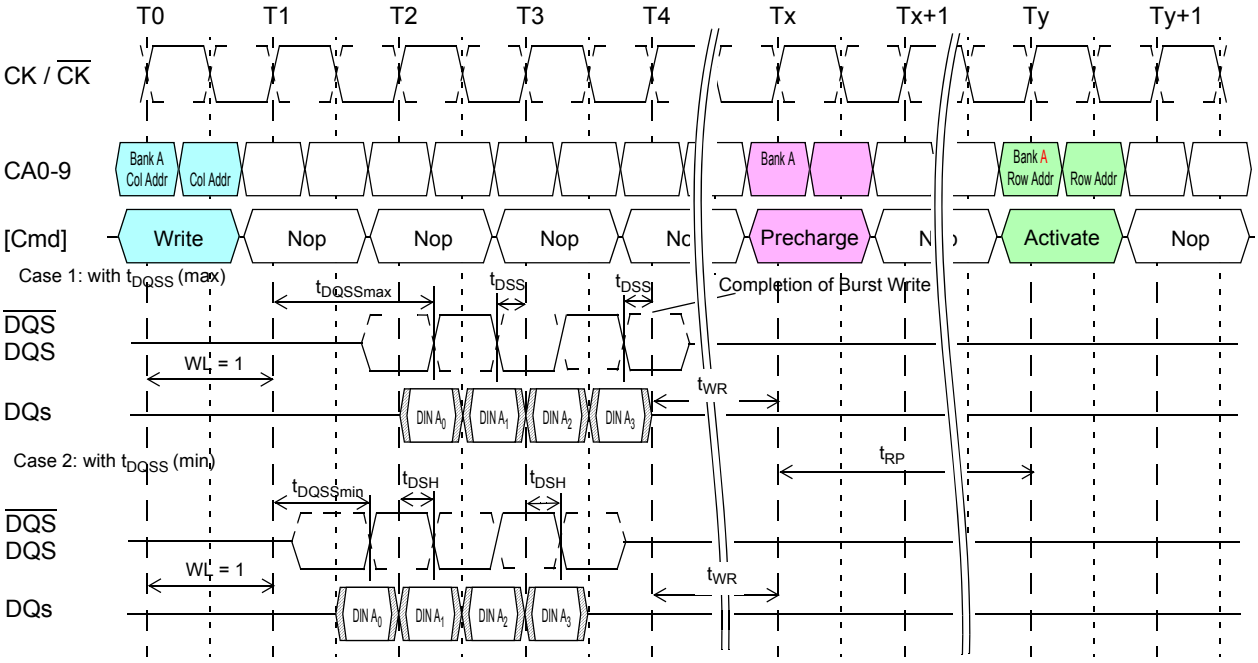


Figure 17: LPDDR2-S4: Burst write : WL = 1, BL = 4

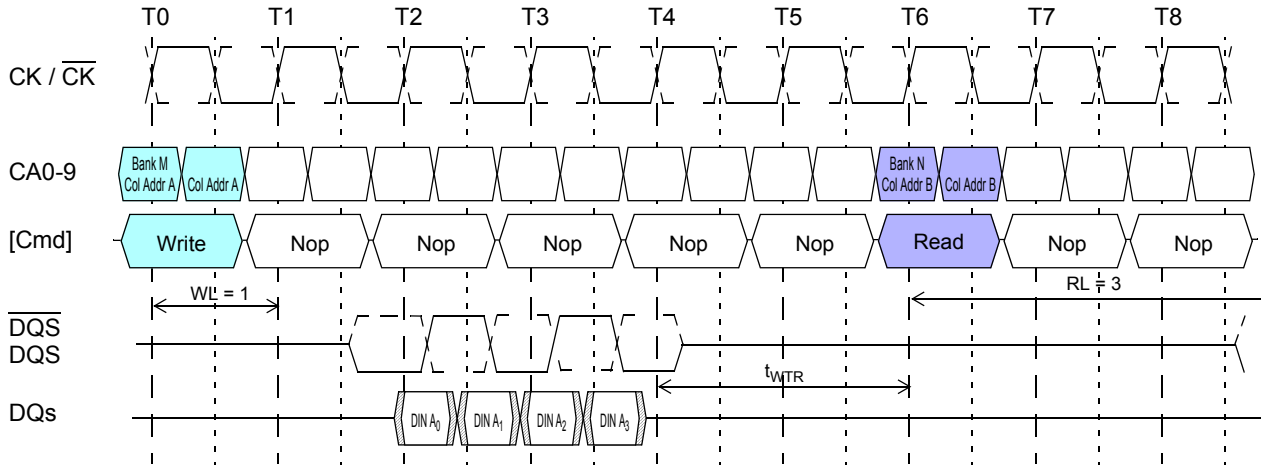


Figure 18: LPDDR2-S4: Burst write followed by burst read: RL=3, WL = 1, BL = 4

NOTE :

1) The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})].

2) t_{WTR} starts at the rising edge of the clock after the last valid input datum.

3) If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

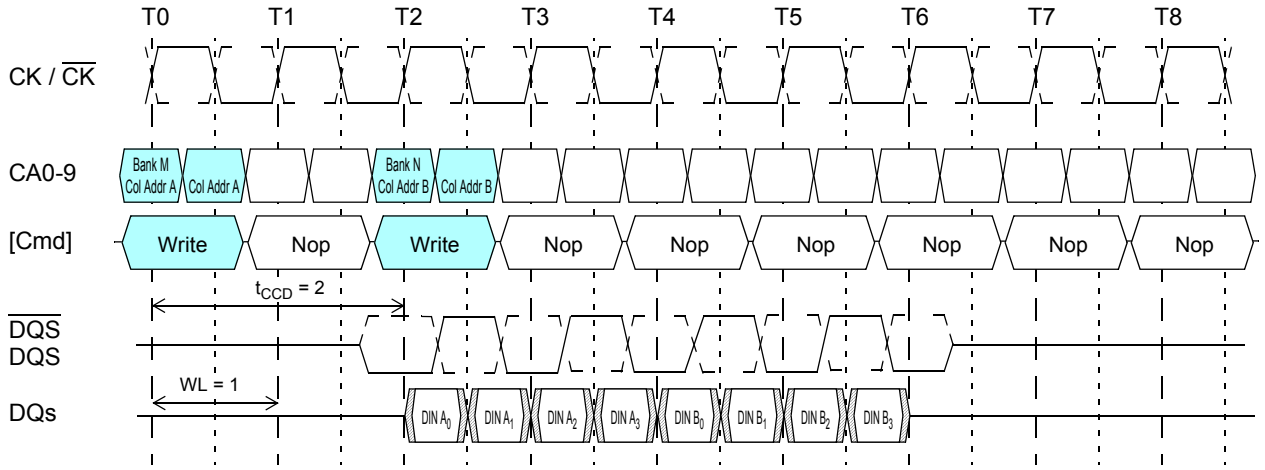


Figure 19: LPDDR2-S4: Seamless burst write: WL = 1, BL = 4, t_{CCD} = 2

NOTE :

1) The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

6.1 Writes interrupted by a write

For LPDDR2-S4 devices, burst write can only be interrupted by another write on even clock cycles after the Write command, provided that tCCD(min) is met.

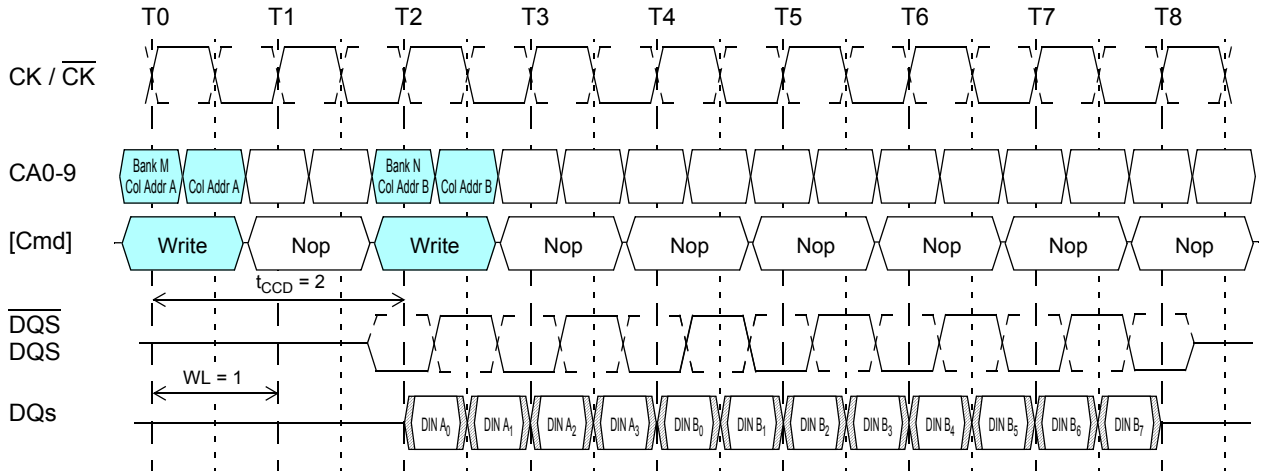


Figure 20: LPDDR2-S4: Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2

NOTE :
1) For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2) For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.
3) Writes can only be interrupted by other writes or the BST command.
4) Write burst interruption is allowed to any bank inside DRAM.
5) Write burst with Auto-Precharge is not allowed to be interrupted.
6) The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

7.0 BURST TERMINATE

The Burst Terminate (BST) command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as "BL" to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

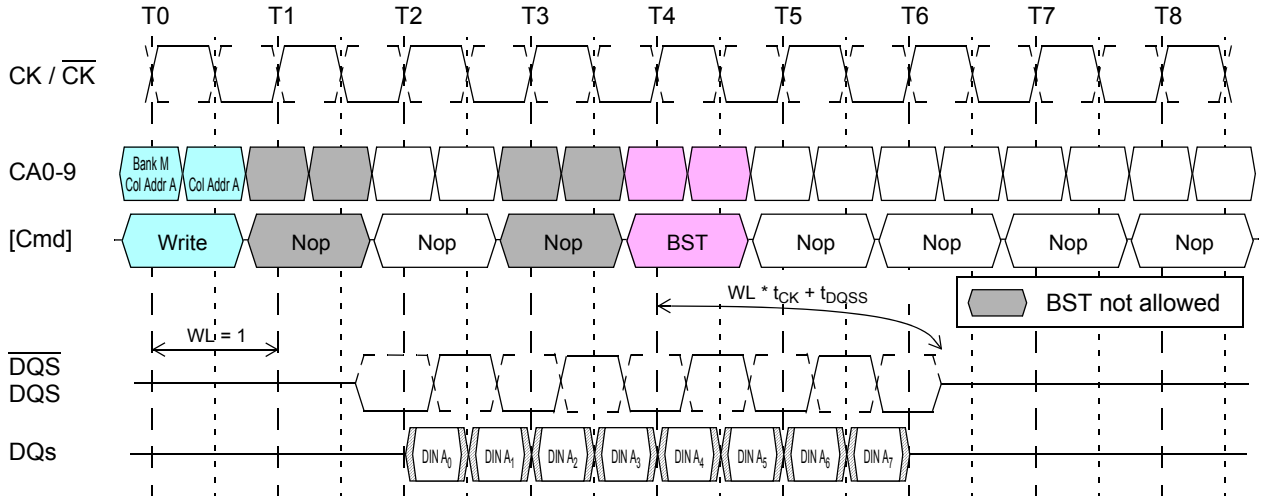


Figure 21: LPDDR2-S4: Burst Write truncated by BST: WL = 1, BL = 16

NOTE :
1)The BST command truncates an ongoing write burst WL * t_{CK} + t_{DQSS} after the rising edge of the clock where the Burst Terminate command is issued.
2) For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3) Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

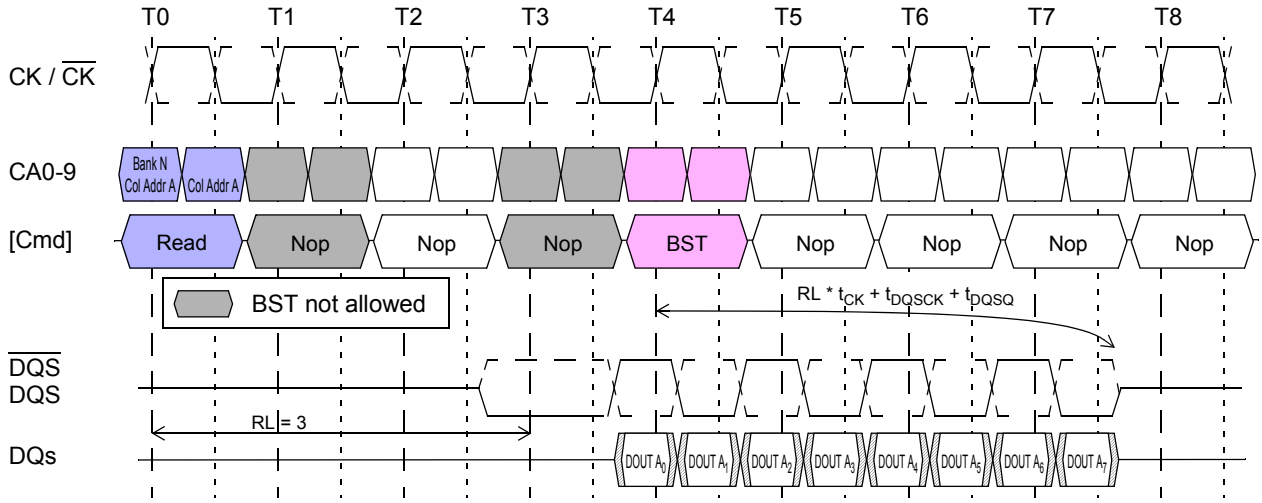


Figure 22: LPDDR2-S4: Burst Read truncated by BST: RL=3, BL = 16

NOTE :
1) The BST command truncates an ongoing read burst RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Burst Terminate command is issued.
2) For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3) Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

8.0 WRITE DATA MASK

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on Mobile DDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

See Table 4 for Write to Precharge timings for LPDDR2-S4.

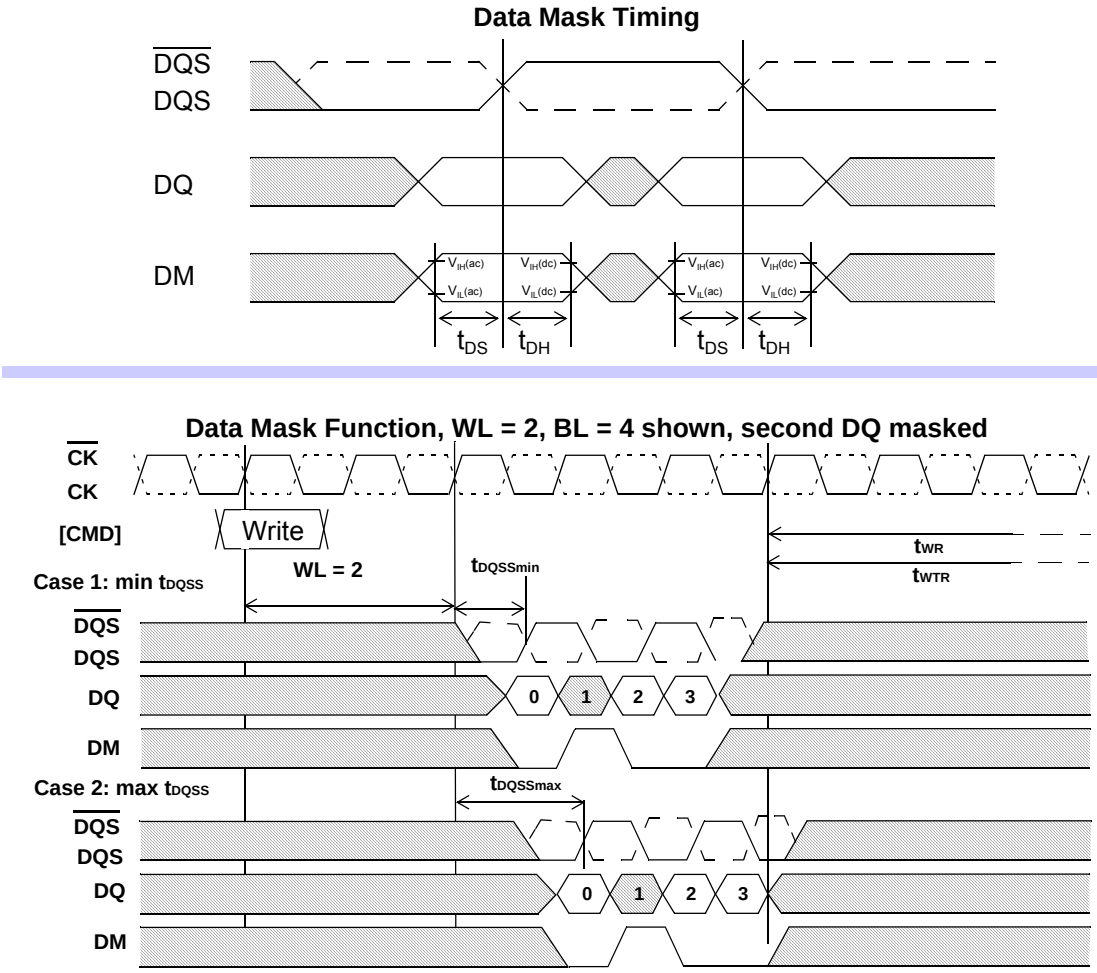


Figure 23: LPDDR2-S4: Write data mask

9.0 LPDDR2-S4 : PRECHARGE OPERATION

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices , the AB flag, and the bank address bits, BA0 and BA1, are used to determine which bank(s) to precharge. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access t_{RPab} after an All-Bank Precharge command is issued and t_{RPpb} after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge for 8-bank devices (t_{RPab}) will be longer than the Row Precharge time for a Single-Bank Precharge (t_{RPpb}). For 4-bank devices, the Row Precharge time (t_{RP}) for an All-Bank Precharge (t_{RPab}) is equal to the Row Precharge time for a Single-Bank Precharge (t_{RPpb}).

Figure 2 shows Activate to Precharge timing.

[Table 3] Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only	Bank 0 only
0	0	0	1	Bank 1 only	Bank 1 only
0	0	1	0	Bank 2 only	Bank 2 only
0	0	1	1	Bank 3 only	Bank 3 only
0	1	0	0	Bank 0 only	Bank 4 only
0	1	0	1	Bank 1 only	Bank 5 only
0	1	1	0	Bank 2 only	Bank 6 only
0	1	1	1	Bank 3 only	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks	All Banks

9.1 LPDDR2-S4: Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command cannot be issued until after tRAS is satisfied.
For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command. This time is called tRTP (Read to Precharge).

For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, the effective "BL" shall be used to calculate when tRTP begins.

See Table 4 for Read to Precharge timings for LPDDR2-S4.

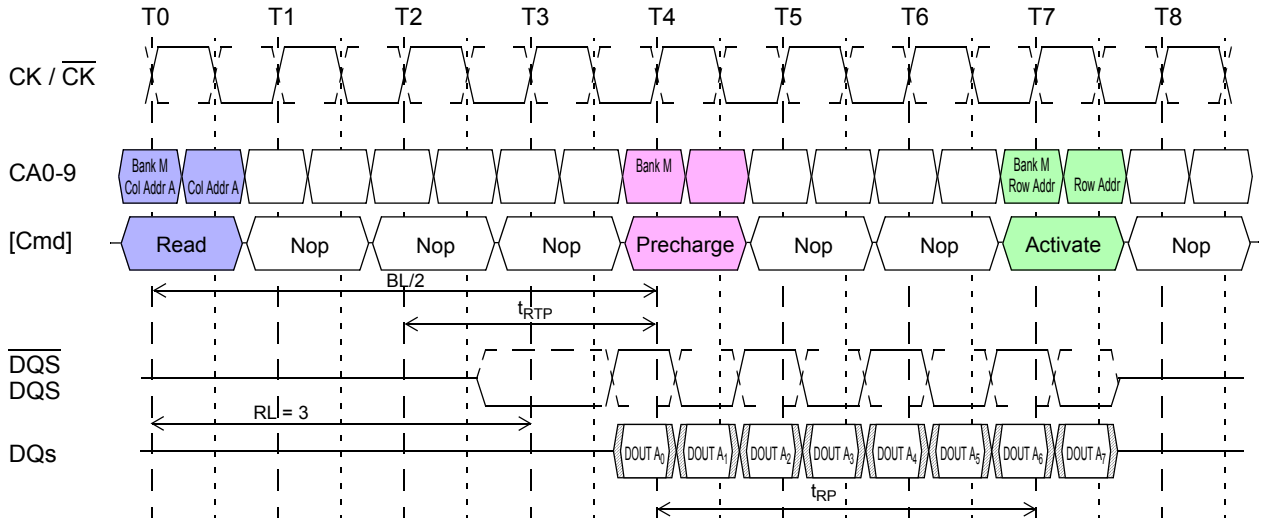


Figure 24: LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL = 8, RU(t_{RTP}(min)/ t_{CK}) = 2

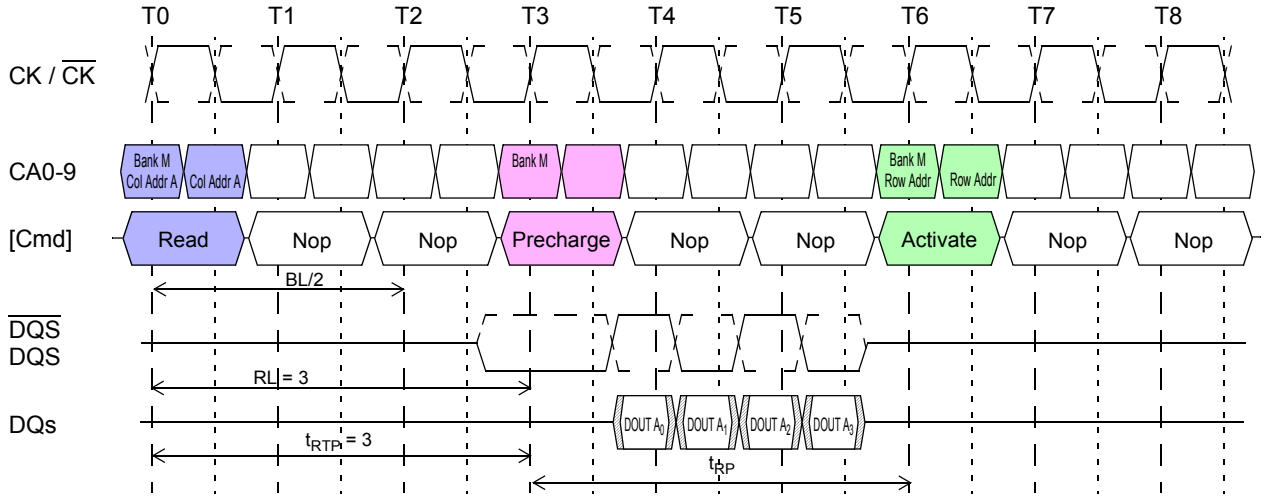


Figure 25: LPDDR2-S4: Burst read followed by Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 3

9.2 LPDDR2-S4: Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (t_{WR}) referenced from the completion of the burst write to the precharge command. No Precharge command to the same bank should be issued prior to the t_{WR} delay.

LPDDR2-S4 devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely.

For LPDDR2-S4 devices, minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(t_{WR}/t_{CK}) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

See Table 4 for Write to Precharge timings for LPDDR2-S4.

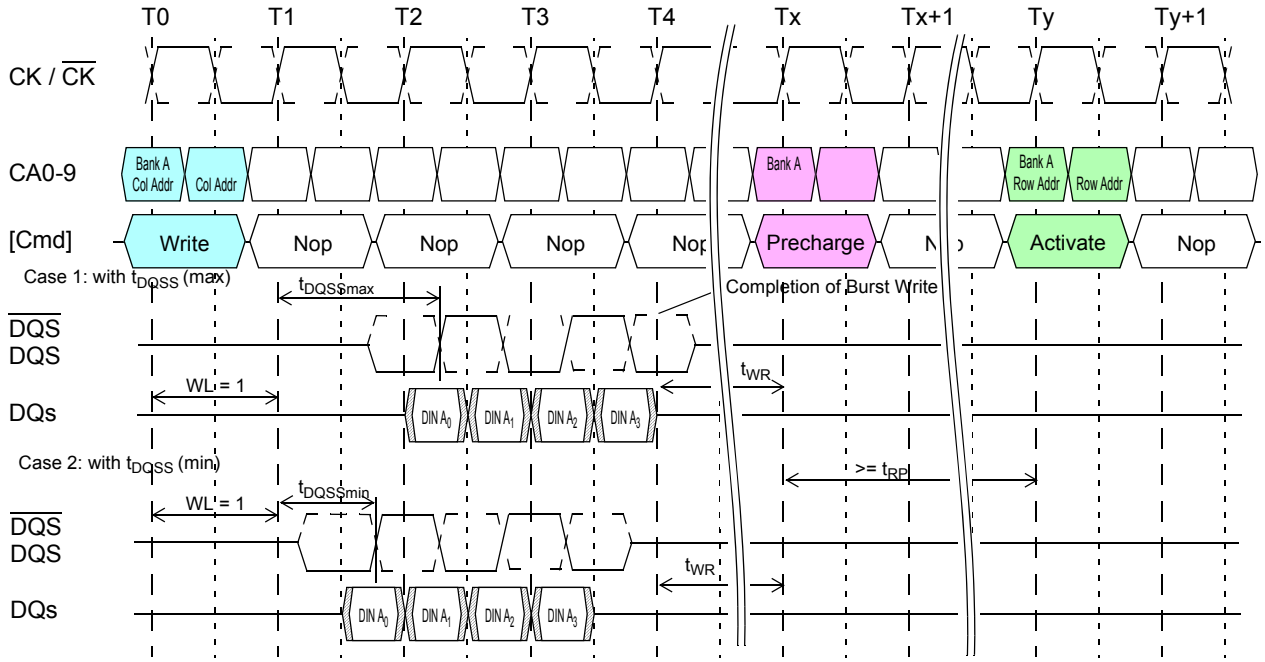


Figure 26: LPDDR2-S4: Burst write followed by precharge: WL = 1, BL = 4

9.3 LPDDR2-S4: Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

9.4 LPDDR2-S4: Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged.

LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(t_{RTP}/t_{CK}) clock cycles later than the Read with AP command, whichever is greater. Refer to Table 4 for equations related to Auto-Precharge for LPDDR2-S4.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

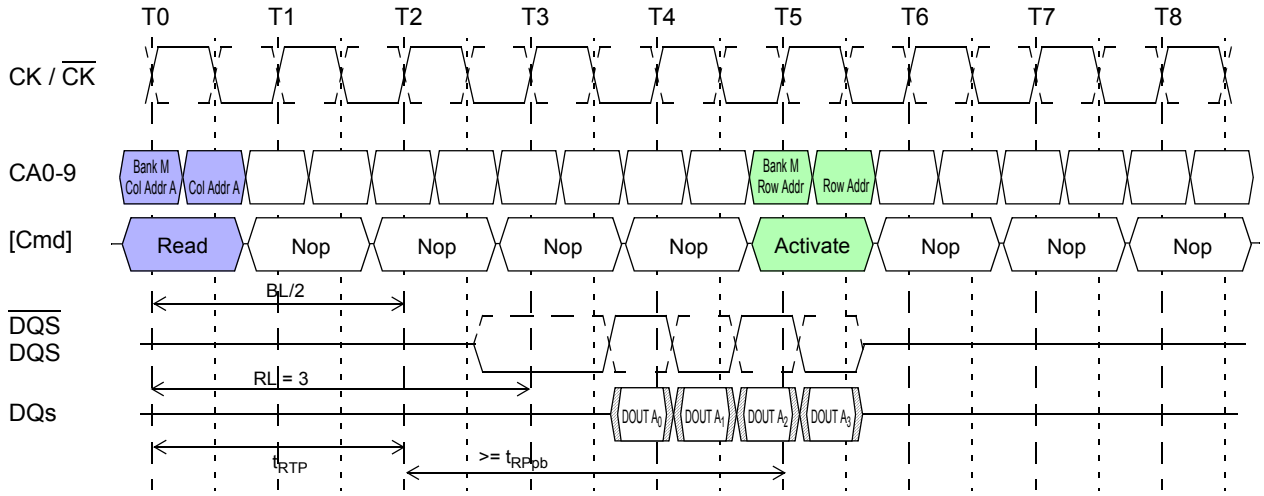


Figure 27: LPDDR2-S4: Burst read with Auto-Precharge: RL = 3, BL = 4, RU(t_{RTP}(min)/t_{CK}) = 2

9.5 LPDDR2-S4: Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is t_{WR} cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge begins.

The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

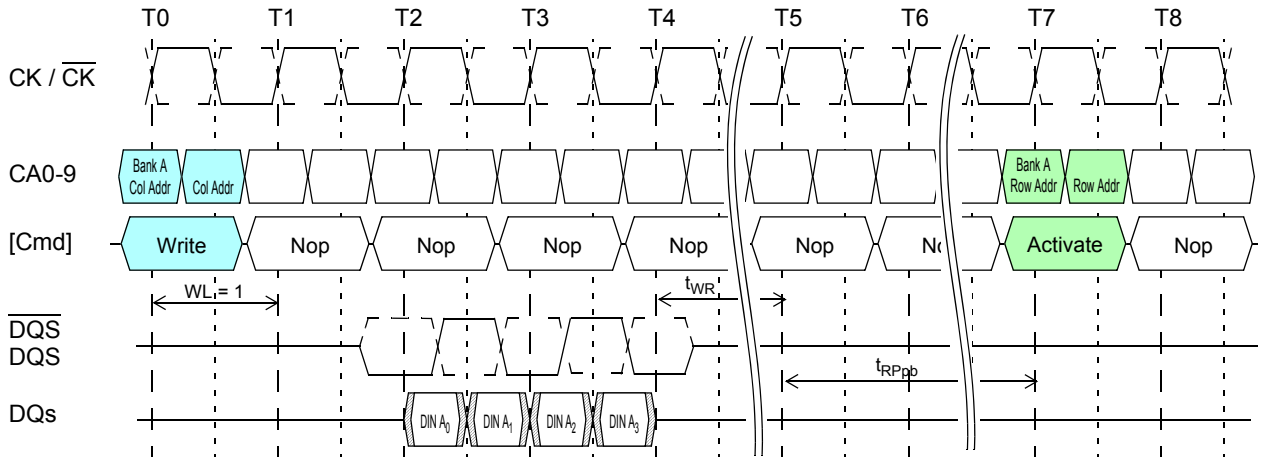


Figure 28: LPDDR2-S4: Burst write w/Auto Precharge: WL = 1, BL = 4

[Table 4] LPDDR2-S4: Precharge & Auto Precharge clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + (RU(BL/4) * 2) + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + (RU(BL/4) * 2) + RU(t_{WR}/t_{CK}) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + RU(t_{WR}/t_{CK}) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + (RU(BL/4) * 2) + RU(t_{WR}/t_{CK}) + 1	clks	1
	Precharge All	WL + (RU(BL/4) * 2) + RU(t_{WR}/t_{CK}) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + (RU(BL/4) * 2) + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})	clks	1
	Write or Write w/AP (same bank)	Illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	Illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

NOTE :
1) For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after t_{RP} depending on the latest precharge command issued to that bank.
2) Any command issued during the minimum delay time as specified in Table 4 is illegal.
3) After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/ AP and Write w /AP may not be interrupted or truncated.

10.0 LPDDR2-S4: REFRESH COMMAND

The Refresh command is initiated by having $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command (see Table 3).

A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

As shown in Table 5 , the REFpb command may not be issued to the memory until the following conditions are met:

a) t_{RFCab} has been satisified after the prior REFab command

b) t_{RFCpb} has been satisfied after the prior REFpb command

c) t_{RP} has been satisified after the prior Precharge command to that given bank

t_{RRD} has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessable during the Per Bank Refresh cycle time (t_{RFCpb}), however other banks within the device are accessable and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.

As shown in Table 5 , after issuing REFpb:

a) t_{RFCpb} must be satisified before issuing a REFab command

b) t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank

c) t_{RRD} must be satisified before issuing an ACTIVATE command to a different bank

d) t_{RFCpb} must be satisified before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero.

As shown in Table 5 , the REFab command may not be issued to the memory until the following conditions have been met:

a) t_{RFCab} has been satisified after the prior REFab command

b) t_{RFCpb} has been satisified after the prior REFpb command

c) t_{RP} has been satisified after prior Precharge commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state.

As shown in Table 5 , after issuing REFab:

a) the t_{RFCab} latency must be satisfied before issuing an ACTIVATE command

b) the t_{RFCab} latency must be satisfied before issuing a REFab or REFpb command.

[Table 5] Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to		Notes
t_{RFCab}	REFab	REFab		
		Activate cmd to any bank .		
		REFpb		
t_{RFCpb}	REFpb	REFab		
		Activate cmd to same bank as REFpb		
		REFpb		
t_{RRD}	REFpb	Activate cmd to *different* bank than REFpb		
	Activate	REFpb affecting an idle bank (*different* bank than Activate)		1
		Activate cmd to *different* bank than prior Activate		

NOTE :
1) A bank must be in the Idle state before it is refreshed. Therefore, after Activate, REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state.

10.1 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:
The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within *any* rolling Refresh Window (t_{REFW} = 32 ms @ Tcase ≤ 85 °C). See Table 6 for actual numbers per density. The resulting average refresh interval (t_{REFI}) is given in Table 6 .

See Mode Register 4 on specific datasheet for t_{REFW} and t_{REFI} refresh multipliers at different MR4 settings.

For LPDDR2-SDRAM devices supporting Per-Bank-Refresh, a REFab command may be replaced by a full cycle of eight REFpb commands.

(2) Burst Refresh limitation:
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling t_{REFBW} (t_{REFBW} = 4 x 8 x t_{RFCab}). This condition does not apply if REFpb commands are used.

(3) Refresh Requirements and Self-Refresh:
If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:
$R^* = R - RU\{t_{SRF} / t_{REFI}\} = R - RU\{R * t_{SRF} / t_{REFW}\}$; where RU stands for the round-up function.

[Table 6] LPDDR2-S4 Refresh Requirement Parameters (per density)

Parameter		Symbol	64 Mb	128 Mb	256 Mb	512 Mb	1 Gb	2 Gb	4 Gb	8 Gb	Unit
Number of Banks			4				8				
Refresh Window Tcase ≤ 85°C		t_{REFW}	32								ms
Refresh Window 85°C < Tcase ≤ 105°C		t_{REFW}	8								ms
Required number of REFRESH commands (min)		R	2,048	2,048	4,096	4,096	4,096	8,192	8,192	8,192	
average time between REFRESH commands (for reference only) Tcase≤ 85°C	REFab	t_{REFI}	15.6	15.6	7.8	7.8	7.8	3.9	3.9	3.9	us
	REFpb	t_{REFIpb}	(REFpb not allowed below 1 Gb.)				0.975	0.4875	0.4875	0.4875	us
Refresh Cycle time		t_{RFCab}	90	90	90	90	130	130	130	210	ns
Per Bank Refresh Cycle time		t_{RFCpb}	NA				60	60	60	60	ns
Burst Refresh Window = 4 x 8 x tRFCab		t_{REFBW}	2.88	2.88	2.88	2.88	4.16	4.16	4.16	6.72	us

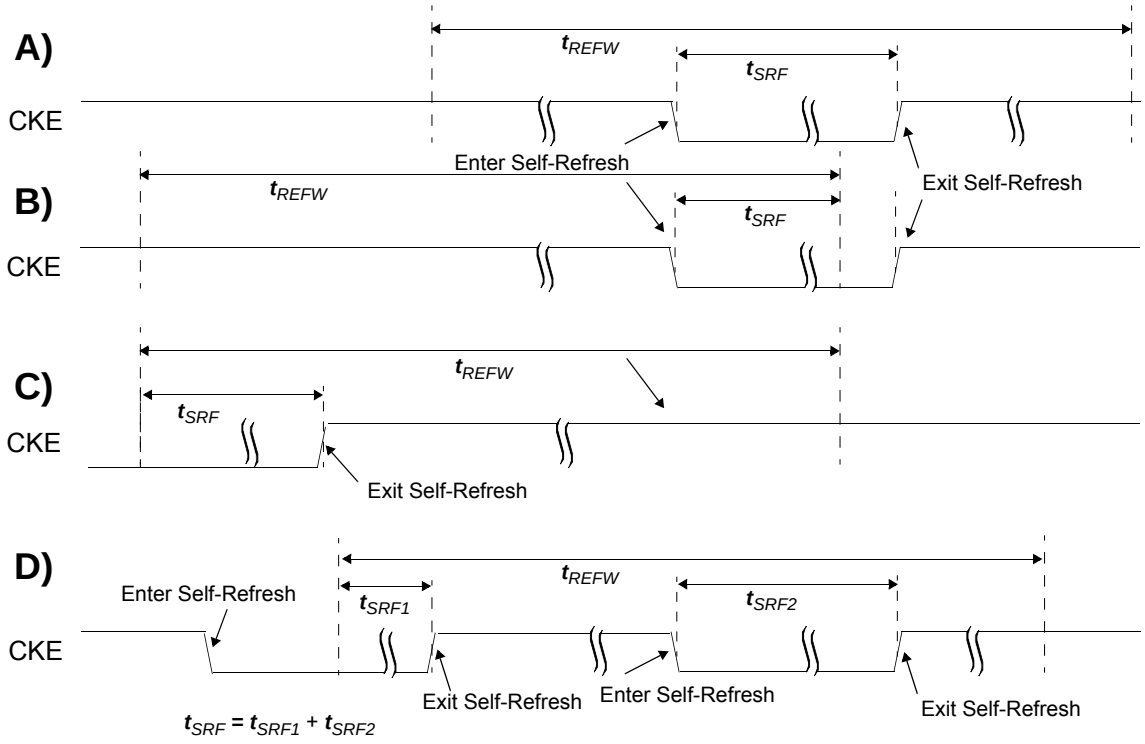


Figure 29: LPDDR2-S4: Definition of t_{SRF}

Several examples on how to t_{SRF} is caclulated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (*t*REFW),
B: at Self-Refresh entry
C: at Self-Refresh exit
D: with several different invervals spent in Self Refresh during one *t*REFW interval

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-S4 devices allow significant flexibiliy in scheduling REFRESH commands, as long as the boundary conditions above are met.

In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time.

The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme (e.g., LPDDR2-S4 1Gb) the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by tREFW - (R / 8) * tREFBW = tREFW - R * 4 * tRFCab. (e.g., for a LPDDR2-S4 1Gb device @ Tcase <= 85oC this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms).

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in *every* rolling refresh window during the transition. Figure 31 on page 128 shows an example of an allowable transition from a burst pattern to a regular, distributed pattern. If this transition happens directly after the burst refresh phase, all rolling tREFW intervalls will have at least the required number of refreshes. Figure 32 on page 129 shows an example of a non-allowable transition. In this case the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimmun number of REFRESH commands is not satisfied. The understanding of the pattern transition is extremly relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern as indicated in Figure 33 on page 129 and begin with the burst phase upon exit from Self-Refresh.

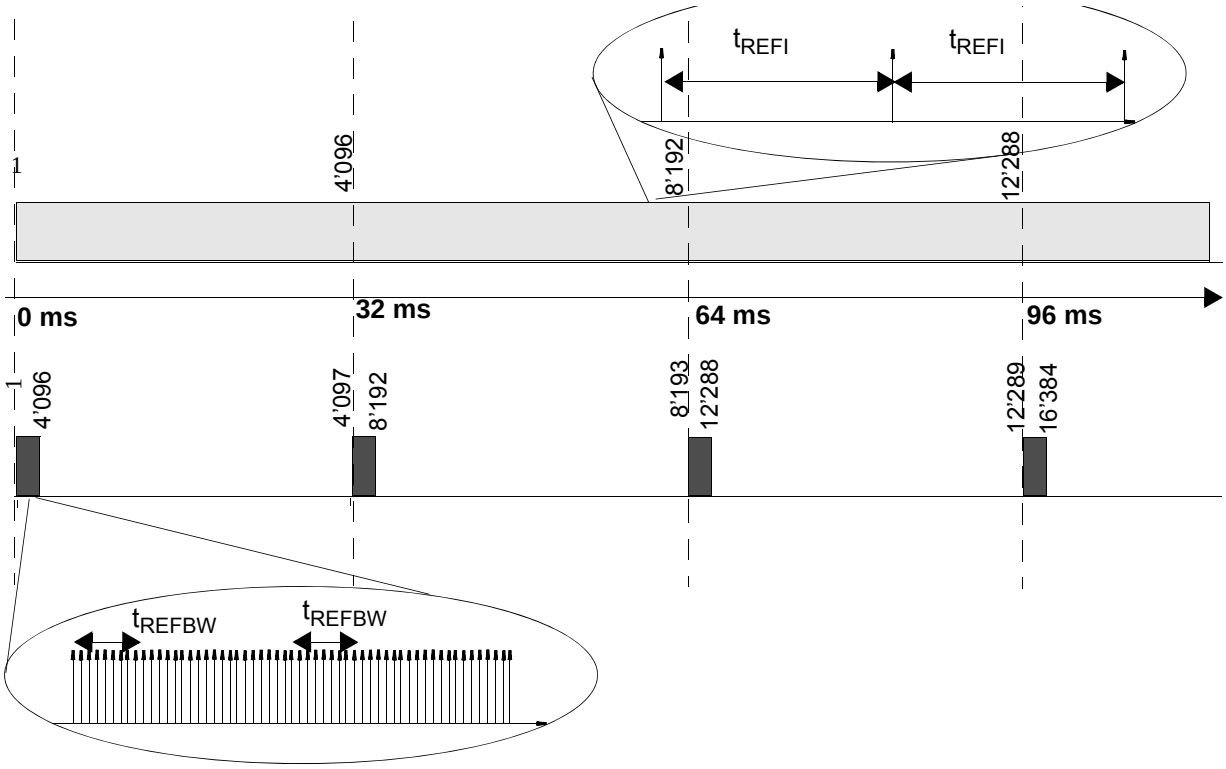


Figure 30: LPDDR2-S4: Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause

NOTE :
1) For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85oC the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

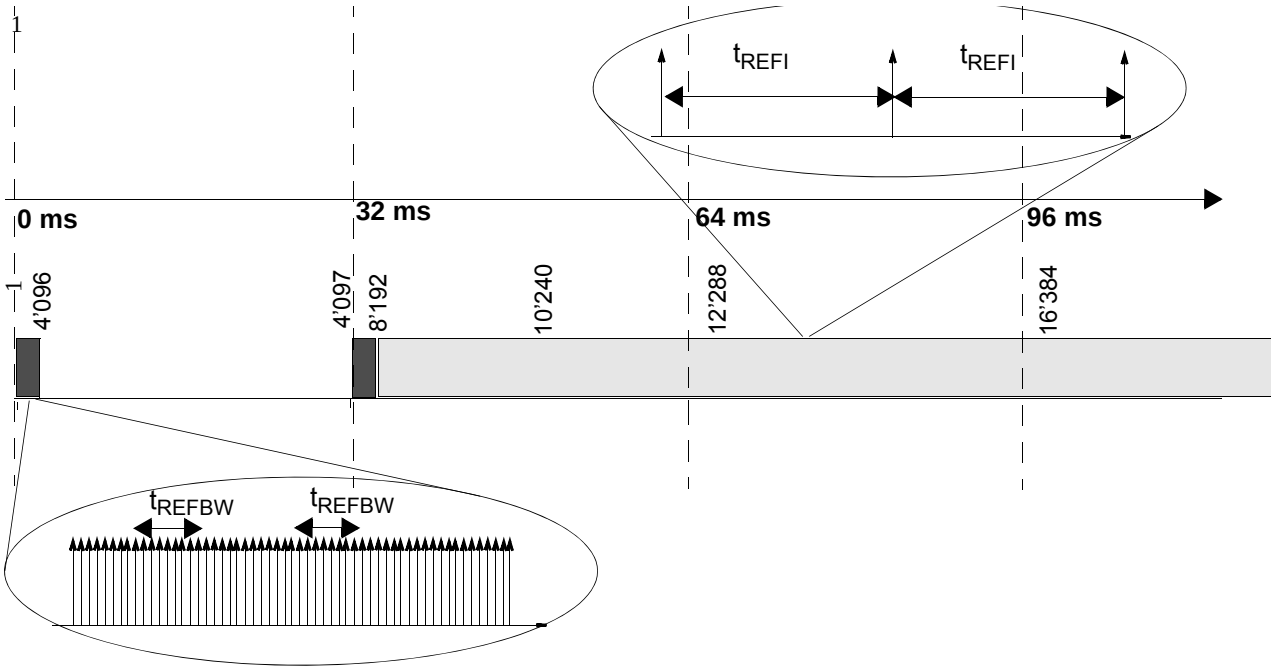


Figure 31: LPDDR2-S4: Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE :
1) For a (e.g.) LPDDR2-S4 1 Gb device @ Tcase less than or equal to 85oC the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have an average of one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

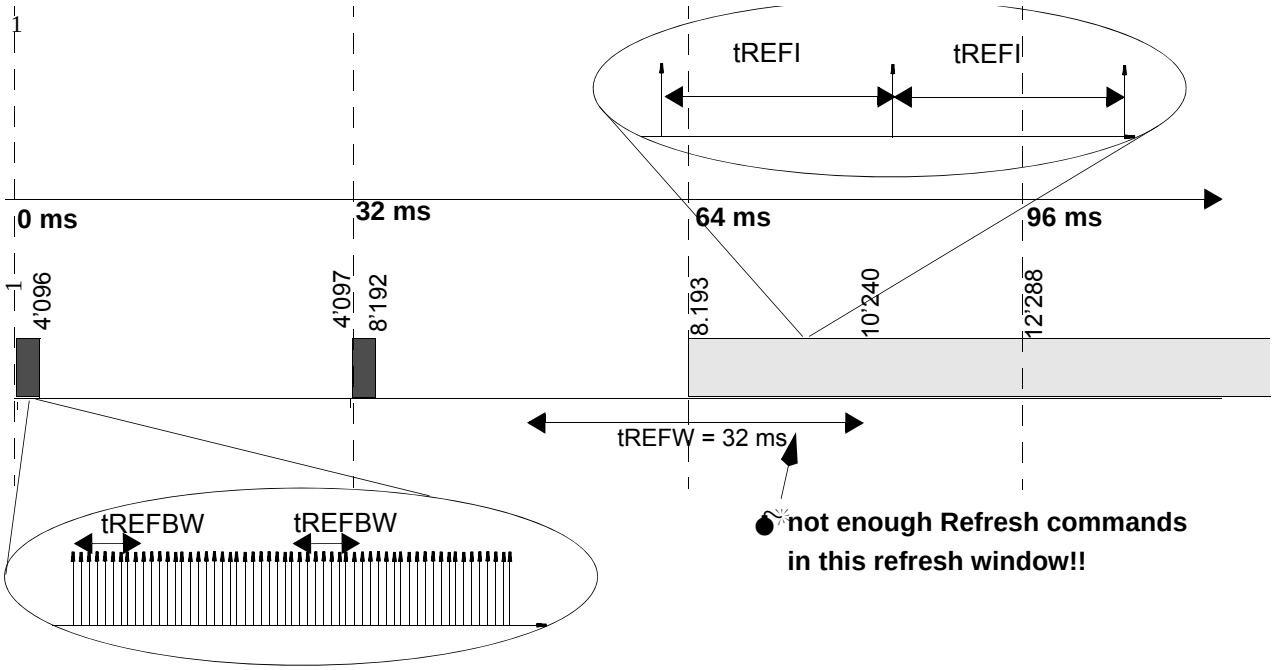


Figure 32: LPDDR2-S4: NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

NOTE :
1) Only ~2048 REFRESH commands (<R!!) in the indicated tREFW window.

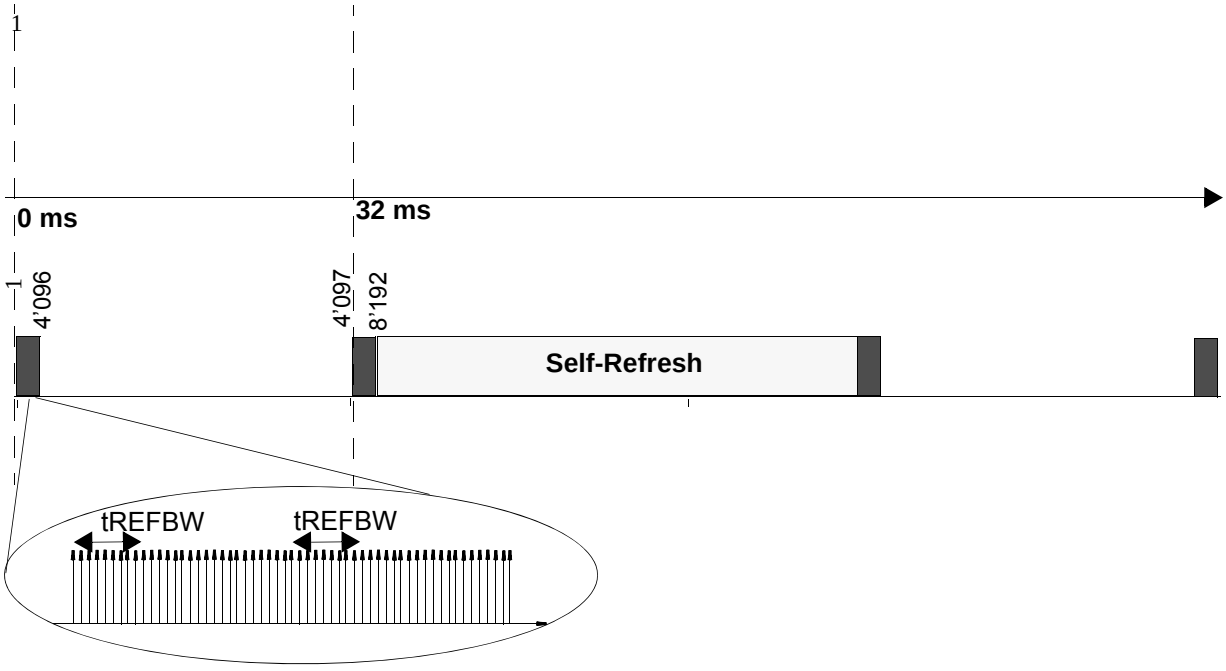


Figure 33: LPDDR2-S4: Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns

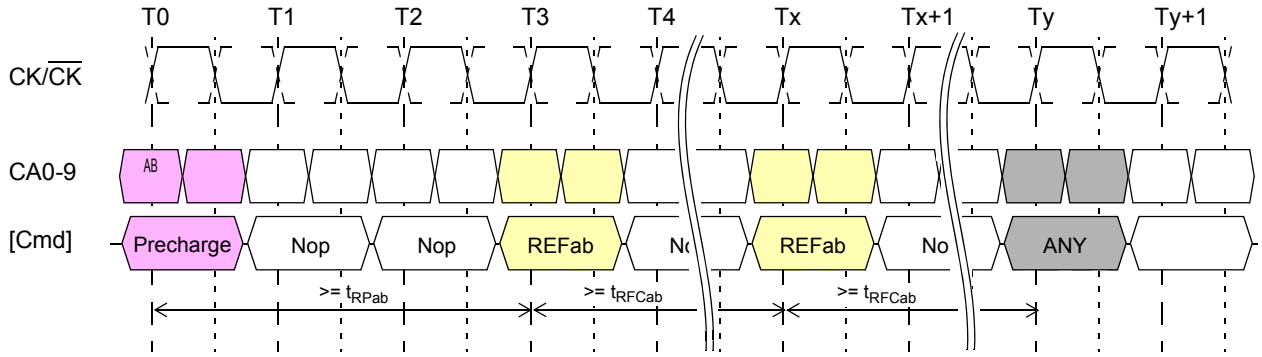


Figure 34: LPDDR2-S4: All Bank Refresh Operation

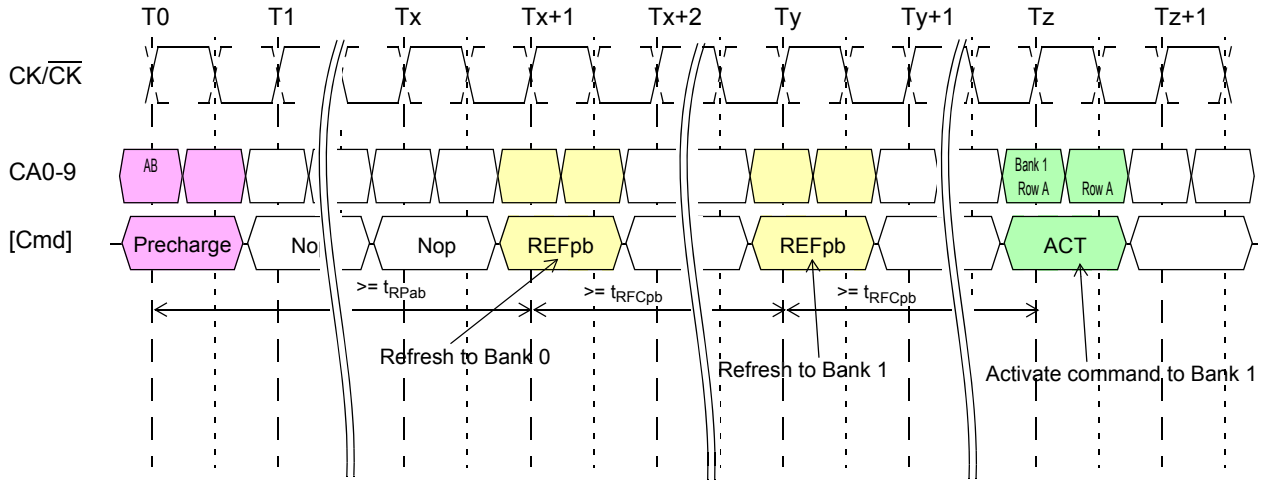


Figure 35: LPDDR2-S4: Per Bank Refresh Operation

NOTE :
1) In the beginning of this example, the REFpb bank is pointing to Bank 0.
2) Operations to other banks than the bank being refreshed are allowed during the t_{RFCpb} period.

11.0 LPDDR2-S4: SELF REFRESH OPERATION

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures. See "LPDDR2 IDD Specification Parameters and Operating Conditions" on Specific datasheet for details.

Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels. VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see "Absolute Maximum DC Ratings" on Specific datasheet). However prior to exiting Self-Refresh, VrefDQ and VrefCA must be within specified limits (see "Recommanded DC Operating Conditions" on specific datasheet). The SDRAM initiates a minimum of one all-bank refresh command internally within t_{CKESR} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is t_{CKESR}. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2 tCK prior to the positive clock edge that registers CKE. Once Self Refresh Exit is registered, a delay of at least t_{XSR} must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSR} for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSR}.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section Chapter 10.1, since no refresh operations are performed in power-down mode.

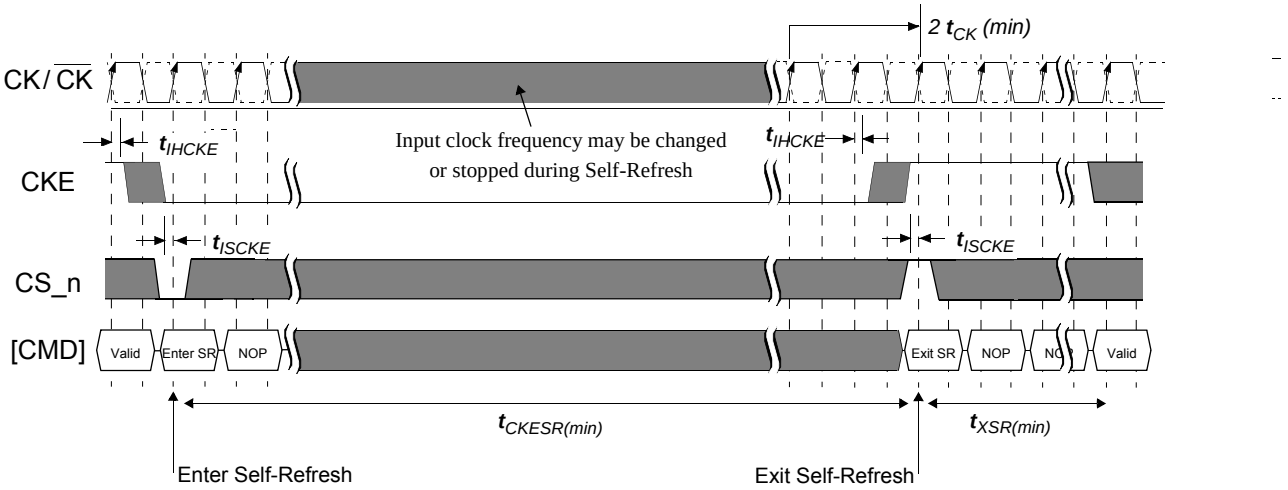


Figure 36: LPDDR2-S4: Self-Refresh Operation

NOTE :
1) Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2) Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3) t_{XSR} begins at the rising edge of the clock after CKE is driven HIGH.
4) A valid command may be issued only after t_{XSR} is satisfied. NOPs shall be issued during t_{XSR}.

11.1 LPDDR2-S4: Partial Array Self-Refresh: Bank Masking

LPDDR2-S4 SDRAM has 4 or 8 banks. For LPDDR2-S4 devices, 64Mb to 512Mb LPDDR2 SDRAM has 4 banks, while 1Gb and higher density has 8. Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

11.2 LPDDR2-S4: Partial Array Self-Refresh: Segment Masking

Segment masking scheme may be used in lieu of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits. LPDDR2 SDRAM whose density is 64Mb, 128Mb, 256Mb, or 512Mb does not support segment masking. Only bank masking scheme is available. For 1Gb and larger densities, 8 segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. These 2 mode register units are noted as “not used” for low-density LPDDR2-S4 SDRAM and a programming of mask bits has no effect on the device operation.

[Table 7] Example of Bank and Segment Masking use in LPDDR2-S4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0		M						M
Segment 1	0		M						M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0		M						M
Segment 4	0		M						M
Segment 5	0		M						M
Segment 6	0		M						M
Segment 7	1	M	M	M	M	M	M	M	M

NOTE :
1) This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

12.0 MODE REGISTER READ COMMAND

The Mode Register Read command is used to read configuration and status data from mode registers for SDRAM. The Mode Register Read (MRR) command is initiated by having $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 41. All DQS, DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS, DQS shall be toggled.

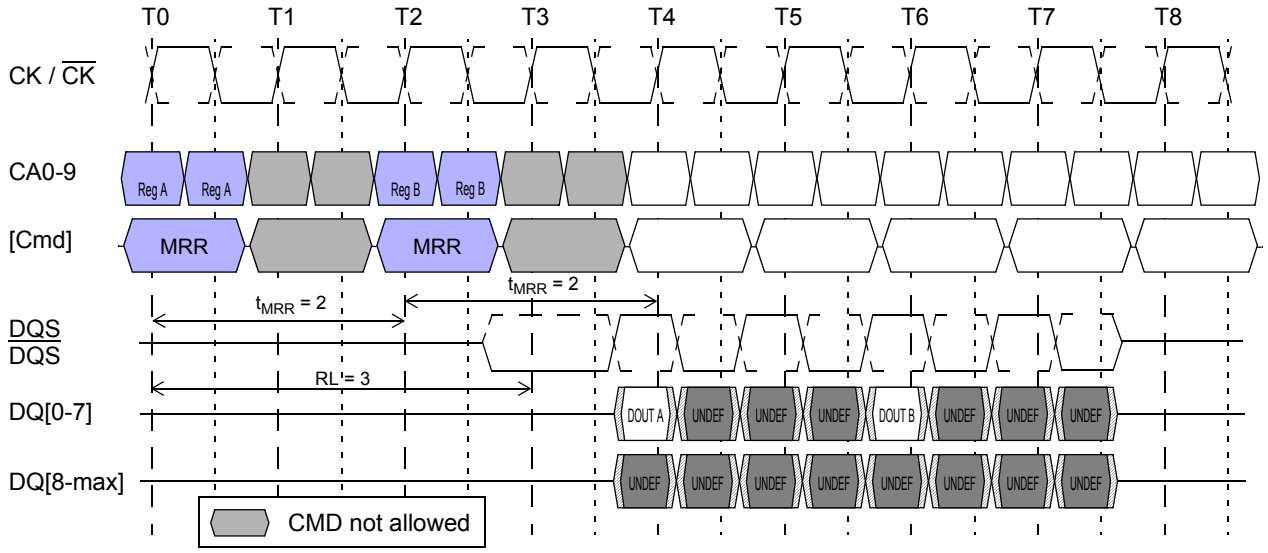


Figure 37: Mode Register Read timing example: RL = 3, t_{MRR} = 2

NOTE :
1) Mode Register Read has a burst length of four.
2) Mode Register Read operation shall not be interrupted.
3)Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4) The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
5) Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6) Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7) Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1clock cycles.

The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”

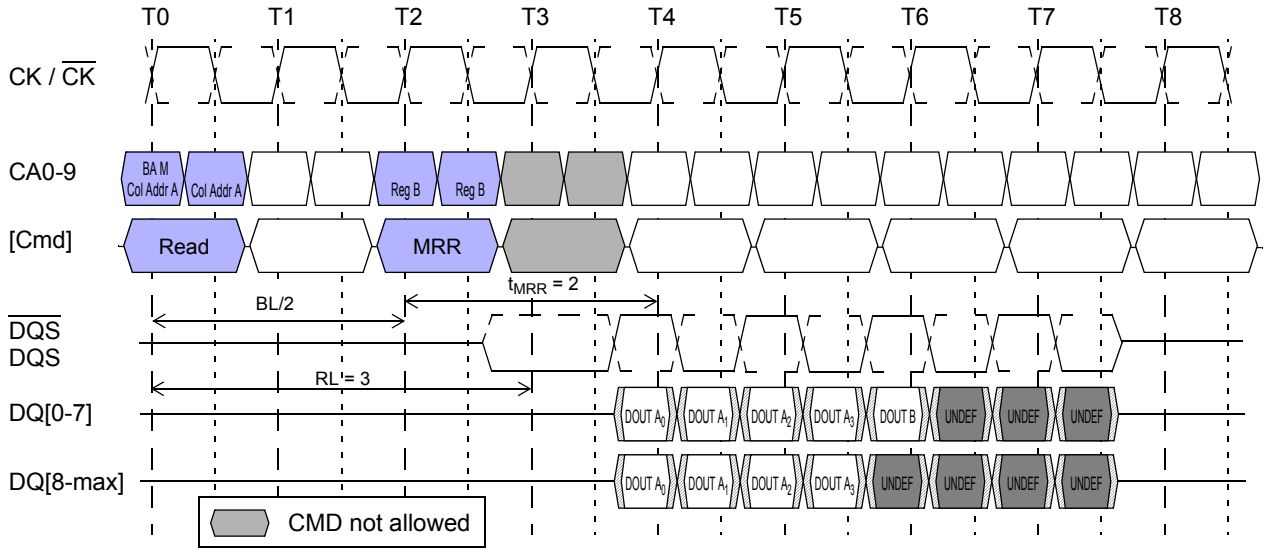


Figure 38: LPDDR2: Read to MRR timing example: RL = 3, t_{MRR} = 2

NOTE :
1) The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2) The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

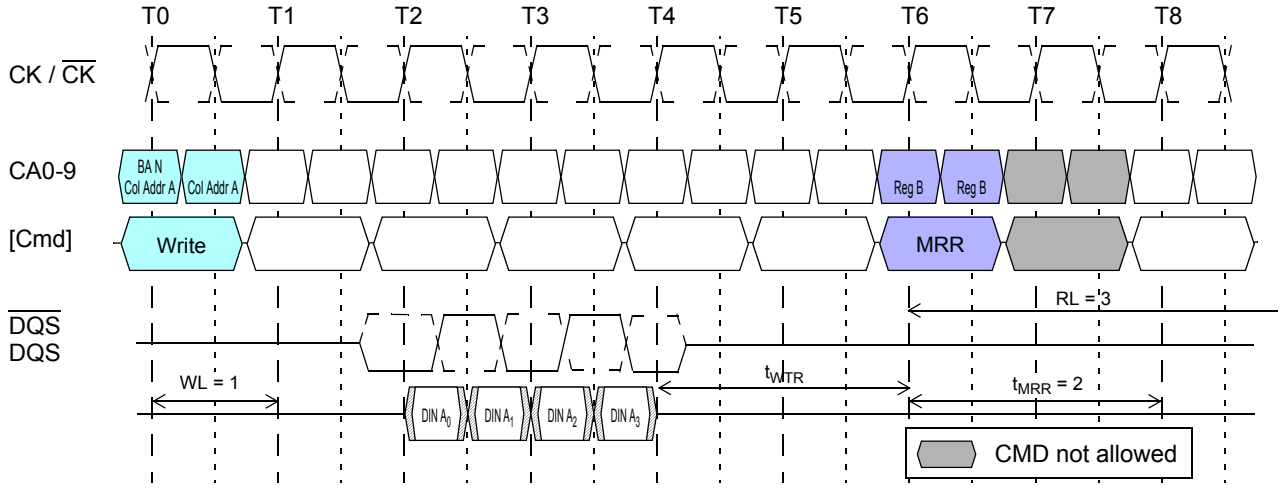


Figure 39: LPDDR2: Burst Write Followed by MRR: RL = 3, WL = 1, BL = 4

NOTE :
1) The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(t_{WTR} /t_{CK})].
2) The Mode Register Read Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

12.1 Temperature Sensor

LPDDR2-S4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the Extended Temperature Range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER (See "Operating Temperature Range" on Specific datasheet) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See "Operating Temperature Range" on Specific datasheet) that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85o C when MR4[2:0] equals 011B.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2^{o} C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

LPDDR2 devices shall allow for a 2^{o} C temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2C$$

[Table 8] Temperature Sensor

Parameter	Symbol	Max/Min	Value	Unit
System Temperature Gradient	TempGradient	Max	System Dependent	^{o}C/s
MR4 Read Interval	ReadInterval	Max	System Dependent	ms
Temperature Sensor Interval	tTSI	Max	32	ms
System Response Delay	SysRespDelay	Max	System Dependent	ms
Device Temperature Margin	TempMargin	Max	2	^{o}C

For example, if TempGradient is 10^{o}C/s and the SysRespDelay is 1 ms:

$$\frac{10C}{s} \times (ReadInterval + 32ms + 1ms) \leq 2C$$

In this case, ReadInterval shall be no greater than 167 ms.

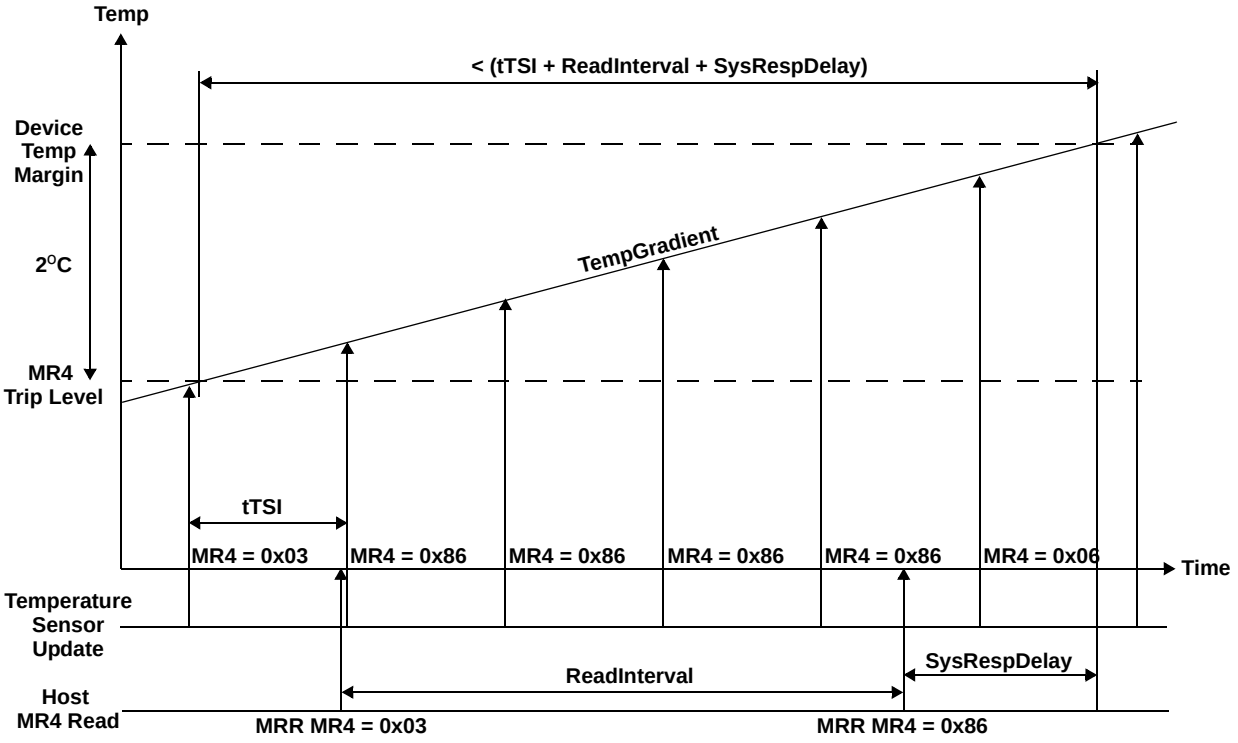


Figure 40: Temp Sensor Timing

12.2 DQ Calibration

LPDDR2-S4 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0] for x8 devices, DQ[0] and DQ[8] for x16 devices, and DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x8 devices, DQ[7:1] drive 0b during the MRR burst. For x16 devices, DQ[7:1] and DQ[15:9] drive 0b during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive 0b during the MRR burst.

For LPDDR2-S4 devices, MRR DQ Calibration commands may only occur in the Idle state.

[Table 9] Data Calibration Pattern Description

Parameter	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern "A" (MR32)	1	0	1	0
Pattern "B" (MR40)	0	0	1	1

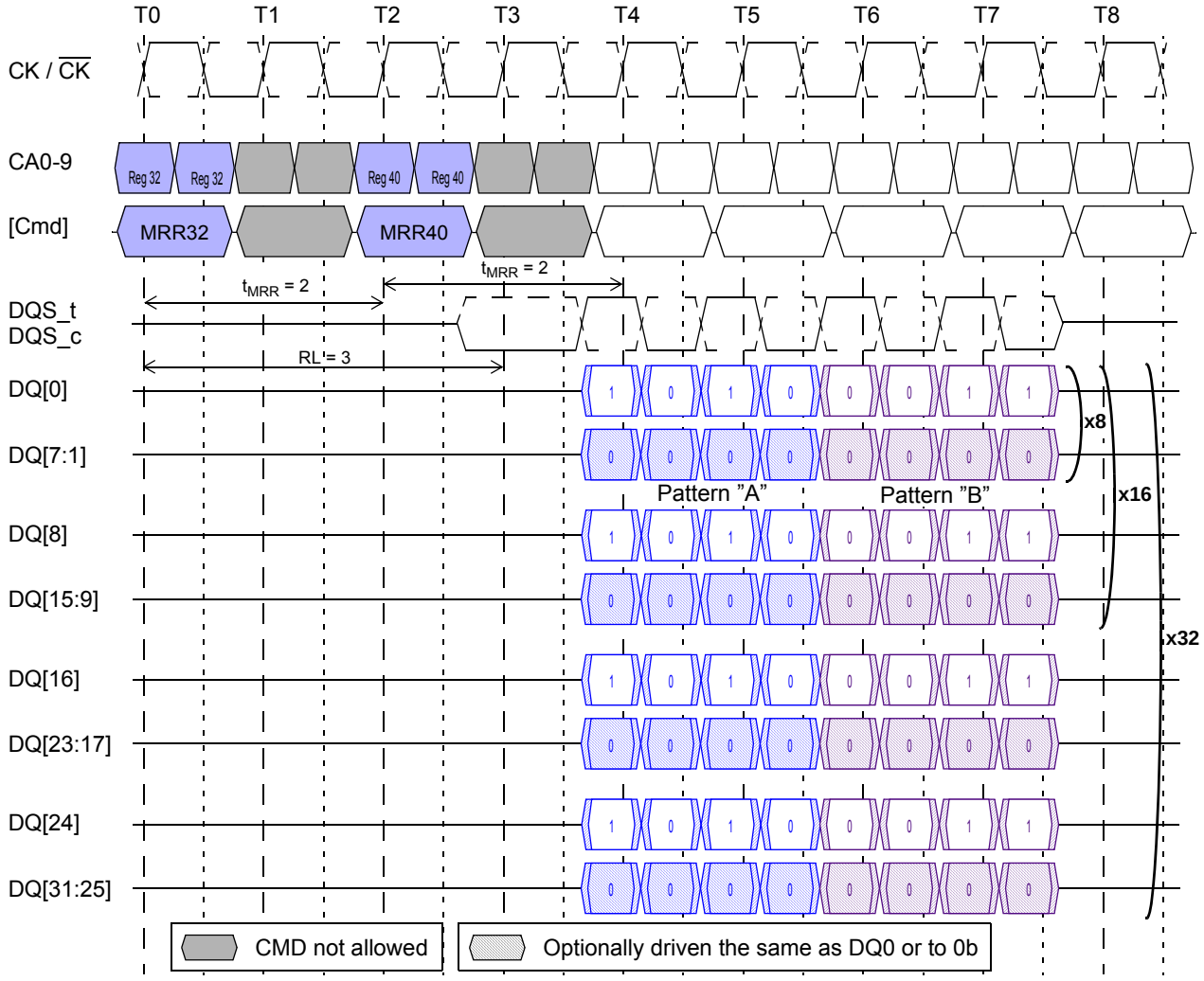


Figure 41: MR32 and MR40 DQ Calibration timing example: RL = 3, t_{MRR} = 2

NOTE :
1) Mode Register Read has a burst length of four.
2) Mode Register Read operation shall not be interrupted.
3) Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x16 devices, DQ[8] shall drive the same information as DQ[0] during the burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.
4) The Mode Register Command period is t_{MRR}. No command (other than Nop) is allowed during this period.

13.0 MODE REGISTER WRITE COMMAND

The Mode Register Write command is used to write configuration data to mode registers for SDRAM. The Mode Register Write (MRW) command is initiated by having $\overline{CS}$ LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by t_{MRW}. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

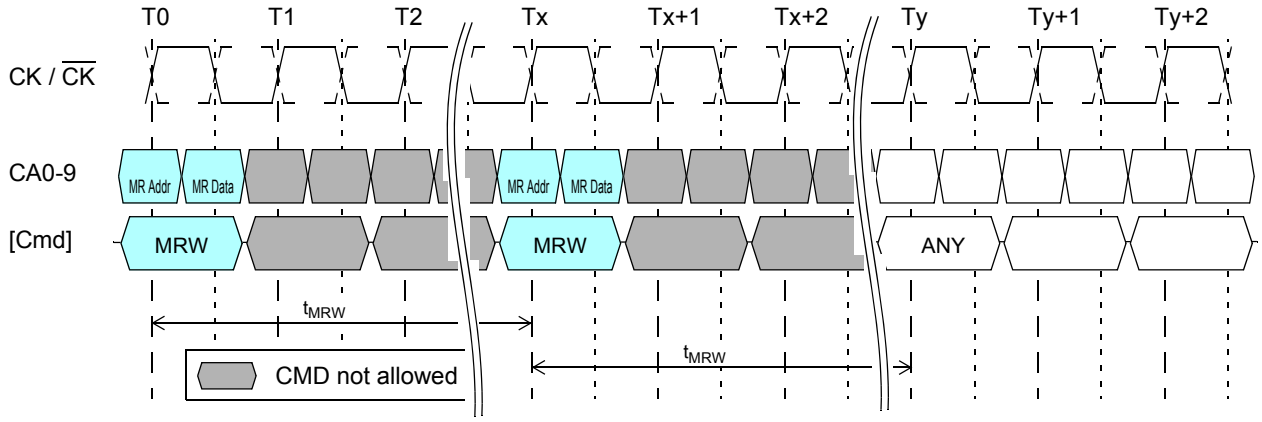


Figure 42: Mode Register Write timing example: RL = 3, t_{MRW} = 5

NOTE :
1) The Mode Register Write Command period is t_{MRW}. No command (other than Nop) is allowed during this period.
2) At time Ty, the device is in the idle state.

13.1 LPDDR2-S4: Mode Register Write

For LPDDR2 devices (SDRAM), the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command.

[Table 10] Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)Mode Register Write Reset (MRW Reset)

Current State	Command	Intermediate State	Next State
SDRAM		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Init)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

13.2 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence (step 2 in Chapter 1.1). The MRW Reset command may be issued from the Idle state for LPDDR2-S4 devices. This command resets all Mode Registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period (t_{INIT4}). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-S4 devices are undefined after the MRW Reset command.

For the timing diagram related to MRW Reset, refer to Figure 1 .

13.3 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 ouput drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 on specific datasheet for description on the command codes for the different ZQ Calibration commands.

The Initialization ZQ Calibration(ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQReset Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / ^{o}C, VSens = 0.20% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4\,s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.

No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See "Output Driver DC Electrical Characteristics without ZQ Calibration")

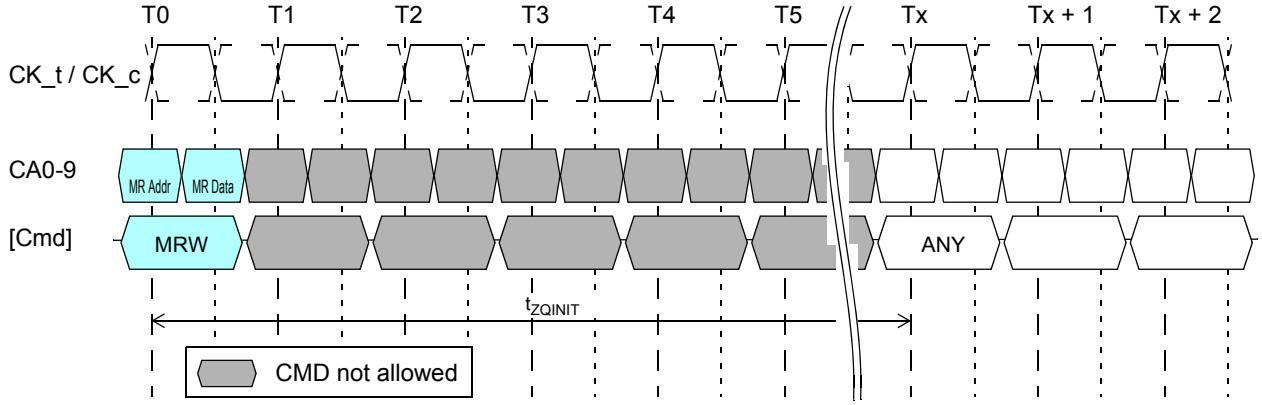


Figure 43: ZQ Calibration Initialization timing example

NOTE :
1) The ZQ Calibration Initialization period is t_{ZQINIT}. No command (other than Nop) is allowed during this period.
2) CKE must be continuously registered HIGH during the calibration period.
3) All devices connected to the DQ bus should be high impedance during the calibration process.

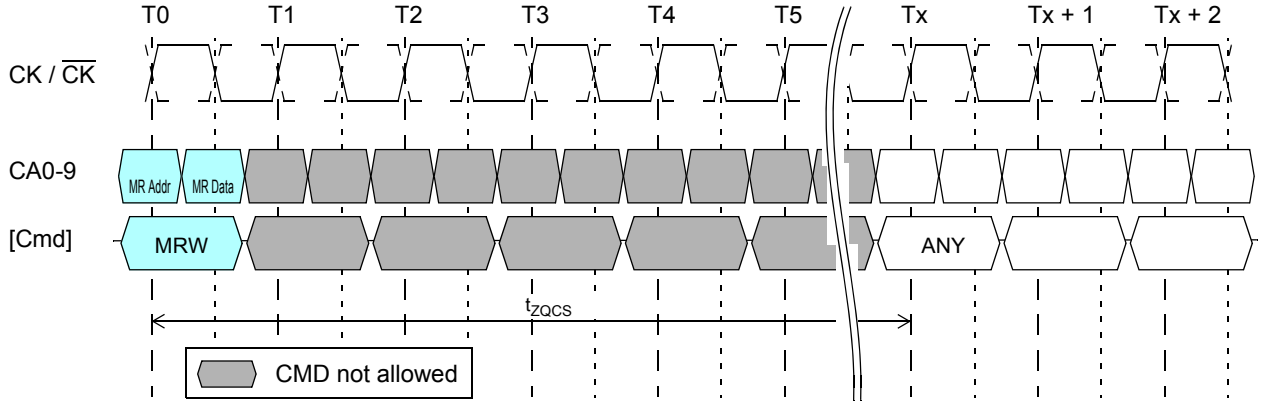


Figure 44: ZQ Calibration Short timing example

NOTE :
1) The ZQ Calibration Short period is t_{ZQCS}. No command (other than Nop) is allowed during this period.
2) CKE must be continuously registered HIGH during the calibration period.
3) All devices connected to the DQ bus should be high impedance during the calibration process.

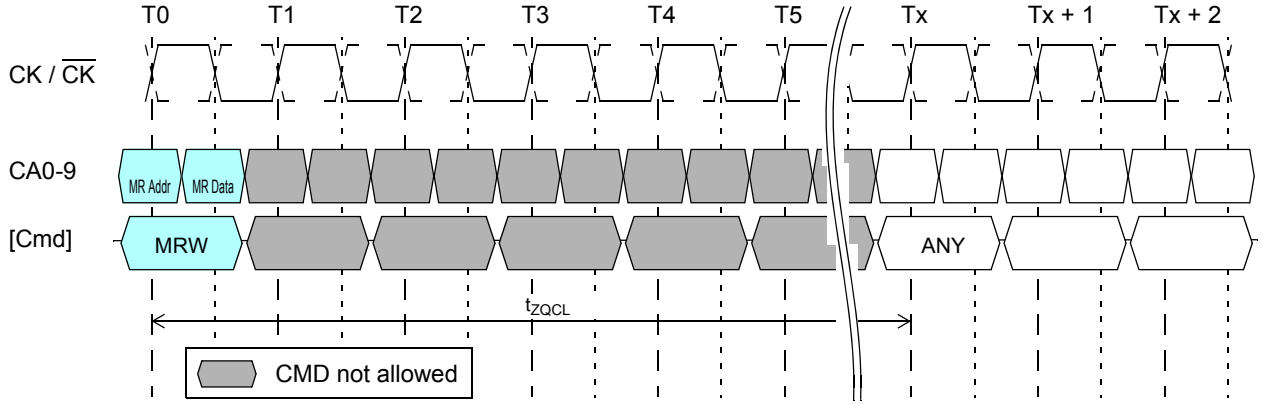


Figure 45: ZQ Calibration Long timing example

NOTE :
1) The ZQ Calibration Long period is t_{ZQCL}. No command (other than Nop) is allowed during this period.
2) CKE must be continuously registered HIGH during the calibration period.
3) All devices connected to the DQ bus should be high impedance during the calibration process.

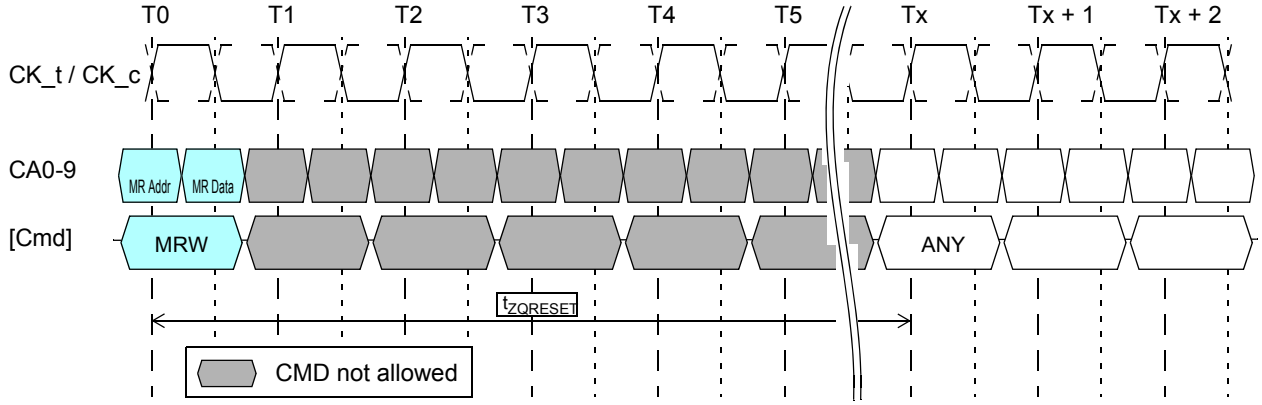


Figure 46: ZQ Calibration Reset timing example

NOTE :
1) The ZQ Calibration Reset period is $t_{ZQRESET}$. No command (other than Nop) is allowed during this period.
2) CKE must be continuously registered HIGH during the calibration period.
3) All devices connected to the DQ bus should be high impedance during the calibration process.

13.3.1 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited (See "Input/output capacitance" on specific datasheet)

14.0 POWER-DOWN

For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and $\overline{CS}$ HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power down.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until t_{CKE} has been satisfied. V_{REF} must be maintained at a valid level during power down.

VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges (See "Recommended DC Operating Conditions")

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section Chapter 10.1, as no refresh operations are performed in power-down mode.

The power-down state is exited when CKE is registered HIGH. The controller shall drive $\overline{CS}$ HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with power-down exit latency, t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the timing parameter table of this standard.

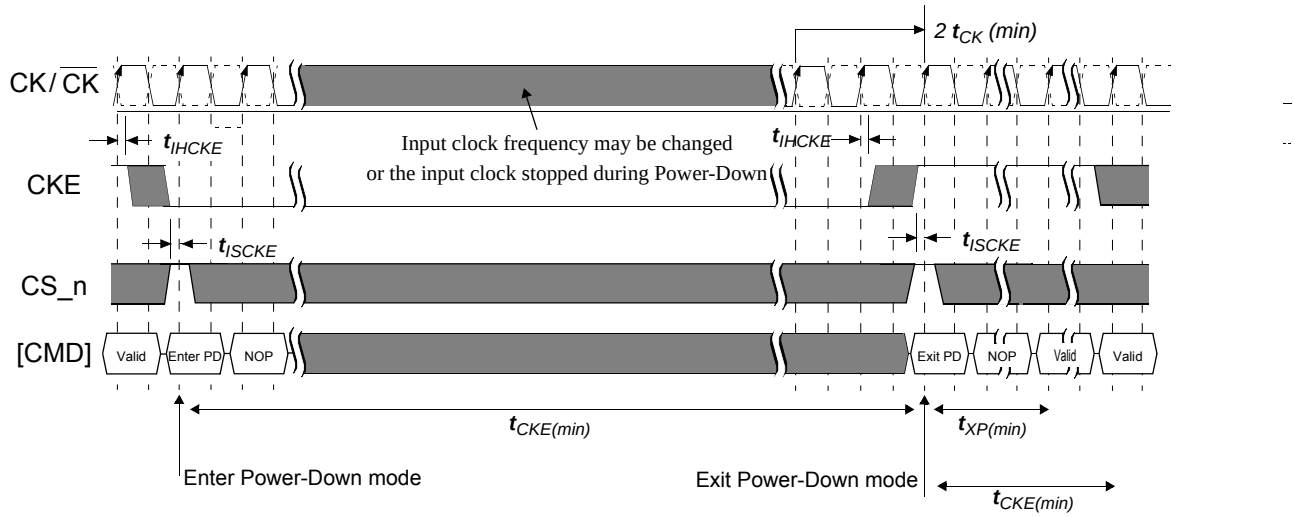


Figure 47: LPDDR2-S4: Basic power down entry and exit timing diagram

NOTE :
1) Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

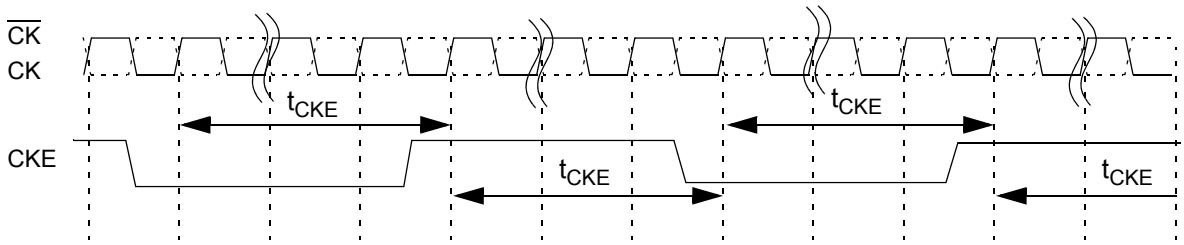


Figure 48: Example CKE intensive environment

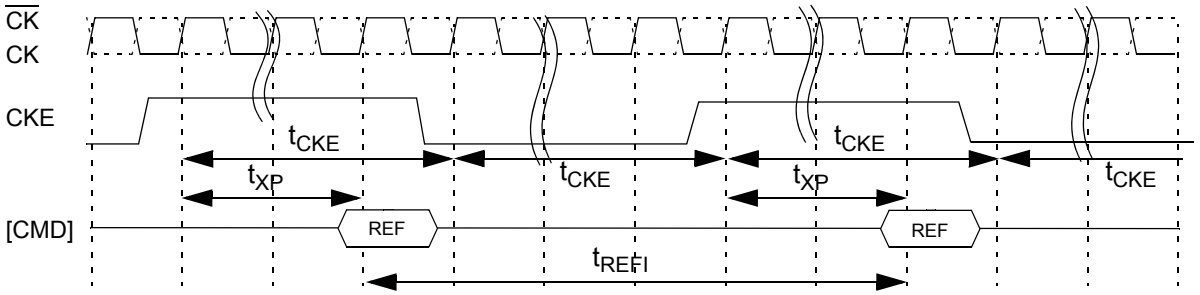


Figure 49: REF to REF timing with CKE intensive environment for LPDDR2 SDRAM

NOTE :
1) The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift

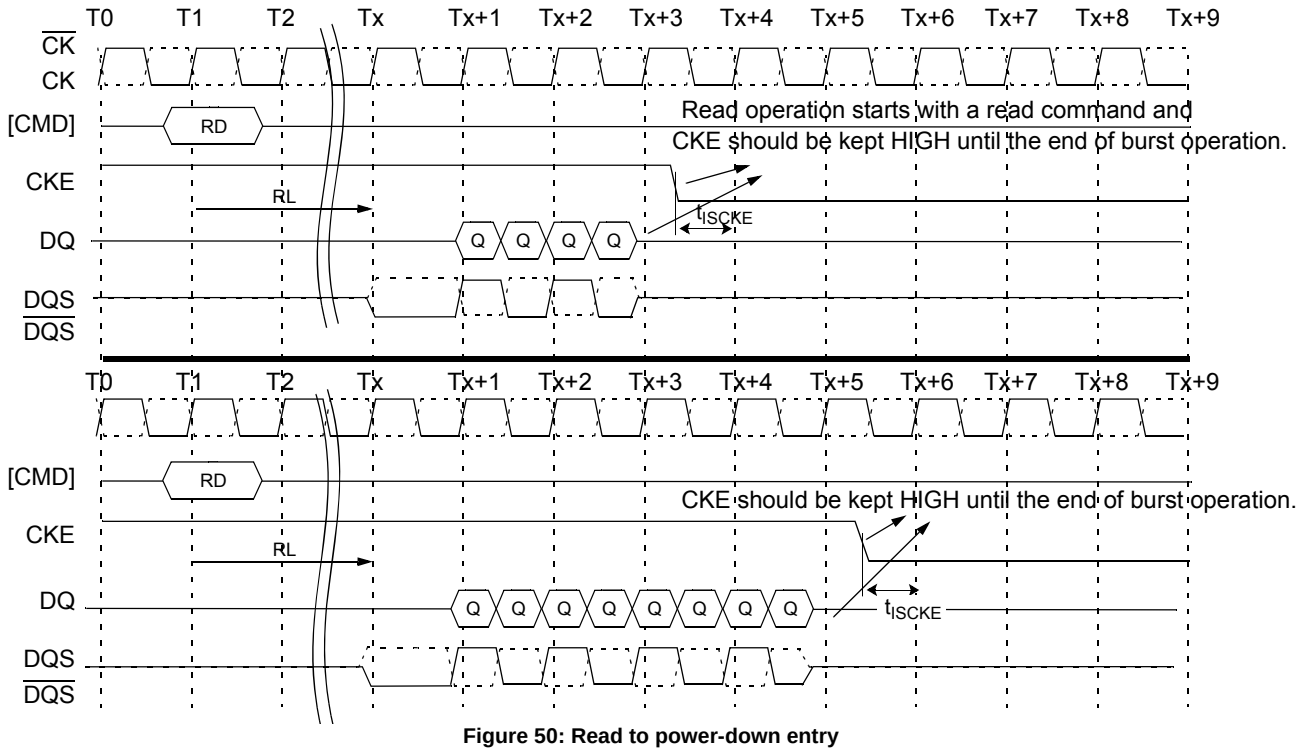


Figure 50: Read to power-down entry

NOTE :

1) CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

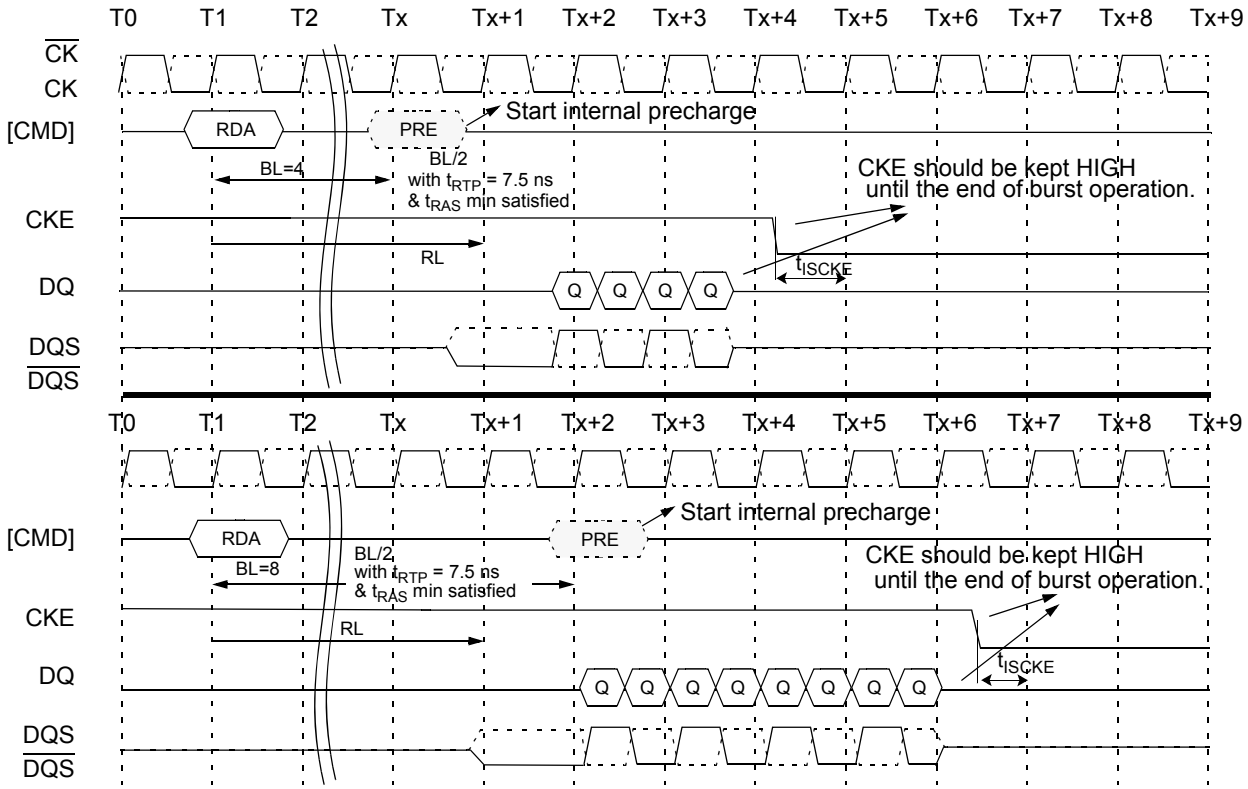


Figure 51: LPDDR2 SDRAM Read with auto precharge to power-down entry

NOTE :

1) CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}/t_{CK}$)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

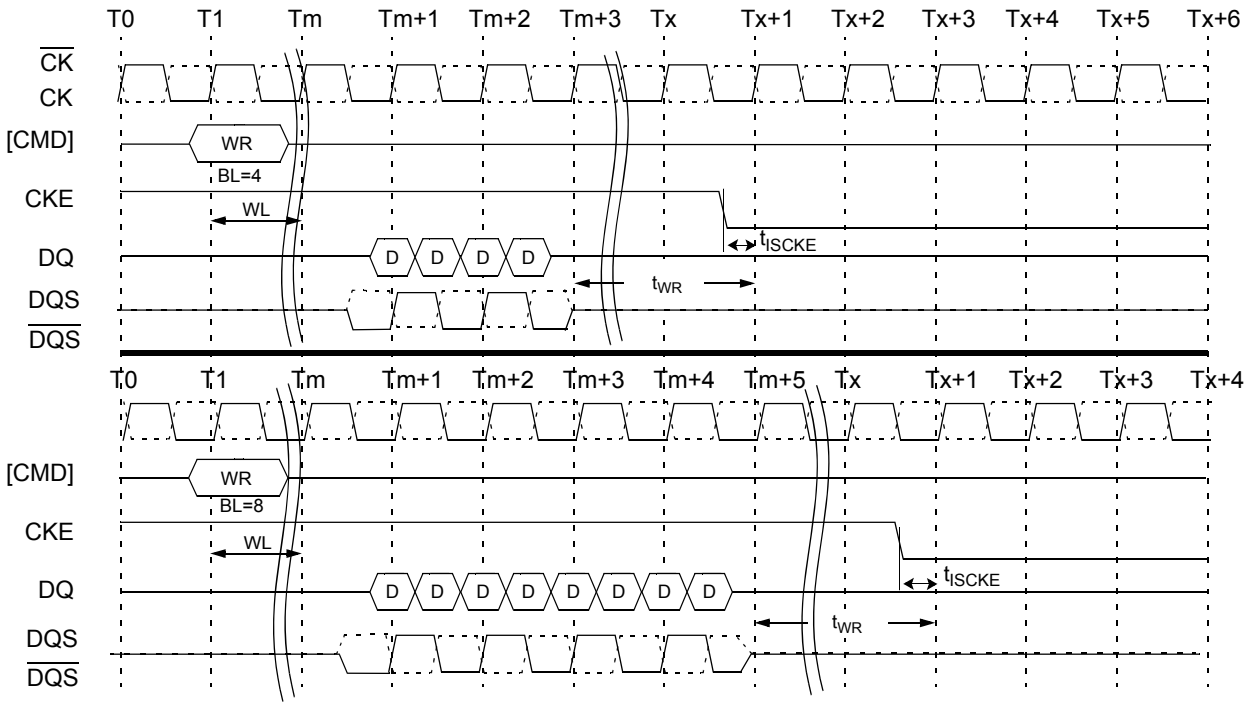


Figure 52: Write to power-down entry

NOTE:
1) CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK})clock cycles after the clock on which the Write command is registered.

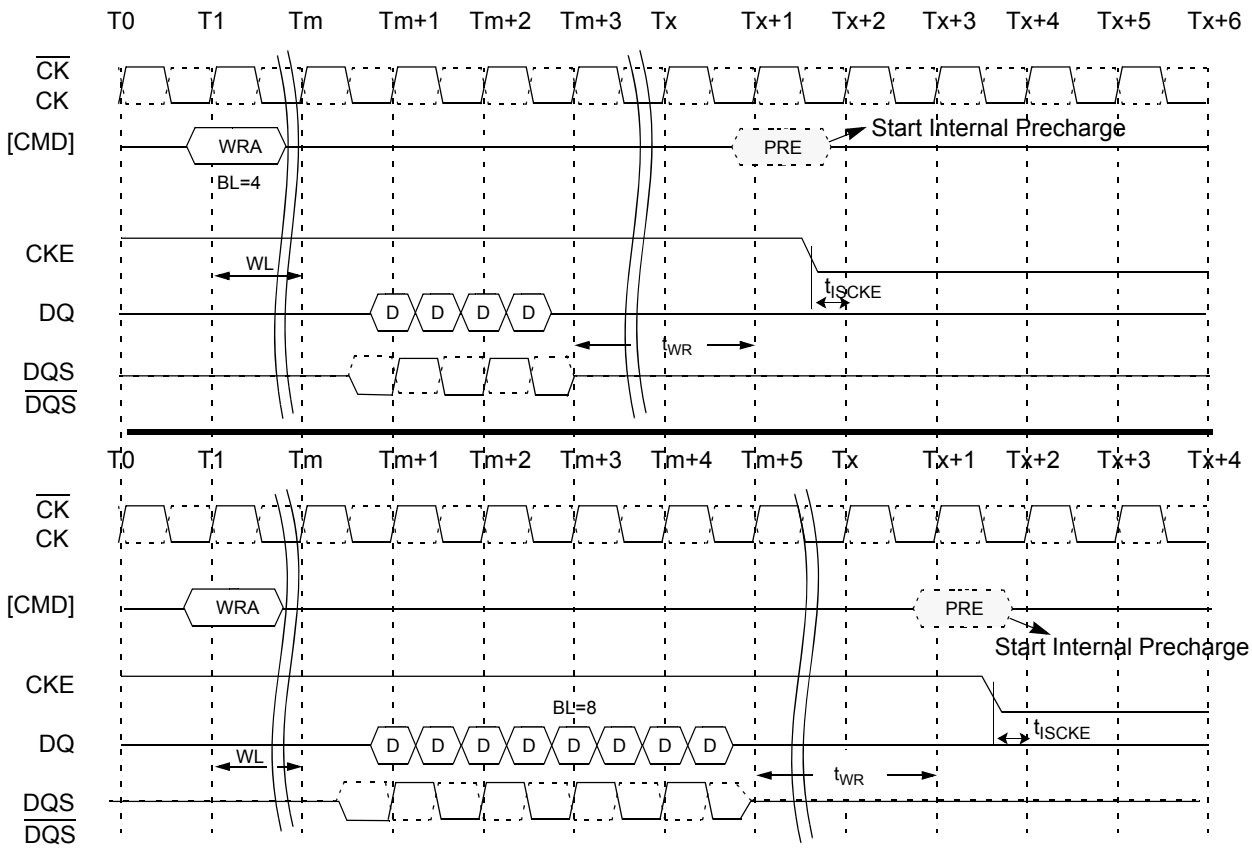


Figure 53: LPDDR2-S4: Write with autoprecharge to power-down entry

NOTE :
1) CKE may be registered LOW WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1 clock cycles after the Write command is registered.

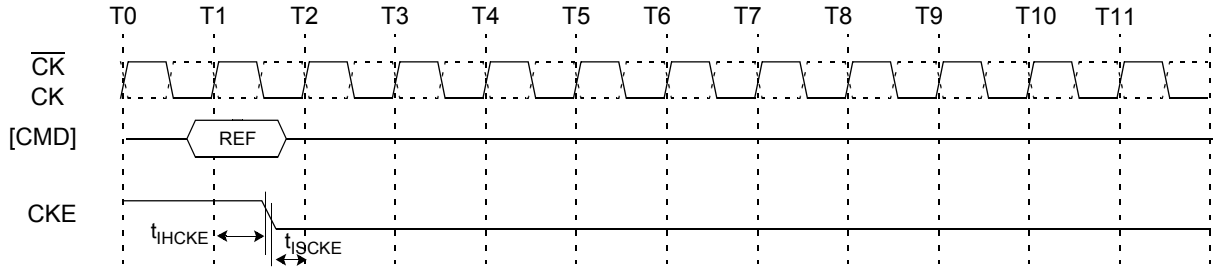


Figure 54: LPDDR2-S4: Refresh command to power-down entry

NOTE :
1) CKE may go LOW t_{IHCKE} after the clock on which the Refresh command is registered.

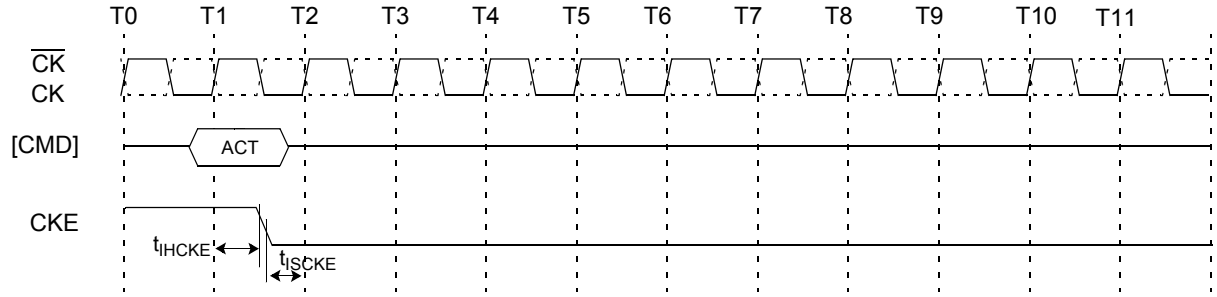


Figure 55: Activate command to power-down entry

NOTE:
1) CKE may go LOW t_{IHCKE} after the clock on which the Activate command is registered.

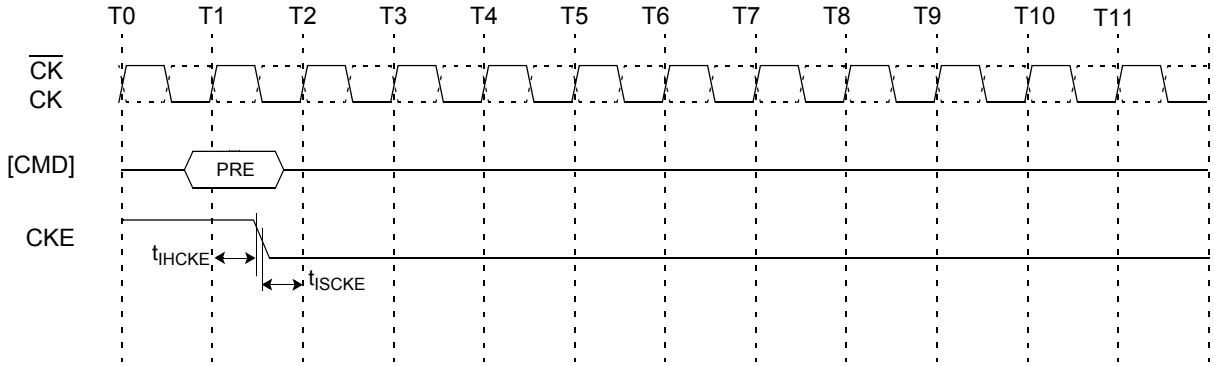


Figure 56: Precharge/Precharge-all command to power-down entry

NOTE :

1) CKE may go LOW tIHCKE after the clock on which the Precharge/Precharge-All command is registered.

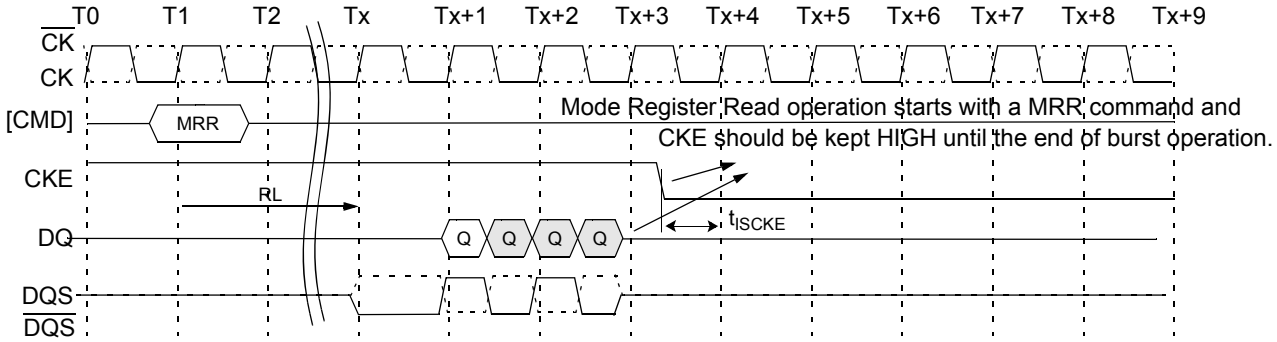


Figure 57: Mode Register Read to power-down entry

NOTE :
1) CKE may be registered LOW RL + RU($t_{DQSCK(MAX)}$/t_{CK})+ 4/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

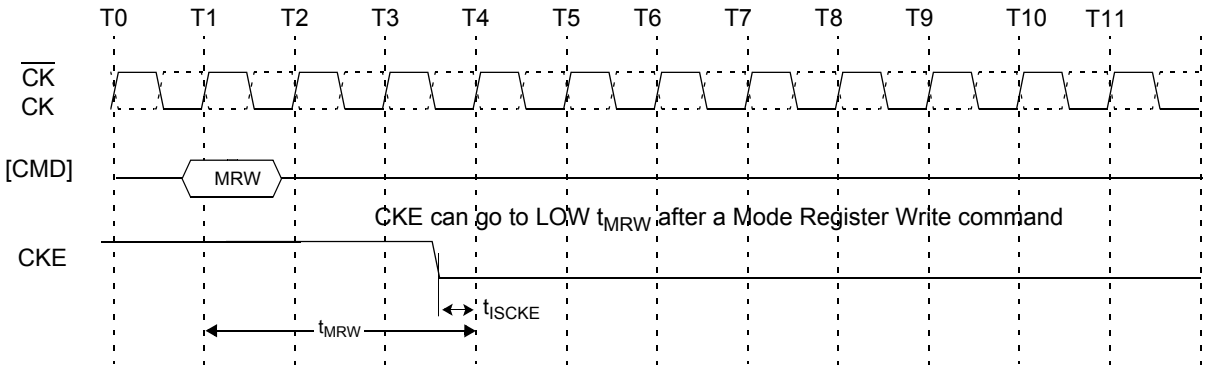


Figure 58: MRW command to power-down entry

NOTE :
1) CKE may be registered LOW t_{MRW} after the clock on which the Mode Register Write command is registered.

15.0 LPDDR2-S4: DEEP POWER-DOWN

Deep Power-Down is entered when CKE is registered LOW with $\overline{CS}$ LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.

All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (see "Absolute Maximum DC Rating" on specific datasheet). However prior to exiting Deep Power-Down, Vref must be within specified limits (see "Recommended DC Operating Conditions" on specific datasheet)

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting t_{ISCKE} with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

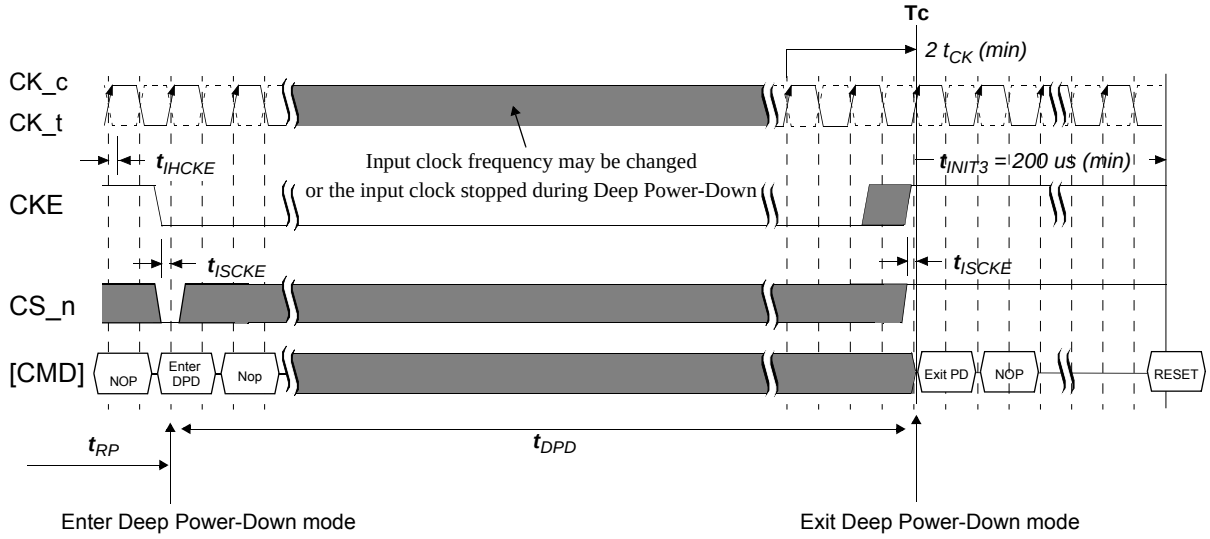


Figure 59: LPDDR2-S4: Deep power down entry and exit timing diagram

NOTE :
1) Initialization sequence may start at any time after Tc.
2) t_{INIT2}, t_{INIT3}, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see Chapter 1
3) Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

16.0 INPUT CLOCK STOP AND FREQUENCY CHANGE

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:

- CK is held LOW and $\overline{CK}$ is held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to changing the frequency;
- $\overline{CS}$ shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR2 device is ready for normal operation after the clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2tCK + tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:

- $\underline{CK}$ is held LOW and $\overline{CK}$ is held HIGH during clock stop;
- $\overline{CS}$ shall be held HIGH during clock clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD}, t_{WR}, t_{WRA}, t_{RP}, t_{MRW}, t_{MRR}, etc.) have been met prior to stopping the clock;
- The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2tCK + tXP.

17.0 NO OPERATION COMMAND

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. $\overline{CS}$ HIGH at the clock rising edge N.
2. $\overline{CS}$ LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.