KMS5U000KM-B308

MCP Specification

4GB e·MMC
+ 4Gb DDP(64M x32+ 64Mx32) Mobile DDR SDRAM

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	Initial issue. - 4GB e·MMC B-die_ Ver 0.0 - 4Gb DDP Mobile DDR SDRAM D-die_Ver 1.0	May. 09 , 2012	Preliminary	K.N.Kang
1.0	- Final datasheet.	May. 15 , 2012	Fianl	K.N.Kang

1. FEATURES

<Common>
• Operating Temperature : -25°C ~ 85°C
• Package : 153ball FBGA Type - 11.5 x 13 x 1.0mmt, 0.5mm pitch

<e·MMC>
MultiMediaCard System Specification Ver. 4.41 compatible. Detail description is referenced by JEDEC Standard
• SAMSUNG e·MMC supports below special features which are being discussed in JEDEC
- High Priority Interrupt scheme is supported
- Back ground operation is supported.
• Full backward compatibility with previous MultiMediaCard system (1bit data bus, multi-e·MMC systems)
• Data bus sidth :1bit(Default), 4bit and 8bit
• MMC I/F Clock Frequency : 0 ~ 52MHz
MMC I/F Boot Frequency : 0 ~ 52MHz
• Dual Data Rate mode is supported
• Power : Interface power → VDD = VCCQm(1.70V ~ 1.95V or 2.7V ~ 3.6V) , Memory power → VDDF = VCCm(2.7V ~ 3.6V)

<Mobile DDR SDRAM>
• VDD/VDDQ = 1.8V/1.8V
• Double-data-rate architecture; two data transfers per clock cycle.
• Bidirectional data strobe (DQS).
• Four banks operation.
• Differential clock inputs (CK and $\overline{CK}$).
• MRS cycle with address key programs.
- CAS Latency (3)
- Burst Length (2, 4, 8, 16)
- Burst Type (Sequential & Interleave)
• EMRS cycle with address key programs.
- Partial Array Self Refresh (Full, 1/2, 1/4 Array)
- Output Driver Strength Control (Full, 1/2, 1/4, 1/8, 3/4, 3/8, 5/8, 7/8)
• Internal Temperature Compensated Self Refresh.
• All inputs except data & DM are sampled at the positive going edge of the system clock (CK).
• Data I/O transactions on both edges of data strobe, DM for masking.
• Edge aligned data output, center aligned data input.
• No DLL; CK to DQS is not synchronized.
• DM for write masking only.
• Auto refresh duty cycle.
• 7.8us
•Clock Stop capability.

Operating Frequency

	DDR400
Speed @CL3[1)]	200MHz

NOTE :
1) CAS Latency

ADDRESS CONFIGURATION

Organization	$\overline{CS}$	CKE	Bank Address	Row Address	Column Address
64M x32	$\overline{CS}$0	CKE0	BA0, BA1	A0 - A13	A0 - A9
64M x32	$\overline{CS}$1	CKE1	BA0, BA1	A0 - A13	A0 - A9

2. GENERAL DESCRIPTION

The KMS5U000KM is a Multi Chip Package Memory which combines 4GB e·MMC and 4Gb DDP Mobile DDR synchronous high data rate Dynamic RAM.

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.5 which is a industry standard.
e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.
There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

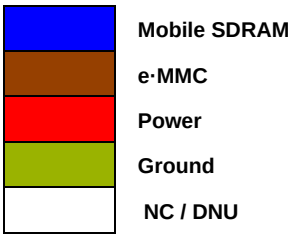
In 4Gb DDP Mobile DDR SDRAM, Synchronous design make a device controlled precisely with the use of system clock. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

The KMS5U000KM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 153-ball FBGA Type.

3. PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DNU	NC	DAT0m	DAT1m	DAT2m	NC	NC	VDDQd	VSSQd	VSSd	VDDd	VSSQd	NC	DNU
B	NC	DAT3m	DAT4m	DAT5m	DAT6m	DAT7m	DQ30d	DQ28d	DQ26d	DQ24d	DQS3d	DQ23d	VDDQd	NC
C	VSSd	VDDIm	A4d	VSSQm	NC	VCCQm	DQ31d	DQ29d	DQ27d	DQ25d	DM3d	DQ22d	DQ21d	VDDQd
D	A5d	A6d	A7d	NC								DQ19d	DQ20d	VSSQd
E	A12d	A11d	A8d		NC	VCCm	VSSm	NC	NC	NC		DQ18d	DQ17d	DQ16d
F	VDDd	A13d	A9d		VCCm					NC		DQS2d	DM2d	VSSQd
G	CKE0d	/CS0d	NC		VSSm					NC		CKd	VDDQd	VDDd
H	VDDQd	/RASd	/WEd		NC					VSSm		$\overline{CK}$d	VDDQd	VSSd
J	CKE1d	/CASd	/CS1d		NC					VCCm		DQS1d	DM1d	VSSQd
K	BA1d	VSSd	A10d		RSTm	NC	NC	VSSm	VCCm	NC		DQ13d	DQ14d	DQ15d
L	BA0d	A0d	A1d									DQ11d	DQ12d	VSSQd
M	VSSd	VDDd	A2d	VCCQm	CMDm	CLKm	DQ1d	DQ3d	DQ5d	DQ7d	DM0d	DQ9d	DQ10d	VDDQd
N	NC	VSSQm	A3d	VCCQm	VSSQm	VSSQd	DQ0d	DQ2d	DQ4d	DQ6d	DQS0d	DQ8d	VDDQd	NC
P	DNU	NC	VCCQm	VSSQm	VCCQm	VSSQm	NC	VDDQd	VSSQd	NC	VDDd	VSSQd	NC	DNU

153 FBGA: Top View (Ball Down)



4. PIN DESCRIPTION

Pin Name	Pin Function(Mobile SDRAM)
CKd,/CKd	System Differential Clock
CKEd,CKE1d	Clock Enable
/CS0d,/CS1d	Chip Selection
/RASd	Row Address Strobe
/CASd	Column Address Strobe
/WEd	Write Enable
A0d ~ A13d	Address Input
BA0d ~ BA1d	Bank Select Input
DM0d / DM3d	Data Input/Output Mask
DQS0d ~ DQS3d	Data Strobe
DQ0d ~ DQ31d	Data Input/Output
VDDd / VDDQd	Power Supply for Core / IOs
VSSd / VSSQd	Ground for Core / IOs

Pin Name	Pin Function(e·MMC)
DAT0m ~ DAT7m	Data Input/Output
CLKm	Clock
CMDm	Command
RSTm	H/W Reset
VSSm	Ground for Flash
VCCQm	Power Supply for Controller
VCCm	Power Supply for Flash
VSSQm	Ground for Controller
VDDIm	Should be connected to External Capacitance for Internal power stability

Pin Name	Pin Function
DNU	Do Not Use
NC	Not Connected

5. ORDERING INFORMATION

KM S 5 U 0 0 0 K M - B 308

Samsung
e·MCP

Device Type
S : e·MMC + SDRAM+ SDRAM

e·MMC Density & VCC & Org.
5: 4GByte, 32G, TLC, 3.3V, 1.8V~3.3V, x8

LSI
U : VHX01_PWD

NOR Flash Density & VCC & Org.
0 : NONE

NAND/OneNAND Density & VCC & Org
0 : NONE

UtRAM/SRAM Density & VCC & Org.
0 : NONE

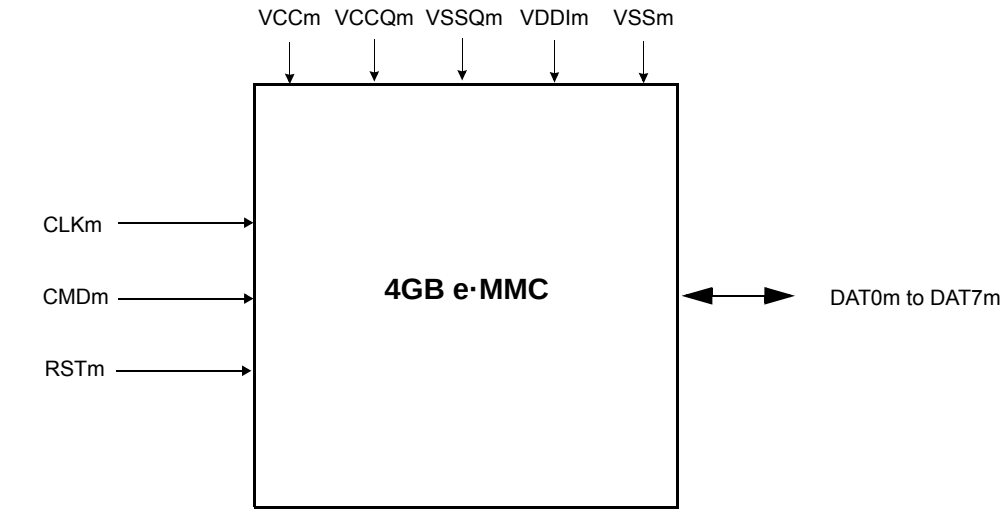
DRAM I/F & Density & VCC & Org.
K : MDDR*2, 2G*2, 1.8V/1.8V, x32

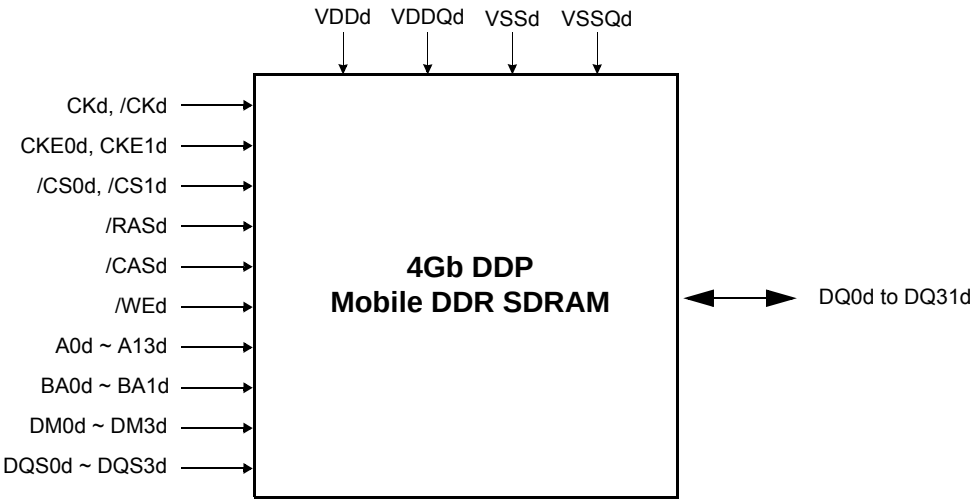
Generation
M: 1st Generation

Package
B : FBGA(HF, OSP LF)

308:
e·MMC = 19ns
Mobile DDR SDRAM = 5ns, 5ns

6. FUNCTIONAL BLOCK DIAGRAM

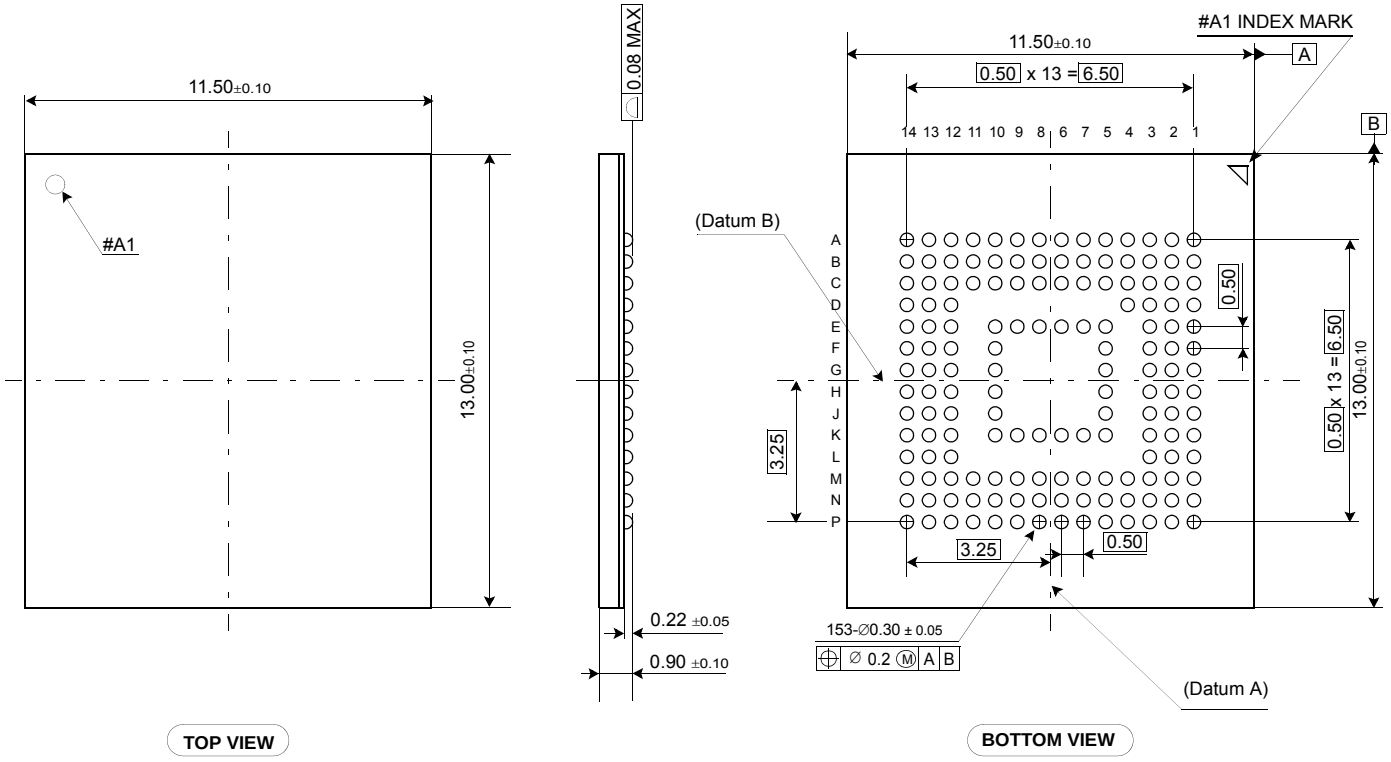




7. PACKAGE DIMENSION

153-Ball Fine pitch Ball Grid Array Package (measured in millimeters)

Units:millimeters



4GB e·MMC

1.0 Product Architecture

- e·MMC consists of NAND Flash and Controller. VDD is for Controller power and VDDF is for flash power

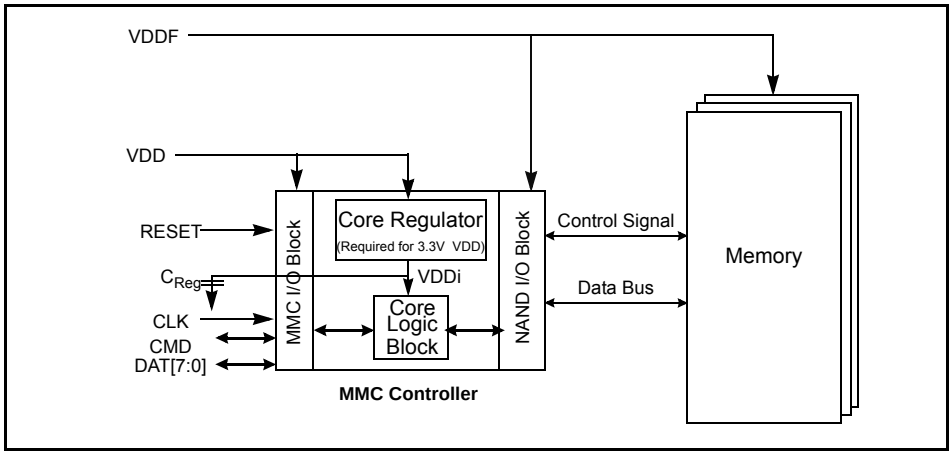


Figure 1. e·MMC Block Diagram

2.0 e.MMC 4.41 features

2.1 Data Write

Host can configure reliability mode to protect existing data per each partition.

This relibility mode has to be set before partitioning is completed.

This reliability setting only impacts the reliability of the main user area and the general purpose partitions.

[Table 1] EXT_CSD value for reliability setting in write operation

Name	Field	Size (Bytes)	Cell Type	EXT_CSD-slice	Value
Data Reliability Configuration	WR_REL_SET	1	R/W	[167]	0x1F
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Explanation of each field in the upper table is mentioned below

[Table 2] Definition of EXT_CSD value for reliability setting

Fields	Definitions
HS_CTRL_REL	0x0: All the WR_DATA_REL parameters in the WR_REL_SET registers are read only bits. 0x1: All the WR_DATA_REL parameters in the WR_REL_SET registers are R/W.
EN_REL_WR	0x0: The device supports the previous definition of reliable write. 0x1: The device supports the enhanced definition of reliable write

The below table shows each field for WE_REL_SET

[Table 3] Description of each field for WE_REL_SET

Name	Field	Bit	Size	Type
Write Data Reliability (user Area)	WR_DATA_REL_USR	0	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 1	WR_DATA_REL_1	1	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 2	WR_DATA_REL_2	2	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 3	WR_DATA_REL_3	3	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 4	WR_DATA_REL_4	4	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Reserved	-	7:5	-	-

2.2 Reliable Write

[Table 4] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Reliable write with EN_REL_WR is 0x1 supports atomicity of sector unit.

The block size defined by SET_BLOCKLEN (CMD16) is ignored and reliable write is executed as only 512 byte length. There is no limit on the size of the reliable write.

[Table 5] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	0x01

2.3 Secure Trim

Secure Trim operation consists of Secure Trim Step1 and Secure Trim Step2.
In Secure Trim Step 1 the host defines the range of write blocks that it would like to mark for the secure purge.

[Table 6] EXT_CSD value for secure trim

Field	Definitions	Value
SEC_TRIM_MULT	Secure Trim Step2 Timeout = 300ms x ERASE_TIMEOUT_MULT x SEC_TRIM_MULT	0x11

Area marked by Secure Trim Step1 is shown as EXT_CSD[181](ERASED_MEM_CONT) before Secure Trim Step2 is completed.

When Secure Trim Step2 is issued, if there is no data marked by Secure Trim Step1, Secure Trim Step2 does not work.

2.4 High Priority Interrupt

High Priority Interrupt is to stop ongoing operation and perform read operation with high priority

Command set for High Priority Interrupt operation is the below

[Table 7] Command List for High Priority Interrupt

CMD Index	Type	Argument	Resp	Abbreviation	Command Description
CMD12	ac	[31:16] – RCA* [15:1] – stuff bits [0] – High Priority Interrupt * *To be used only to send a High Priority Interrupt	R1b	STOP_TRANSMISSION	If High Priority Interrupt flag is set the device shall interrupt its internal operations in a well defined timing

Interruptible commands by read while write operation are the below.

[Table 8] List of Interruptible Command

Commands	Names	Notes
CMD24	WRITE SINGLE BLOCK	-
CMD25	WRITE MULTIPLE BLOCKS	-
CMD25	RELIABLE WRITE	Stopping a reliable write command with 'High Priority Interrupt' flag set turns that command into a reliable write command
CMD38	ERASE	-
	TRIM	-
	SECURE ERASE	-
	SECURE TRIM	-
CMD6	SWITCH	BACKGROUND OPERATION ONLY

[Table 9] EXT_CSD value for HPI

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
HPI features	HPI_FEATURES	1	R	[503]	0x03
Number of correctiy programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out of interrupt busytiming	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00

[Table 10] Definition of EXT_CSD value for HPI

Fields	Definitions
HPI_FEATURES	Bit 0 means HPI_SUPPORT Bit 0 = 0x0 : High Priority Interrupt mechanism not supported Bit 0 = 0x1 : High Priority Interrupt mechanism supported Bit 1 means HPI_IMPLEMENTATION 0x0 : HPI mechanism implementation based on CMD13 0x1 : HPI mechanism implementation based on CMD12
CORRECTLY_PRG_SECTOR_NUM	This field indicates how many 512B sectors were successfully programmed by the last WRITE_MULTIPLE_BLOCK command (CMD25). CORRECTLY_PRG_SECTORS_NUM=EXT_CSD[242]*2^0+EXT_CSD[243]*2^8 +EXT_CSD[244]*2^16 + EXT_CSD[245]*2^24
PARTITION_SWITCH_TIME	This field indicates the maximum timeout for the SWITCH command (CMD6) when switching partitions by changing PARTITION_ACCESS bits in PARTITION_CONFIG field (EXT_CSD byte [179]). Time is expressed in units of 10 milliseconds
OUT_OF_INTERRUPT_TIME	This field indicates the maximum timeout to close a command interrupted by HPI - time between the end bit of CMD12 / CMD 13 to the DAT0 release by the device.
HPI_MGMT	Bit 0 means HPI_EN 0x0 : HPI mechanism not activated by the host 0x1 : HPI mechanism activated by the host

2.5 Background Operation

When the host is not being serviced, e·MMC can do internal operation by using “Background Operation” command. In this operation which takes long time to complete can be handled later when host ensure enough idle time (In Back ground operation)

Background Operation Sequence is the following

[Table 11] Background Operation Sequence

Function	Command	Description
Background Operation Check	CMD8 Or Card Status Register	If BKOPS_STATUS is not 0 or 6th bit of card status register is set, there are something to be performed by background operation
Background Operation Start	CMD6	Background operation starts by BKOPS_START is set to any value. When background operation is completed BKOPS_STATUS is set to 0 and BKOPS_START is set to 0.
Background Operation Stop	HPI	If the background operation is stopped BKOPS_START is set to 0

[Table 12] EXT_CSD value for Background Operation

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
Background operations Support	BKOPS_SUPPORT	1	R	[502]	0x01
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations hand shake	BKOP_EN	1	R/W	[163]	0x00

[Table 13] Definition of EXT_CSD value for Bakgrourd Operation

Fields	Definitions
BKOPS_SUPPORT	‘0’ means Background operation is not supported ‘1’ means Background operation is supported
BKOPS_ STATUS	‘0’ means No background work pending ‘1’ means pending background work existing. ‘2’ means pending background work existing & performance being impacted. ‘3’ means pending background work existing & critical
BKOPS_START	Background operation start while BKOPS_START is set to any value. ‘0’ means Background operation is enabled.
BKOPS_EN	‘0’ means host does not support background operation ‘1’ means host use background operation manually

[Table 14] Card Status Register for Background Operation

Bits	Identifier	Type	Det Mode	Value	Description	Clear Cond
6	URGENT_BKOPS	S	R	“0” = Not Urgent “1” = Urgent	If set, device needs to perform background operations urgently. Host can check EXT_CSD field BKOPS_STATUS for the detailed level (in case of BKOPS_STATUS is 2 or 3)	A

3.0 Technical Notes

3.1 S/W Agorithm

3.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

3.1.1.1 Boot Area Partition and RPMB Area Partition

Default size of each Boot Area Partition is 2,048KB and can be changed by Vendor Command as multiple of 512KB.
Default size of RPMB Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB.

Boot Partition size & RPMB Partition Size are set by the following command sequence :

[Table 15] Setting sequence of Boot Area Partition size and RPMB Area Partition size

Function	Command	Description
Partition Size Change Mode	CMD62(0xEFAC62EC)	Enter the Partition Size Change Mode
Partition Size Set Mode	CMD62(0x00CBAEA7)	Partition Size setting mode
Set Boot Partition Size	CMD62(BOOT_SIZE_MULTI)	Boot Partition Size value
Set RPMB Partition Size	CMD62(RPMB_SIZE_MULTI)	RPMB Partition Size value F/W Re-Partition is executed in this step.
Power Cycle		

Boot partition size is calculated as (128KB * BOOT_SIZE_MULTI)
BOOT_SIZE_MULTI should be set as multiple of 8.
The size of Boot Area Partition 1 and 2 can not be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULTI).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

[Table 16] REL_WR_SEC_C value for write operation on RPMB partition

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is ‘0x00’.

3.1.1.2 Enhanced Partition (Area)

SAMSUNG e·MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

3.1.2 Write protect management

In order to allow the host to protect data against erase or write, the device shall support write protect commands.

3.1.2.1 User Area Write Protection

TMP_WRITE_PROTECT (CSD[12]) and PERM_WRITE_PROTECT(CSD[13]) registers allow the host to apply write protection to whole device including Boot Partition, RPMB Partition and User Area.

[Table 17] whole device write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

USER_WP (EXT_CSD[171]) register allows the host to apply write protection to all the partitions in the user area.

[Table 18] User area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

The host has the ability to check the write protection status of segments by using the SEND_WRITE_PROT_TYPE command (CMD31). When full card protection is enabled all the segments will be shown as having permanent protection.

3.1.2.2 Boot Partition Write Protection

BOOT_WP (EXT_CSD [173]) register allows the host to apply write protection to Boot Area Partitions.

[Table 19] Boot area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset

An attempt to set both the disable and enable bit for a given protection mode (permanent or power-on) in a single switch command will have no impact and switch error occurs.
Setting both B_PERM_WP_EN and B_PWR_WP_EN will result in the boot area being permanently protected.

3.1.3 Boot operation

Device supports not only boot mode but also alternative boot mode.
Device supports high speed timing and dual data rate during boot

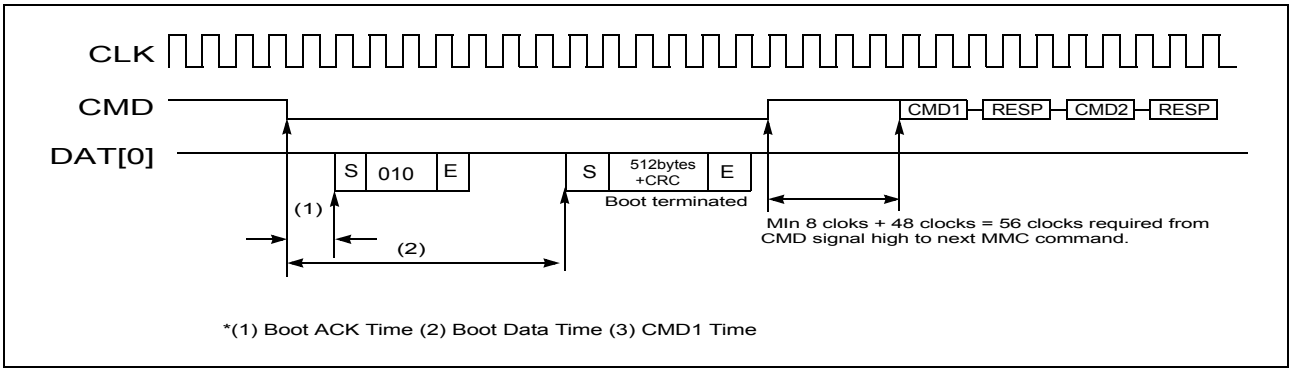


Figure 2. MultiMediaCard state diagram (boot mode)

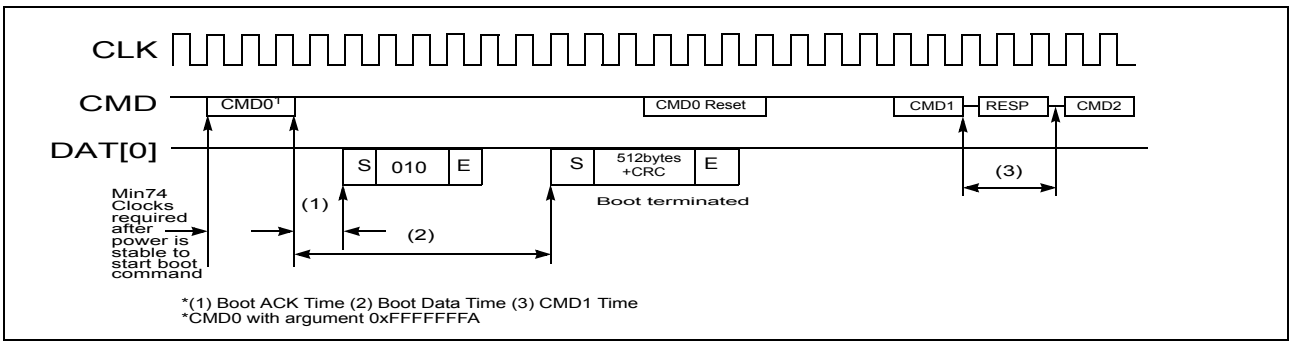


Figure 3. MultiMediaCard state diagram (alternative boot mode)

[Table 20] Boot ack, boot data and initialization Time

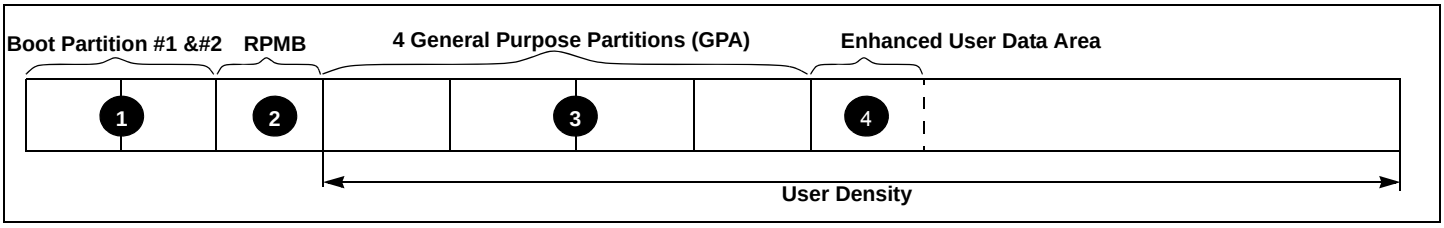
Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 60 ms
(3) Initialization Time[1)]	< 3 secs

NOTE:
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 300ms

Minimum function for reading boot data is initialized during boot time and after that full function is initialized during initialization time.

3.1.4 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 96MB in TLC.
This results in decreasing of user density



[Table 21] Capacity according to partition

	Boot partition 1	Boot partition 2	RPMB
Min.	2,048KB	2,048KB	128KB
Max.	4,096KB	4,096KB	4,096KB

[Table 22] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
4 GB	TBD

[Table 23] User Density Size

Device	User Density Size
4 GB	3,909,091,328 Bytes

3.1.5 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

[Table 24] Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 25] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
GotoSleep Time	< 1ms	< 1ms

3.1.6 End of Life Management

The end of device life time is defined when there is no more available reserved block for bad block management in the device. When the deivice reaches to end of its life time, device shall change its state to permanent write protection state. In this case, write operation is not allowed any more but read operation are still allowed.
But, reliability of the operation can not be guaranteed after end of life

3.1.7 Performance

[Table 26] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
4 GB	60	6

* Test/ Estimation Condition : Bus width x8, 52MHz DDR, 4MB data transfer, w/o file system overhead

4.0 REGISTER VALUE

4.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by all e·MMCs.

[Table 27] OCR Register

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	e·MMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the e·MMC has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

4.2 CID Register

[Table 28] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	---[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	---[2]
Product serial number	PSN	32	[47:16]	---[3]
Manufacturing date	MDT	8	[15:8]	---[4]
CRC7 checksum	CRC	7	[7:1]	---[5]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as e.MMC JEDEC standard
2) PRV is composed of the revision count of controller and the revision count of F/W patch
3) A 32 bits unsigned binary integer. (Random Number)

4.2.1 Product name table (In CID Register)

[Table 29] Product name

Part Number	Density	Product Name in CID Register (PNM)
KMS5U000KM-B308	4 GB	0 x53355530304D

4.3 CSD Register

The Card-Specific Data register provides information on how to access the e·MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 30] CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value
					4GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	-	2	R	[75:74]	-
Card size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06
Card size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x1F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x02
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	-
Not used, always '1'	-	1	-	[0:0]	-

4.4 Extended CSD Register

The Extended CSD register defines the e·MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e·MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e·MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 31] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value
					4GB
Properties Segment					
Reserved[1]		7	-	[511:505]	-
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x03
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Reserved[1]		255	-	[501:247]	-
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
I st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Reserved[1]		1	-	[240]	-
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Reserved[1]		2	-	[237:236]	-
Minimum Write Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved[1]		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x15
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved[1]		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x10
Access size	ACC_SIZE	1	R	[225]	0x06
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x1E
Sleep current (VDDF)	S_C_VDDF	1	R	[220]	0x07
Sleep current (VDD)	S_C_VDD	1	R	[219]	0x07
Reserved[1]		1	-	[218]	-
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Reserved[1]		1	-	[216]	-
Sector Count	SEC_COUNT	4	R	[215:212]	0x748000

Reserved[1]		1	-	[211]	-
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved[1]		1	-	[204]	-
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	0x00
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	0x00
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	0x00
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02
Reserved[1]		1	-	[197]	-
Card Type	CARD_TYPE	1	R	[196]	0x07
Reserved[1]		1	-	[195]	-
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved[1]		1	-	[193]	-
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x05
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved[1]		1	-	[190]	-
Command Set Revision	CMD_SET_REV	1	R	[189]	0x00
Reserved[1]		1	-	[188]	-
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved[1]		1	-	[186]	-
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved[1]		1	-	[184]	-
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved[1]		1	-	[182]	-
Erased Memory Content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved[1]		1	-	[180]	-
Partition configurationn	PARTITION_CONFIG	1	R/W/E& R/W/E_P	[179]	0x00
Boot config proteetion	BOOT_CONFIG_PRPT	1	R/W & R/W/C_P	[178]	0x00
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	0x00
Reserved[1]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Reserved[1]		1	-	[174]	-
Boot area write proection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved[1]		1	-	[172]	-
User area write protection register	USER_WP	1	R/W, R/W/C_P& R/W/E_P	[171]	0x00
Reserved[1]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00

RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x01
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x05
Reserved[1]		1	-	[165]	-
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitoning support	RARTITIONING_SUPPORT	1	R	[160]	0x03
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	TBD
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Paritioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved[1]		1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMT	1	R/W	[134]	0x00
Reserved[1]		134	-	[133:0]	-

NOTE :
1) Reserved bits should be read as "0."

5.0 AC PARAMETER

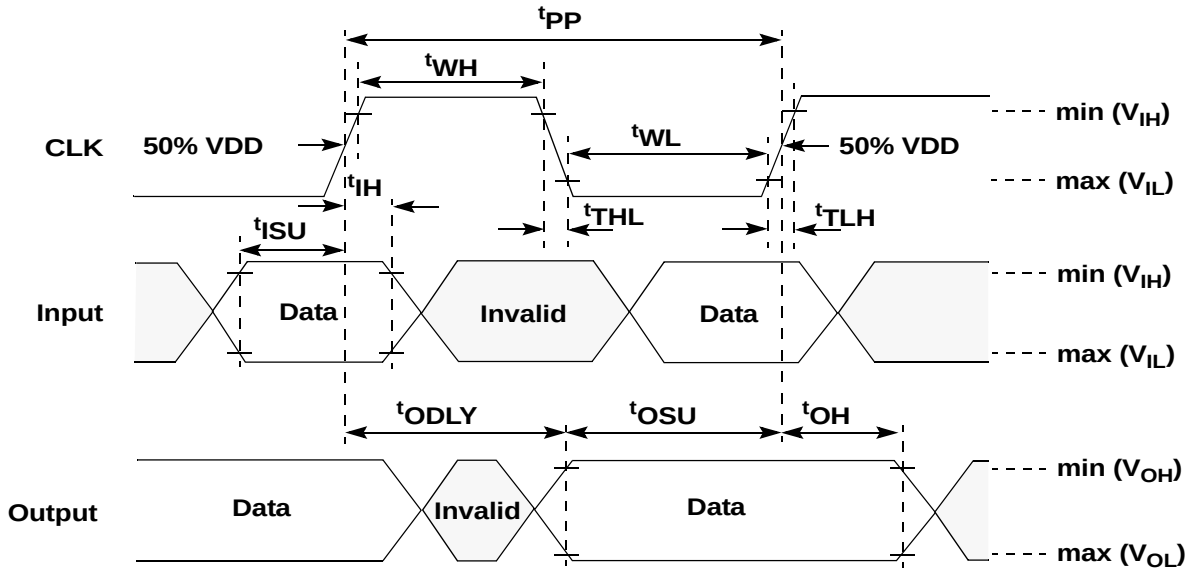
5.1 Time Parameter

[Table 32] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal 1)	300	ms
	After partition setting 2)	3	s
Read Timeout		100	ms
Write Timeout		350(TBD)	ms
Erase Timeout		15	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout 3)		600	ms
Partition Switching Timeout (after Init)		100	us

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 6.4 EXT_CSD register
3) If 8KB Size and Address are aligned, Max. Timeout value is 300ms

5.2 Bus Timing Parameter



Data must always be sampled on the rising edge of the clock.

Figure 4. Bus signal levels

[Table 33] Default (under 26MHz)

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[2]					
Clock frequency Data Transfer Mode3	fPP	0[4]	26	MHz	CL <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode	f_{OD}	0[4]	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock high time	t_{WH}	10			
Clock rise time[5]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF

NOTE :
1)The card must always start with the backward-compatible interface timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VDD.
3) For compatibility with cards that suport the v4.2 standard or earlier verison, host should not use>20MHz before switching to high-speed interface timing.
4) Frequency is periodically sampled and is not 100% tested.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

[Table 34] High-Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[1]					
Clock frequency Data Transfer Mode[2]	f_{PP}	0[3]	52[4)]	MHz	C_L <= 30 pF
Clock frequency Identification Mode	f_{OD}	0[3]	400	kHz	CL <= 30 pF
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock High time	t_{WH}	6.5		ns	C_L <= 30 pF
Clock rise time[5]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	CL <= 30 pF
Output hold time	t_{OH}	2.5			C_L <= 30 pF
Signal rise time	t_{RISE}		3	ns	C_L <= 30 pF
Signal fall time	t_{FALL}		3	ns	C_L <= 30 pF

NOTE :
1) CLK timing is measured at 50% of VDD.
2) A MultiMediaCard shall support the full frequency range from 0-26MHz, or 0-52MHz
3) Frequency is periodically sampled and is not 100% tested.
4) Card can operate as high-speed card interface timing at 26MHz clock frequency.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).6) Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

5.3 Bus timing for DAT signals during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK.The CMD signal still operates synchronously of the rising edge of CLK and there fore it complies with the bus timing specified in chapter 7.2, Therefore there is no timing change for the CMD signal

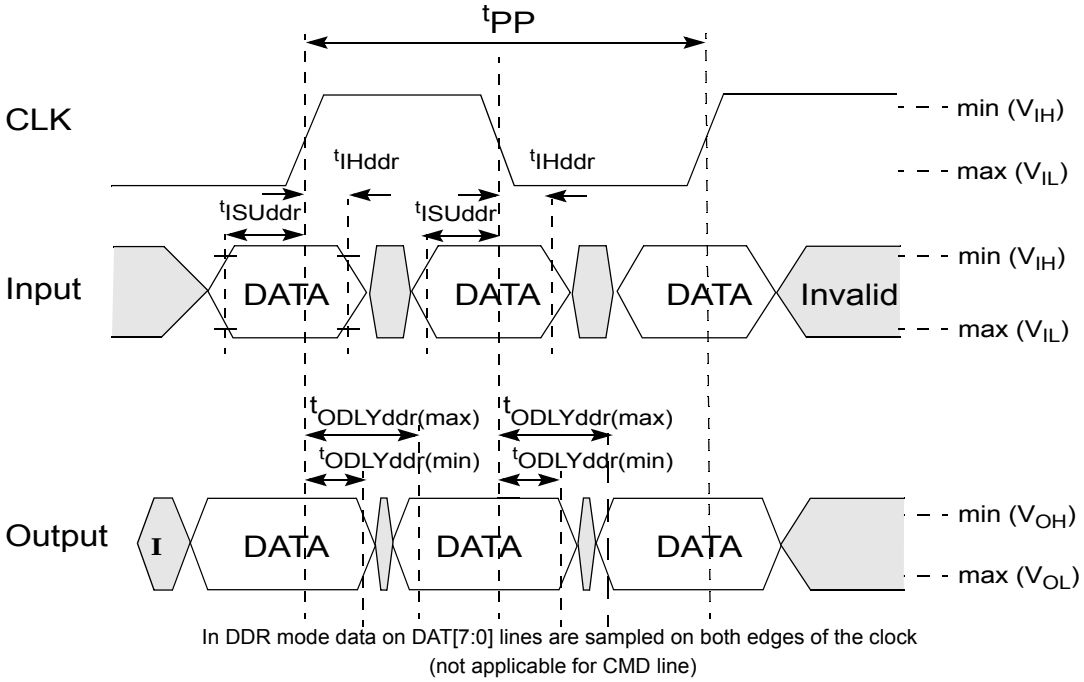


Figure 5. Timing diagram: data input/output in dual data rate mode

5.3.1 Dual data rate interface timings

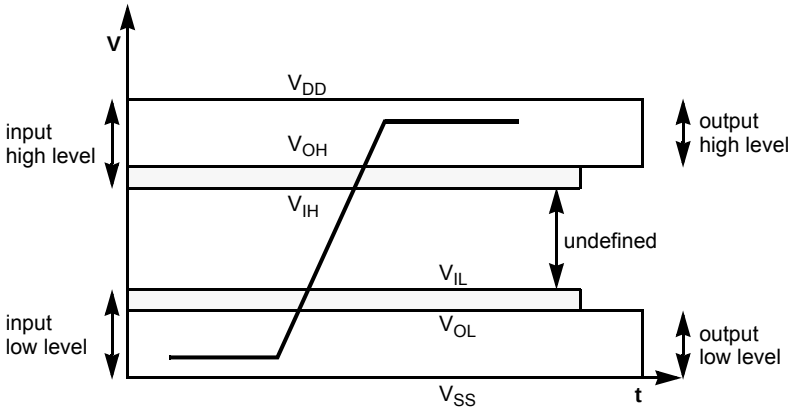
[Table 35] High-speed dual rate interface timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

NOTE :
1) CLK timing is measuted at 50% of VDD
2) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max(V_{IL}), and outputs CMD,DATrise and fall times measured by min(V_{OH}) and max(V_{OL})

5.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



5.4.1 Open-drain mode bus signal level

[Table 36] Open-drain bus signal level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2		V	I_{OH} = -100 uA
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

5.4.2 Push-pull mode bus signal level.high-voltage MultiMediaCard

To meet the requirements of the JEDEC standard JESD8C.01, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

[Table 37] Push-pull signal level.high-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -100 uA@V_{DD} min
Output LOW voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100 uA@V_{DD} min
Input HIGH voltage	V_{IH}	0.625*V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{DD}	V	

5.4.3 Push-pull mode bus signal level.dual-voltage MultiMediaCard

The definition of the I/O signal levels for the Dual voltage MultiMediaCard changes as a function of V_{DD}.

- 2.7V - 3.6V: Identical to the High Voltage MultiMediaCard (refer to Chapter 5.4.2 on page29 above).
- 1.95V - 2.7V: Undefined. The card is not operating at this voltage range.
- 1.70V - 1.95V: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

[Table 38] Push-pull signal level—dual-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.45V		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{DD} 1)	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{DD} 2)	V	

NOTE:
1) 0.7*V_{DD} for MMC4.3 and older revisions.
2) 0.3*V_{DD} for MMC4.3 and older revisions.

5.4.4 Push-pull mode bus signal level.e·MMC

The definition of the I/O signal levels for the e·MMC devices changes as a function of VCCQ.

- 2.7V-3.6: Identical to the High Voltage MultiMediaCard (refer to Chapter 5.4.2 on page29).
- 1.95- 2.7V: Undefined. The e·MMCdevice is not operating at this voltage range.
- 1.65V-1.95V: Identical to the 1.8V range for the Dual Voltage MultiMediaCard (refer to Chapter 5.4.3 on page29).
- 1.3V - 1.65V: Undefined. The e·MMC device is not operating at this voltage range.
- 1.1V-1.3V: Compatible with EIA/JEDEC Standard “JESD8-12A.01 normal range: as defined in the following table.

[Table 39] Push-pull signal level.1.1V-1.3V VCCQ range e·MMC

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	$0.75V_{CCQ}$		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		$0.25V_{CCQ}$	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	$0.65*V_{CCQ}$	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	$0.35*V_{CCQ}$	V	

6.0 DC PARAMETER

6.1 Active Power Consumption during operation

[Table 40] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
4GB	32Gb TLC x 1	100	50	mA

* Power Measurement conditions: Bus configuration =x8 @52MHz
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

6.2 Standby Power Consumption in auto power saving mode and standby state

[Table 41] Standby Power Consumption in auto power saving mode and standby state

Density	NAND Type	CTRL		NAND		Unit
		25°C(Typ)	85°C	25°C(Typ)	85°C	
4GB	32Gb TLC x 1	100	250	50 (TBD)	85 (TBD)	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 @52MHz , No CLK
*Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

6.3 Sleep Power Consumption in Sleep State

[Table 42] Sleep Power Consumption in Sleep State

Density	NAND Type	CTRL		NAND	Unit
		25°C(Typ)	85°C		
4GB	32Gb TLC x 1	100	250	0[1)]	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 @52MHz ,
1) In auto power saving mode , NAND power can not be turned off .However in sleep mode NAND power can be turned off. If NAND power is alive , NAND power is same with that of the Standby state.

6.4 Supply Voltage

[Table 43] Supply Voltage

Item	Min	Max	Unit
VDD	1.70 (2.7)	1.95 (3.6)	V
VDDF	2.7	3.6	V
Vss	-0.5	0.5	V

6.5 Bus Operating Conditions

[Table 44] Bus Operating Conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	3.6	V
Input Leakage Current	-2	2	μA
Output Leakage Current	-2	2	μA

6.6 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{movi} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 45] Bus Signal Line Load

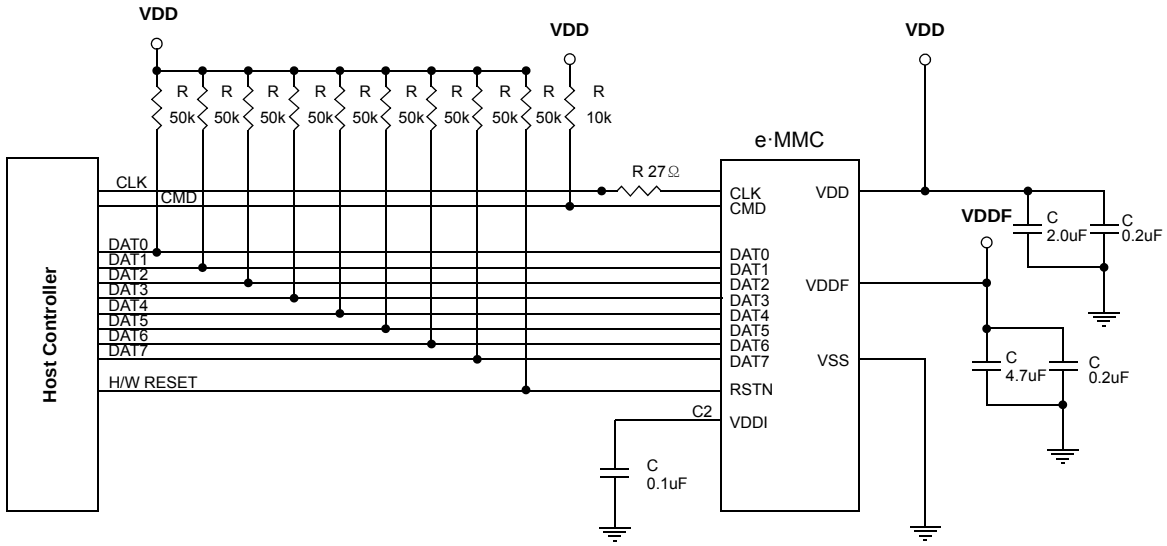
Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single e·MMC capacitance	C_{BGA}		7	12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

A. e·MMC Connection Guide

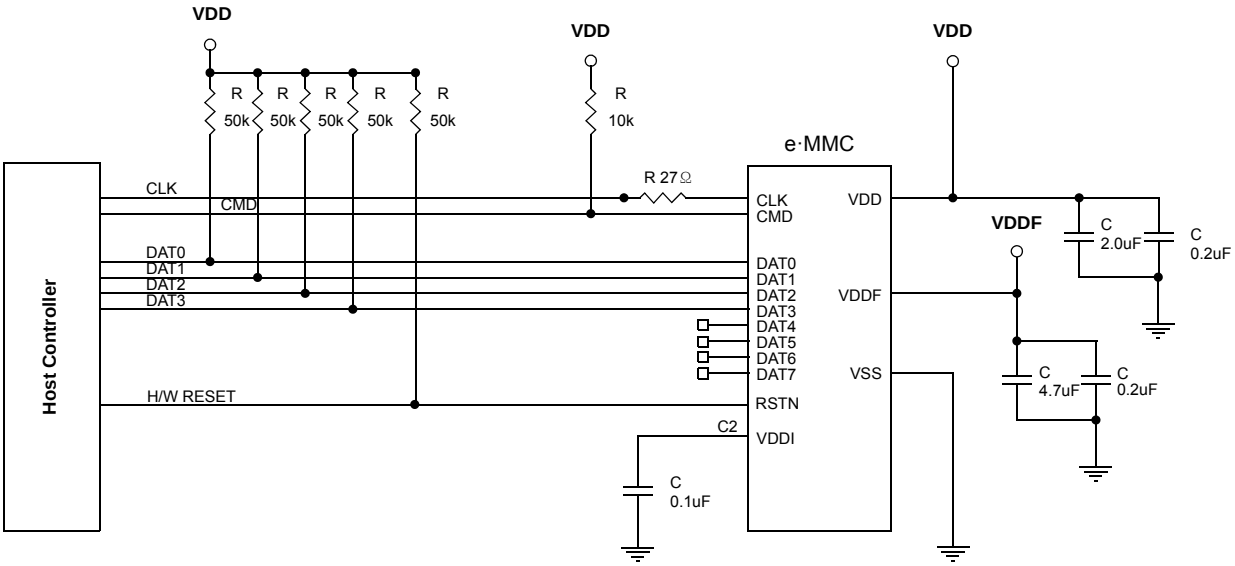
This Connection guide is an example for customers to adopt e·MMC more easily

- This appendix is just guideline for e·MMC connection. This value and schematic can be changed depending on the system environment.
- Coupling capacitor should be connected with VDD and VSS as closely as possible.
- VDDI Capacitor is min 0.1uF
- Impedance on CLK match is needed.
- SAMSUNG recommends 27Ω for resistance on CLK line. However 0Ω ~47Ω is also available.
- If host does not have a plan to use H/W reset, it is not needed to put 50KΩ pull-up resistance on H/W rest line.
- SMASUNG Recommends to separate VDD and VDDF power.

A.1 x8 support Host connection Guide

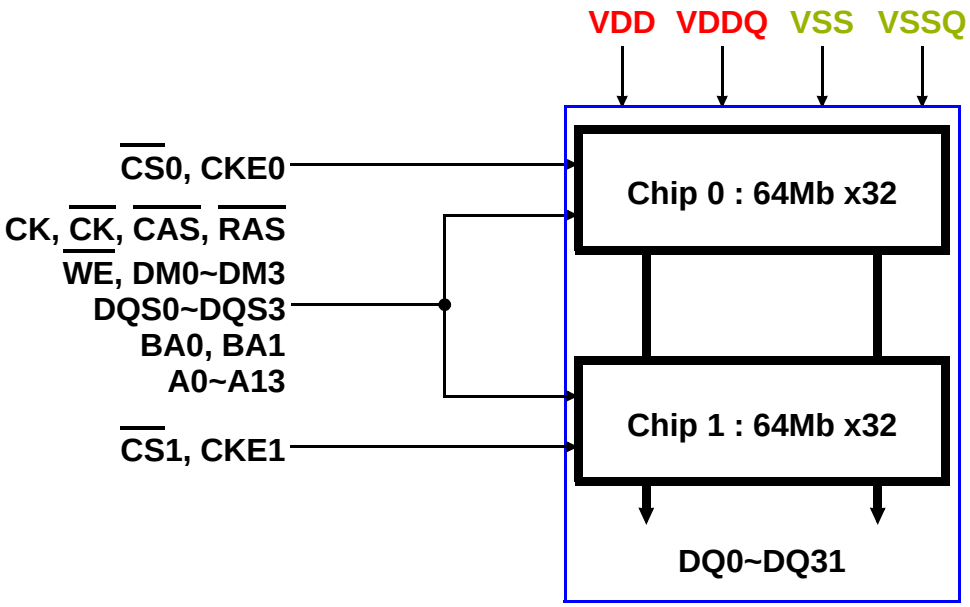


A.2 x4 support Host connection Guide



4Gb DDP(64M x32+ 64Mx32) Mobile DDR SDRAM

1.0 FUNCTIONAL BLOCK DIAGRAM



2.0 FUNCTIONAL DESCRIPTION

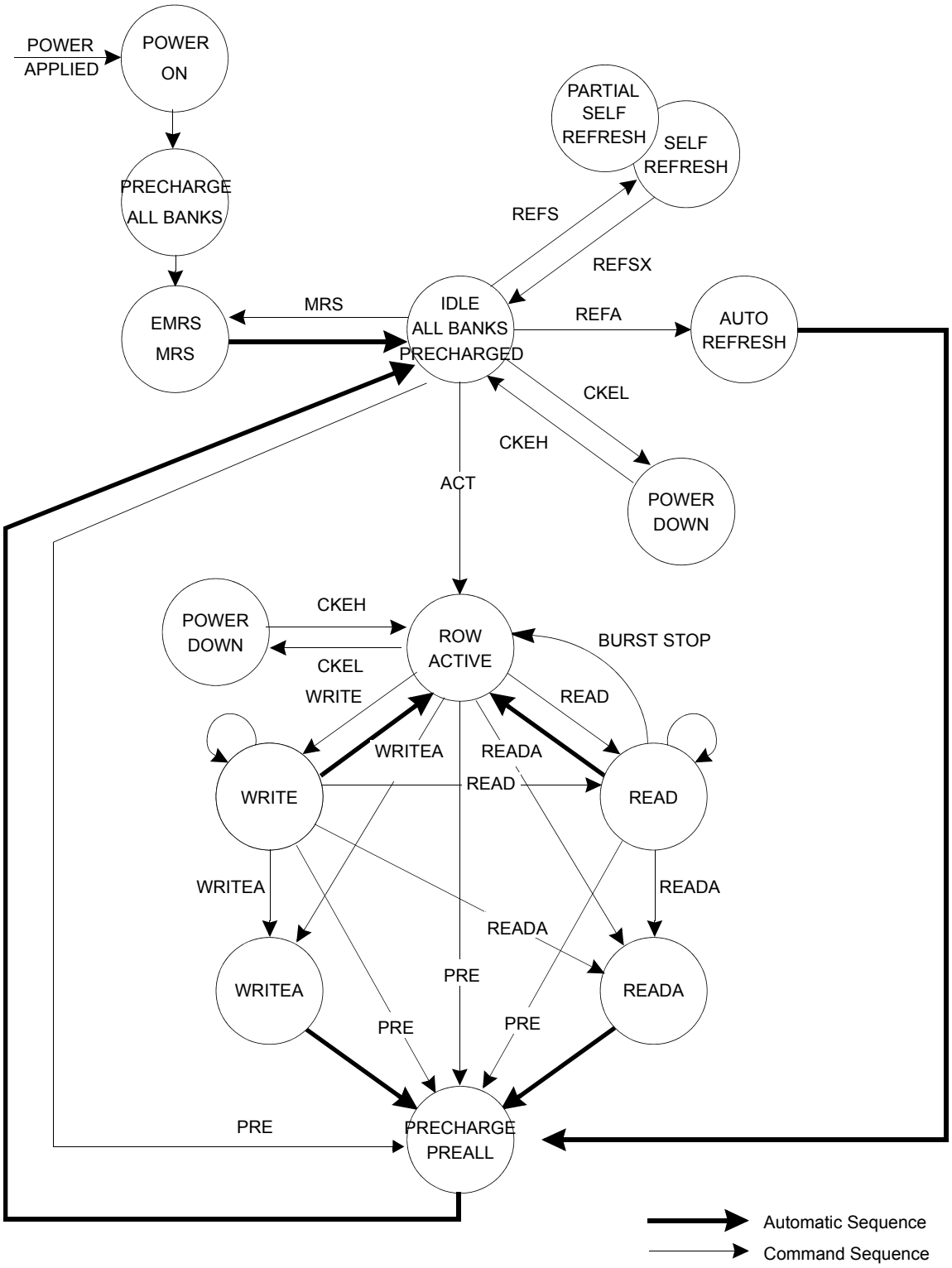
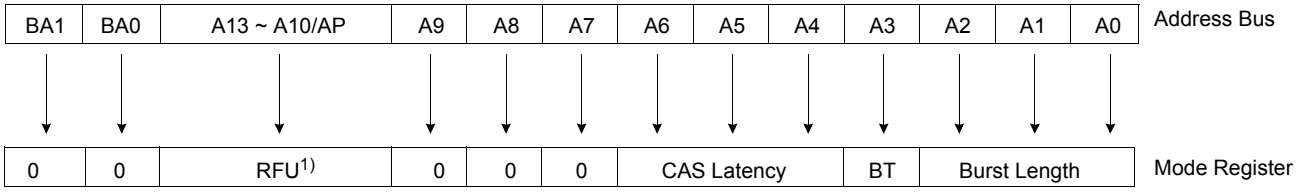


Figure 1. State diagram

3.0 MODE REGISTER DEFINITION

3.1 Mode Register Set (MRS)

The mode register is designed to support the various operating modes of Mobile DDR SDRAM. It includes Cas latency, addressing mode, burst length, test mode and vendor specific options to make Mobile DDR SDRAM useful for variety of applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The Mobile DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The states of address pins A0 ~ A13 and BA0, BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the mode register. Two clock cycles are required to complete the write operation in the mode register. Even if the power-up sequence is finished and some read or write operation is executed afterward, the mode register contents can be changed with the same command and two clock cycles. This command must be issued only when all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, Cas latency (read latency from column address) uses A4 ~ A6, A7 ~ A13 is used for test mode. BA0 and BA1 must be set to low for proper MRS operation.



A_3	Burst Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Type
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Figure 2. Mode Register Set

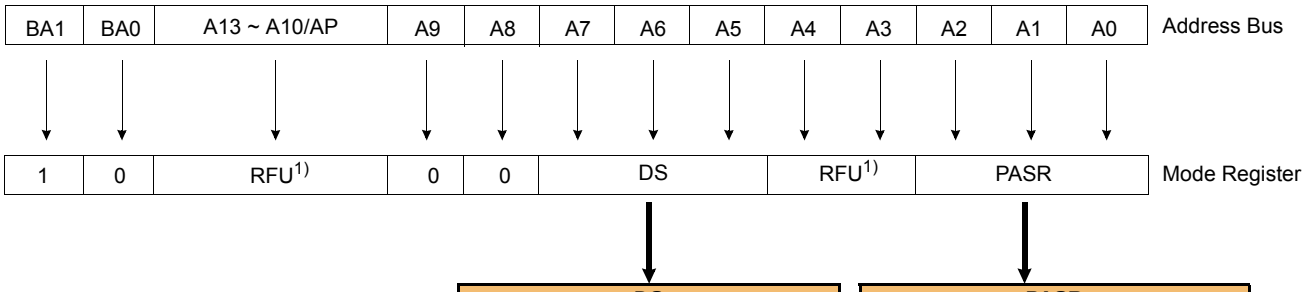
NOTE :
1) RFU (Reserved for future use) should stay "0" during MRS cycle

[Table 1] Burst address ordering for burst length

Burst Length	Starting Address (A3, A2, A1, A0)	Sequential Mode	Interleave Mode
2	xxx0	0, 1	0, 1
	xxx1	1, 0	1, 0
4	xx00	0, 1, 2, 3	0, 1, 2, 3
	xx01	1, 2, 3, 0	1, 0, 3, 2
	xx10	2, 3, 0, 1	2, 3, 0, 1
	xx11	3, 0, 1, 2	3, 2, 1, 0
8	x000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	x001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	x010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	x011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	x100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	x101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	x110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	x111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0000	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15
	0001	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11,10,13,12,15,14
	0010	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1	2, 3, 0, 1, 6, 7, 4, 5,10,11, 8, 9, 14,15,12,13
	0011	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4,11,10, 9, 8, 15,14,13,12
	0100	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3,12,13,14,15, 8, 9, 10,11
	0101	5, 6, 7,8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2,13,12,15,14, 9, 8,11,10
	0110	6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1,14,15,12,13,10,11, 8, 9
	0111	7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, 15,14,13,12,11,10, 9, 8
	1000	8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7	8, 9,10,11,12,13,14,15, 0, 1, 2, 3, 4, 5, 6, 7
	1001	9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, 11,10,13,12,15,14,1, 0, 3, 2, 5, 4, 7, 6
	1010	10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	10,11, 8, 9, 14,15,12,13, 2, 3, 0, 1, 6, 7, 4, 5
	1011	11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11,10, 9, 8, 15,14,13,12, 3, 2, 1, 0, 7, 6, 5, 4
	1100	12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	12,13,14,15, 8, 9, 10,11, 4, 5, 6, 7, 0, 1, 2, 3
	1101	13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11,12	13,12,15,14, 9, 8,11,10, 5, 4, 7, 6, 1, 0, 3, 2
	1110	14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	14,15,12,13,10,11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
	1111	15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	15,14,13,12,11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

3.2 Extended Mode Register Set (EMRS)

The extended mode register is designed to support for the desired operating modes of DDR SDRAM. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1, low on BA0(The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A13 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and two clock cycles. But this command must be issued only when all banks are in the idle state. A0 - A2 are used for partial array self refresh and A5 - A7 are used for driver strength control. "High" on BA1 and "Low" on BA0 are used for EMRS. All the other address pins except A0,A1,A2,A5,A6,A7, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



DS			
A_7	A_6	A_5	Driver Strength
0	0	0	Full
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	3/4
1	0	1	3/8
1	1	0	5/8
1	1	1	7/8

PASR			
A_2	A_1	A_0	Refreshed Area
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Figure 3. Extended Mode Register Set

NOTE :
1) RFU (Reserved for future use) should stay "0" during EMRS cycle

3.3 Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, this Mobile DRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the real device temperature.

2. TCSR ranges for IDD6 shown in the table are only examples.

3. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

Temperature Range	Self Refresh Current (IDD6)			Unit
	Full Array	1/2 Array	1/4 Array	
85 °C	3400	2800	2400	uA
45 °C	800	540	400	

NOTE :
1) IDD6 85°C is guaranteed, IDD6 45°C is typical value.

3.4 Partial Array Self Refresh (PASR)

1. In order to save power consumption, Mobile DDR SDRAM includes PASR option.
2. Mobile DDR SDRAM supports three kinds of PASR in self refresh mode; Full array, 1/2 Array, 1/4 Array.

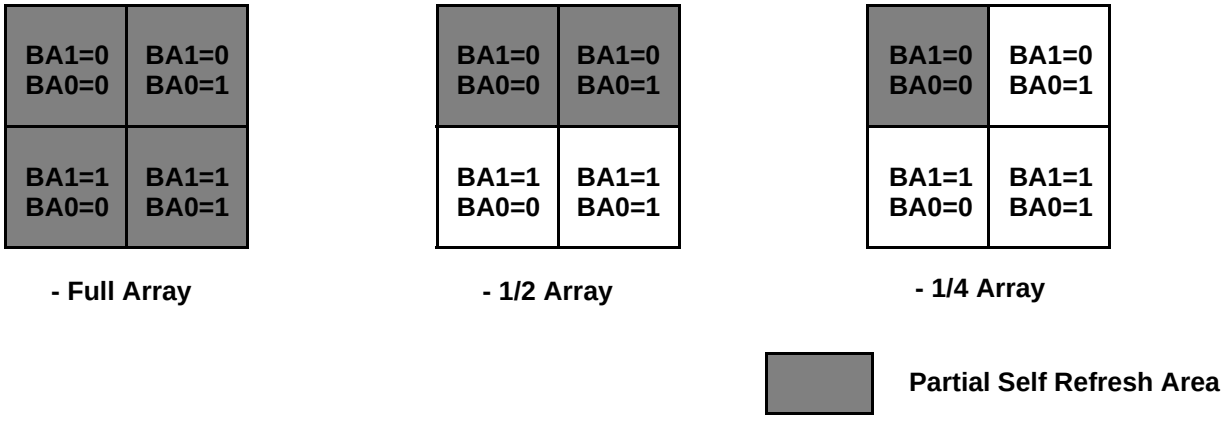


Figure 4. EMRS code and TCSR, PASR

4.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	- 0.5 ~ 2.7	V
Voltage on VDD supply relative to VSS	VDD	- 0.5 ~ 2.7	V
Voltage on VDDQ supply relative to VSS	VDDQ	- 0.5 ~ 2.7	V
Storage temperature	T_{STG}	- 55 ~ + 150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTE :
1) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2) Functional operation should be restricted to recommend operation condition.
3) Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

5.0 DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS=0V, T_C = -25°C to 85°C)

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage (for device with a nominal VDD of 1.8V)		VDD	1.7	1.95	V	1
I/O Supply voltage		VDDQ	1.7	1.95	V	1
Input logic high voltage	Address	V_{IH}(DC)	0.8 x VDDQ	VDDQ + 0.3	V	2
	Data		0.7 x VDDQ	VDDQ + 0.3	V	
Input logic low voltage	Address	V_{IL}(DC)	-0.3	0.2 x VDDQ	V	2
	Data		-0.3	0.3 x VDDQ	V	
Output logic high voltage		V_{OH}(DC)	0.9 x VDDQ	-	V	I_{OH} = - 0.1mA
Output logic low voltage		V_{OL}(DC)	-	0.1 x VDDQ	V	I_{OL} = 0.1mA
Input leakage current		I_I	-4	4	uA	3
Output leakage current		I_{OZ}	-10	10	uA	

NOTE :
1) Under all conditions, VDDQ must be less than or equal to VDD.
2) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
3) Any input 0V ≤ VIN ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.

6.0 DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, Tc = -25 to 85°C)

Parameter	Symbol	Test Condition	DDR400	Unit	Note
Operating Current (One Bank Active)	IDD0	tRC=tRCmin; tCK=tCKmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	61	mA	1
Precharge Standby Current in power-down mode	IDD2P	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	2.0	mA	2
	IDD2PS	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	2.0		
Precharge Standby Current in non power-down mode	IDD2N	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	7	mA	1
	IDD2NS	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	5		
Active Standby Current in power-down mode	IDD3P	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	7	mA	1
	IDD3PS	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	6		
Active Standby Current in non power-down mode (One Bank Active)	IDD3N	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	13	mA	1
	IDD3NS	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	11		
Operating Current (Burst Mode)	IDD4R	one bank active; BL=4; CL=3; tCK = tCKmin; continuous read bursts; I_{OUT} =0 mA address inputs are SWITCHING; 50% data change each burst transfer	86	mA	1
	IDD4W	one bank active; BL = 4; tCK = tCKmin; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	66		
Refresh Current	IDD5	tRC ≥ tRFC; tCK = tCKmin; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	151	mA	1,3
Self Refresh Current	IDD6	CKE is LOW; t CK = t CKmin; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	**TCSR Range**	**Values**		2,7
			Full Array 85°C	3400	uA	
			45°C	800		
			1/2 Array 85°C	2800	uA	
			45°C	540		
			1/4 Array 85°C	2400	uA	
			45°C	400		

NOTE :

1) These specification values are under IDD2PS condition of the other unselected chip.

2) These specification values are under same condition of the both chips are selected at the same time.

3) IDD5 is measured in the below test condition.

Density	128Mb	256Mb	512Mb	1Gb	2Gb	Unit
t_{RFC}	80	80	110	140	140	ns

4) The IDD values need to be measured after devices are properly initialized following all sequences including MRS and EMRS in "Power Up Sequence" section in the specification.

5) Input slew rate is 1V/ns.

6) Definitions for IDD: LOW is defined as $V_{IN} \leq 0.1 * VDDQ$;
HIGH is defined as $V_{IN} \geq 0.9 * VDDQ$;
STABLE is defined as inputs stable at a HIGH or LOW level;
SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles;
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

7) IDD6 85°C is guaranteed, IDD6 45°C is typical value.

7.0 AC OPERATING CONDITIONS & TIMMING SPECIFICATION

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, all inputs	V_{IH} (AC)	0.8 x VDDQ	VDDQ + 0.3	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL} (AC)	-0.3	0.2 x VDDQ	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX} (AC)	0.4 x VDDQ	0.6 x VDDQ	V	2

NOTE :
1) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2) The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

8.0 AC TIMMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	DDR400		Unit	Note
			Min	Max		
Clock cycle time	CL=3	t_{CK}	5		ns	1,2
Row cycle time		t_{RC}	55		ns	
Row active time		t_{RAS}	40	70,000	ns	
RAS to CAS delay		t_{RCD}	15		ns	
Row precharge time		t_{RP}	15		ns	
Row active to Row active delay		t_{RRD}	10		ns	
Write recovery time		t_{WR}	12		ns	
Last data in to Active delay		t_{DAL}	-		-	3
Last data in to Read command		t_{CDLR}	2		tCK	
Col. address to Col. address delay		t_{CCD}	1		tCK	
Clock high level width		t_{CH}	0.45	0.55	tCK	
Clock low level width		t_{CL}	0.45	0.55	tCK	
DQ Output data access time from CK / $\overline{CK}$	CL=3	t_{AC}	2	5	ns	4
DQS Output data access time from CK / $\overline{CK}$	CL=3	t_{DQSCK}	2	5	ns	
Data strobe edge to output data edge		t_{DQSQ}		0.4	ns	
Read Preamble	CL=3	t_{RPRE}	0.9	1.1	tCK	
Read Postamble		t_{RPST}	0.4	0.6	tCK	
CK to valid DQS-in		t_{DQSS}	0.75	1.25	tCK	
DQS-in setup time		t_{WPRES}	0		ns	5
DQS-in hold time		t_{WPREH}	0.25		tCK	
DQS-in high level width		t_{DQSH}	0.4	0.6	tCK	
DQS-in low level width		t_{DQSL}	0.4	0.6	tCK	
DQS falling edge to CK setup time		t_{DSS}	0.2		tCK	
DQS falling edge hold time from CK		t_{DSH}	0.2		tCK	
DQS-in cycle time		t_{DSC}	0.9	1.1	tCK	
Address and Control Input setup time	fast slew rate	t_{IS}	0.9		ns	7
	slow slew rate		1.1			8
Address and Control Input hold time	fast slew rate	t_{IH}	0.9		ns	7
	slow slew rate		1.1			8
Address & Control input pulse width		t_{IPW}	2.2			
DQ & DM setup time to DQS	fast slew rate	t_{DS}	0.48		ns	6,7
	slow slew rate		0.58			6,8
DQ & DM hold time to DQS	fast slew rate	t_{DH}	0.48		ns	6,7
	slow slew rate		0.58			6,8
DQ & DM input pulse width		t_{DIPW}	1.2		ns	
DQ & DQS low-impedence time from CK / $\overline{CK}$		t_{LZ}	1.0		ns	
DQ & DQS high-impedence time from CK / $\overline{CK}$		t_{HZ}		5	ns	
DQS write postamble time		t_{WPST}	0.4	0.6	tCK	

Parameter	Symbol	DDR400		Unit	Note
		Min	Max		
DQS write preamble time	t_{WPRE}	0.25		tCK	
Refresh interval time	t_{REF}		64	ms	
Mode register set cycle time	t_{MRD}	2		tCK	
Power down exit time	t_{PDEX}	2		tCK	
CKE min. pulse width (high and low pulse width)	t_{CKE}	2		tCK	
Auto refresh cycle time	t_{RFC}	120		ns	9
Exit self refresh to active command	t_{XSR}	120		ns	
Data hold from DQS to earliest DQ edge	t_{QH}	t_{HP}min - t_{QHS}		ns	
Data hold skew factor	t_{QHS}		0.5	ns	
Clock half period	t_{HP}	t_{CL}min or t_{CH}min		ns	
Clock half period	t_{HP}	t_{CL}min or t_{CH}min		ns	

NOTE :

1) t_{CK} (max) value is measured at 100ns.

2) The only time that the clock Frequency is allowed to be changed is during clock stop, power-down, self-refresh modes.

3) In case of below 33MHz (t_{CK}=30ns) condition, SEC could support t_{DAL} (=2*tCK).
t_{DAL} =(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})

4) t_{AC} (min) value is measured at the high VDD (1.95V) and cold temperature (-25°C).
t_{AC} (max) value is measured at the low VDD (1.7V) and hot temperature (85°C).
t_{AC} is measured in the device with half driver strength and under the AC output load condition (Fig.6 in next Page).

5) The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.

6) I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Data Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

7) Input slew rate 1.0 V/ ns.

8) Input slew rate 0.5V/ns and < 1.0V/ns.

9) Maximum burst refresh cycle : 8

9.0 AC OPERATING TEST CONDITIONS (VDD = 1.7V to 1.95V, TC = -25°C to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	See Figure 6	

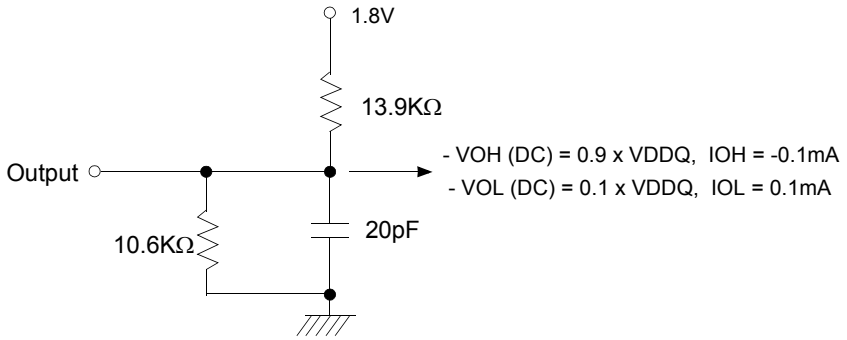


Figure 5. DC Output Load Circuit

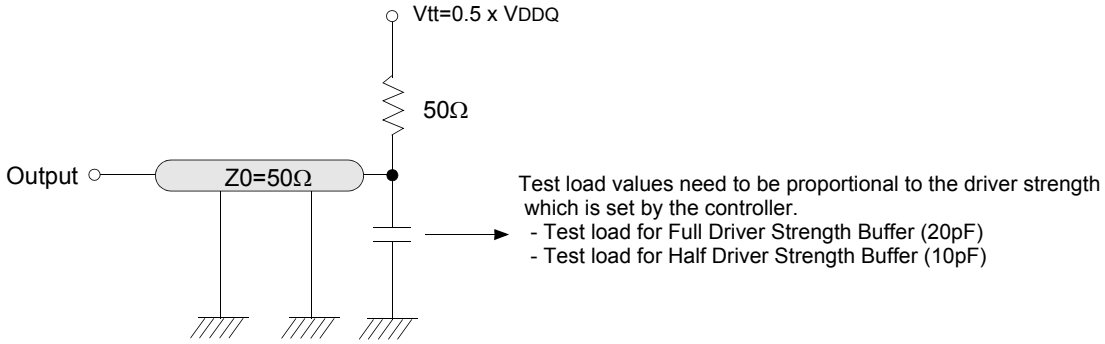


Figure 6. AC Output Load Circuit [1), 2)]

NOTE :

1) The circuit shown above represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half driver strength with a nominal 10pF load parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

2) Based on nominal impedance at 0.5 x VDDQ.
The impedence for Half(1/2) Driver Strength is designed 55ohm. And for other Driver Strength, it is designed proportionally.

10.0 INPUT/OUTPUT CAPACITANCE (VDD=1.8, VDDQ=1.8V, TC = 25°C, f=100MHz)

Parameter	Symbol	Min	Max	Unit
ADDs(A0~A13, BA0~BA1), $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CIN1	2.5	5.5	pF
$\overline{CS0}$, $\overline{CS1}$	CIN2	1.5	3.0	pF
CKE0, CKE1	CIN3	1.5	3.0	pF
CK, $\overline{CK}$	CIN4	2.5	6.5	pF
DMs	CIN5	3.5	8.5	pF
DQs, DQS	COUT	3.5	8.5	pF

11.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR ADDRESS & CONTROL PINS

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDD	3V-ns
Maximum undershoot area below VSS	3V-ns

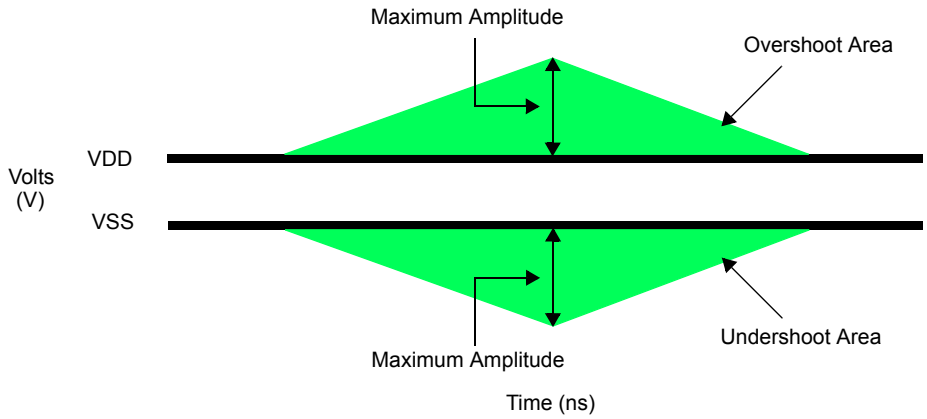


Figure 7. AC Overshoot and Undershoot Definition for Address and Control Pins

12.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR CK, DQ, DQS AND DM PINS

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.9V
Maximum peak Amplitude allowed for undershoot area	0.9V
Maximum overshoot area above VDDQ	3V-ns
Maximum undershoot area below VSSQ	3V-ns

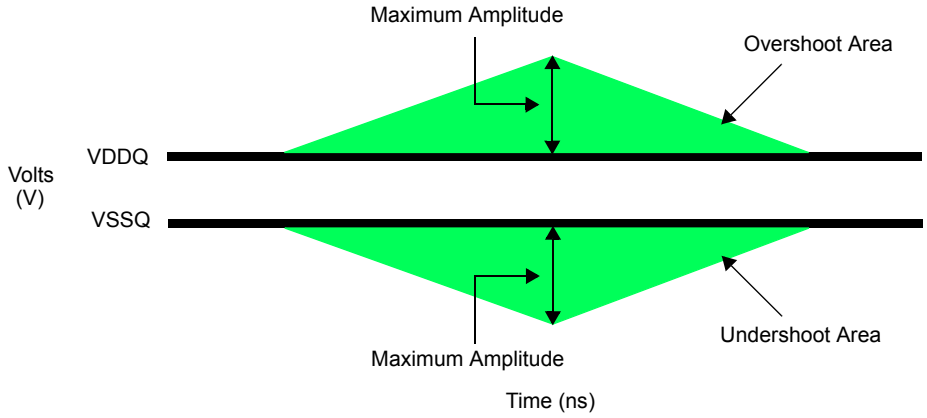


Figure 8. AC Overshoot and Undershoot Definition for CK, DQ, DQS and DM Pins

13.0 COMMAND TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A13~11, A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	X	X	X	X				
Precharge Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	H	H	H				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

NOTE :

1) OP Code : Operand Code. A0 ~ A13 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2) EMRS / MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3) Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4) BA0 ~ BA1 : Bank select addresses.
5) If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6) During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7) Burst stop command is valid at every burst length.
8) DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9) This combination is not defined for any function, which means "No Operation(NOP)" in Mobile DDR SDRAM.

14.0 FUNCTIONAL TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRECHARGE STANDBY	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [4]
	L	L	L	H	X	Refresh	AUTO-Refresh [5]
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set [5]
ACTIVE STANDBY	L	H	H	L	X	Burst Stop	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	L	H	H	L	X	Burst Stop	Terminate Burst
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge [3]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst, Precharge [10]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge [3]
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge [3]
	L	L	H	H	BA, RA	Active	Bank Active/ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	Terminate Burst With DM=High, Precharge [10]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE[6] (READA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	NOTE6
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	NOTE6
	L	L	H	L	BA, A10	PRE/PREA	NOTE6
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE with AUTO RECHARGE[7] (WRITEA)	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	NOTE7
	L	H	L	L	BA, CA, A10	WRITE/WRITEA	NOTE7
	L	L	H	H	BA, RA	Active	NOTE7
	L	L	H	L	BA, A10	PRE/PREA	NOTE7
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING (DURING t_{RP})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	NOP [4] (Idle after t_{RP})
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING (FROM ROW ACTIVE TO t_{RCD})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL [2]
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING (DURING t_{WR} OR t_{CDLR})	L	H	H	L	X	Burst Stop	ILLEGAL [2]
	L	H	L	H	BA, CA, A10	READ	ILLEGAL [2]
	L	H	L	L	BA, CA, A10	WRITE	WRITE
	L	L	H	H	BA, RA	Active	ILLEGAL [2]
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL [2]
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	L	H	H	L	X	Burst Stop	ILLEGAL
	L	H	L	X	BA, CA, A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING 8)	L	H	H	X	X	X	X	Exit Self-Refresh
	L	H	L	H	H	H	X	Exit Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE 9)	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down

(H=High Level, L=Low level, X=Don't Care)

NOTE :

1) All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2) ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
   (ILLEGAL = Device operation and/or data integrity are not guaranteed.)
3) Must satisfy bus contention, bus turn around and write recovery requirements.
4) NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5) ILLEGAL if any bank is not idle.
6) Refer to "Read with Auto Precharge Timing Diagram" for detailed information.
7) Refer to "Write with Auto Precharge Timing Diagram" for detailed information.
8) CKE Low to High transition will re-enable CK, $\overline{CK}$ and other inputs asynchronously.
   A minimum setup time must be satisfied before issuing any command other than EXIT.
9) Power-Down, Self-Refresh can be entered only from All Bank Idle state.

Mobile DDR SDRAM Device Operation & Timing Diagram

Device Operations

1. PRECHARGE

The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses(BA0, BA1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied until the precharge command can be issued. After tRP from the precharge, an active command to the same bank can be initiated.

[Table 1] Bank selection for precharge by Bank address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

2. NO OPERATION(NOP) & DEVICE DESELECT

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode, Mobile DDR SDRAM should ignore all the control inputs. The Mobile DDR SDRAM is put in NOP mode when $\overline{CS}$ is activated and $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are deactivated. Both Device Deselect and NOP command can not affect operation already in progress. So even if the device is deselected or NOP command is issued under operation, the operation will be completed.

3. ROW ACTIVE

The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock (CK). The Mobile DDR SDRAM has four independent banks, so two Bank Select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time, tRCD(min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time, tRRD(min).

Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

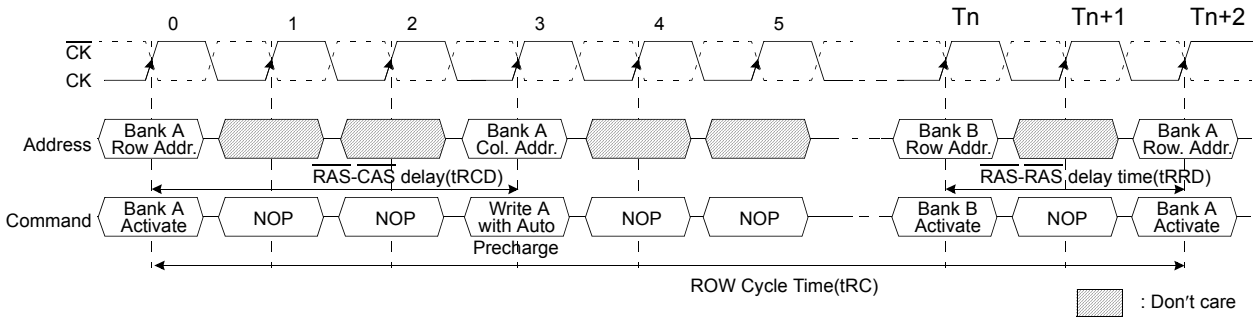


Figure 1. Bank Activation Command Cycle timing <tRCD=3CLK, tRRD=2CLK>

4. READ BANK

This command is used after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the CAS latency time will be determined by the values programmed during the MRS cycle.

5. WRITE BANK

This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{RAS}$, $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling(rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS cycle.

6. BURST READ OPERATION

Burst Read operation in Mobile DDR SDRAM is in the same manner as the Mobile SDR SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock(CK) after tRCD from the bank activation. The address inputs determine the starting address for the Burst. The Mode Register sets type of burst (Sequential or interleave) and burst length(2, 4, 8, 16). The first output data is available with a CAS Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe (DQS) adopted by Mobile DDR SDRAM until the burst length is completed.

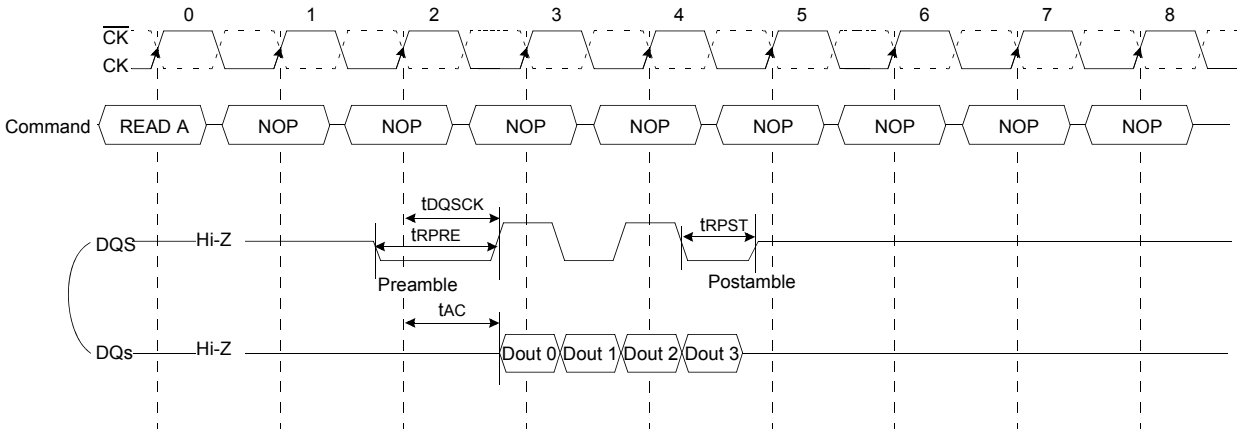


Figure 2. Burst read operation timing

NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency= 3.

7. BURST WRITE OPERATION

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock (CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for burst write cycle. The first data of a burst write cycle must be applied on the DQ pins tDS (Data-in setup time) prior to data strobe edge enabled after tDQSS from the rising edge of the clock (CK) that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

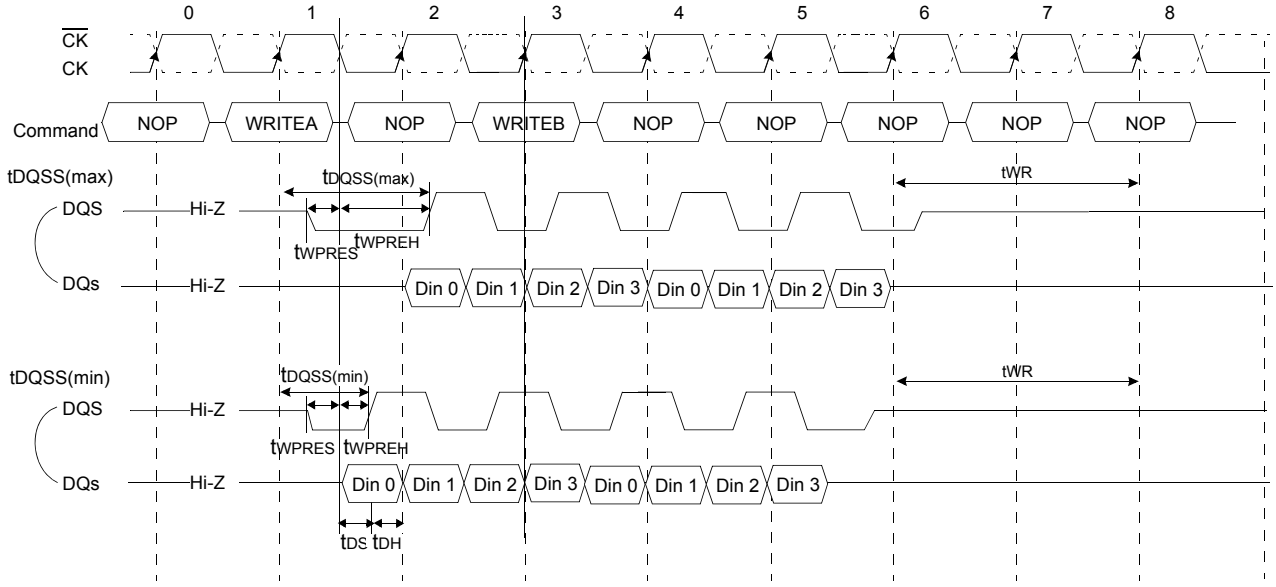


Figure 3. Burst write operation timing

NOTE :
1) Burst Length=4.
2) The specific requirement is that DQS be valid (High or Low) on or before this CK edge.
The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus.

8. READ INTERRUPTED BY A READ

A Burst Read can be interrupted by new Read command of any bank before completion of the burst. When the previous burst is interrupted, the new address with the full burst length override the remaining address. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears. Read to Read interval is minimum 1 Clock.

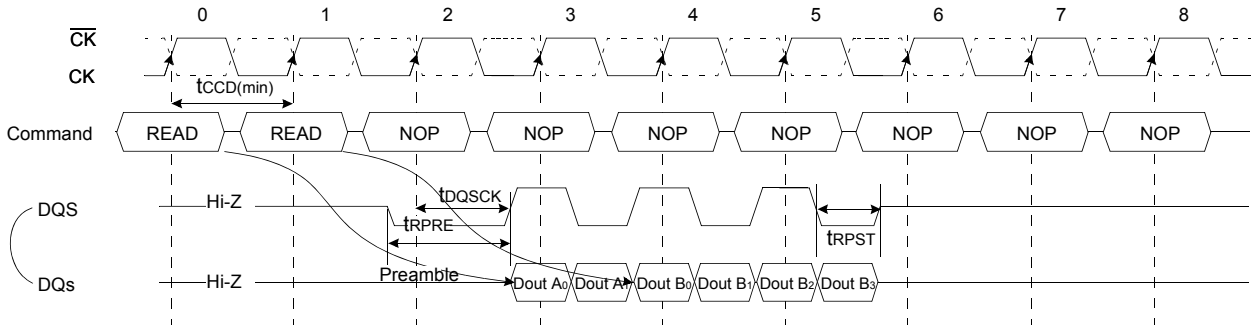


Figure 4. Read interrupted by a read timing

NOTE :
1) Burst Length=4, CAS Latency=3

9. READ INTERRUPTED BY A WRITE & BURST STOP

To interrupt a burst read with a write command, Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQs (Output drivers) in a high impedance state.

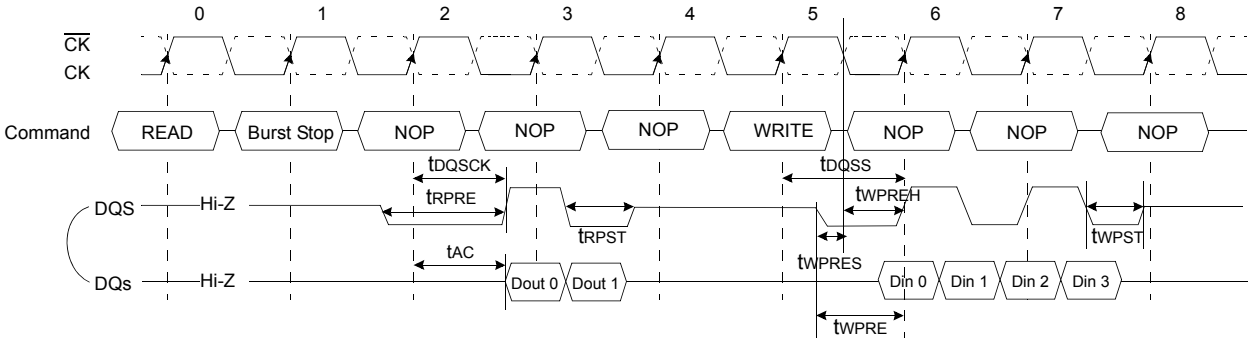


Figure 5. Read interrupted by a write and burst stop timing

NOTE :
1) Burst Length=4, CAS Latency=3 .

The following functionality establishes how a Write command may interrupt a burst Read.

1. For Write commands interrupting a burst Read, a Burst Terminate command is required to stop the burst read and tri-state the DQ bus prior to valid input write data. Burst stop command must be applied at least 2 clock cycles for CL=2 and at least 3 clock cycles for CL=3 before the Write command.

2. It is illegal for a Write command to interrupt a Read with autoprecharge command.

10. READ INTERRUPTED BY A PRECHARGE

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock is required for the read to precharge intervals. The latency from a precharge command to invalid output is equivalent to the CAS latency.

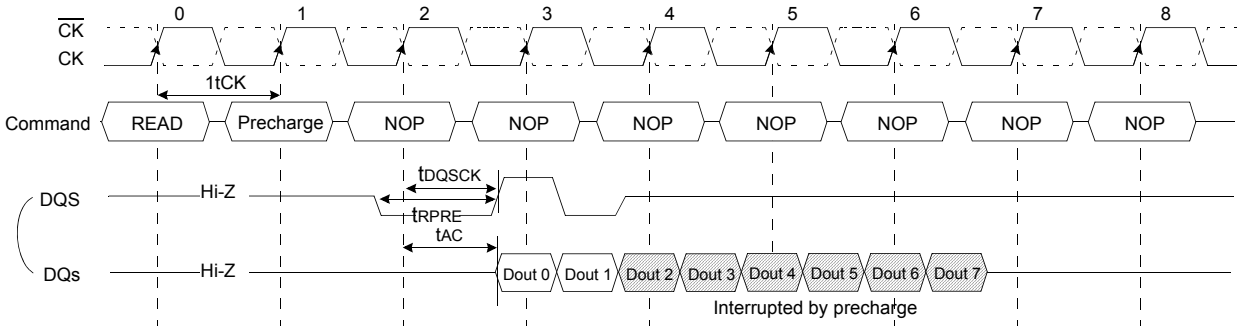


Figure 6. Read interrupted by a precharge timing

NOTE :
1) Burst Length=8, $\overline{\text{CAS}}$ Latency=3 .

When a burst Read command is issued to a Mobile DDR SDRAM, a Precharge command may be issued to the same bank before the Read burst is completed. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a burst Read, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP (Row Precharge time).

2. When a Precharge command interrupts a burst Read operation, the Precharge command given on a rising clock edge terminates the burst with the last valid data word presented on DQ pins at CL-1(CL=CAS Latency) clock cycles after the command has been issued. Once the last data word has been output, the output buffers are tri-stated. A new Bank Activate command may be issued to the same bank after tRP.

3. For a Read with Autoprecharge command, a new Bank Activate command may be issued to the same bank after tRP from rising clock that comes CL(CL=CAS Latency) clock cycles before the end of the Read burst. During Read with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command would initiate a precharge operation without interrupting the Read burst as described in 1 above.

4. For all cases above, tRP is an analog delay that needs to be converted into clock cycles. The number of clock cycles between a Precharge command and a new Bank Activate command to the same bank equals tRP/tCK (where tCK is the clock cycle time) with the result rounded up to the nearest integer number of clock cycles. (Note that rounding to X.5 is not possible since the Precharge and Bank Activate commands can only be given on a rising clock edge).In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Read with autoprecharge commands where tRAS(min) must still be satisfied such that a Read with autoprecharge command has the same timing as a Read command followed by the earliest possible Precharge command which does not interrupt the burst.

11. WRITE INTERRUPTED BY A WRITE

A Burst Write can be interrupted by a new Write command before completion of the burst, where the interval between the successive Write commands must be at least one clock cycle(tCCD(min)). When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

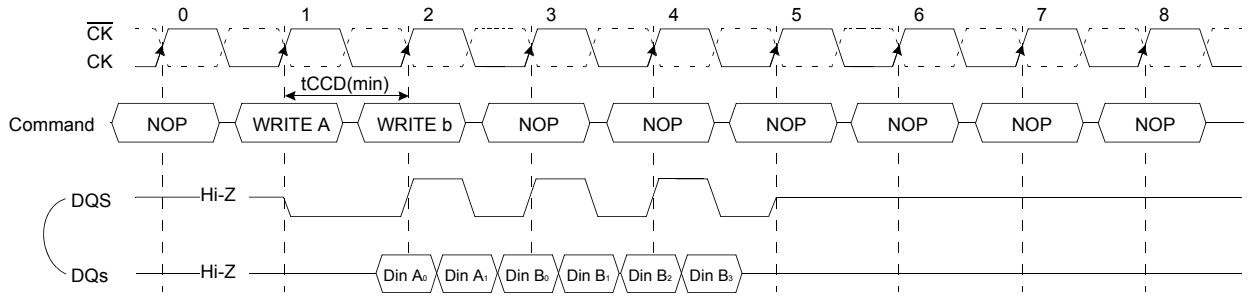


Figure 7. Write interrupted by a write timing

NOTE :
1) Burst Length=4.

12. WRITE INTERRUPTED BY A PRECHARGE & DM

A burst write operation can be interrupted by a precharge of the same bank before completion of the burst. Random column access is allowed. A write recovery time(tWR) is required from the last data to precharge command. When precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

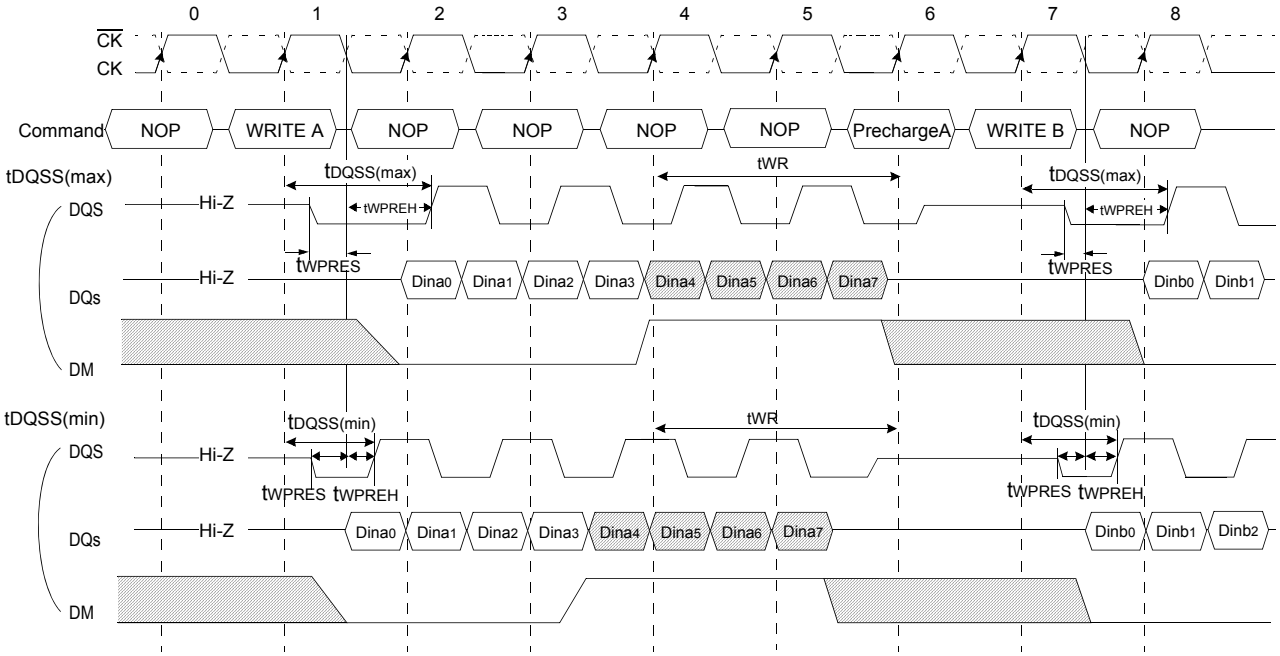


Figure 8. Write interrupted by a precharge and DM timing

NOTE :
1) Burst Length=8.

Precharge timing for Write operations in Mobile DDR SDRAM requires enough time to allow 'write recovery' which is the time required by a Mobile DDR SDRAM core to properly store a full '0' or '1' level before a Precharge operation. For Mobile DDR SDRAM, a timing parameter, tWR, is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The precharge timing for writes is a complex definition since the write data is sampled by the data strobe and the address is sampled by the input clock. Inside the Mobile DDR SDRAM, the data path is eventually synchronized with the address path by switching clock domains from the data strobe clock domain to the input clock domain. This makes the definition of when a precharge operation can be initiated after a write very complex since the write recovery parameter must make reference to only the clock domain that affects internal write operation, i.e., the input clock domain.

tWR starts on the rising clock edge after the last possible DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the precharge command.

1. For the earliest possible Precharge command following a burst Write without interrupting the burst, the minimum time for write recovery is defined by tWR.
2. When a precharge command interrupts a Write burst operation, the data mask pin, DM, is used to mask input data during the time between the last valid write data and the rising clock edge on which the Precharge command is given. During this time, the DQS input is still required to strobe in the state of DM. The minimum time for write recovery is defined by tWR.
3. For a Write with autoprecharge command, a new Bank Activate command may be issued to the same bank after tWR+tRP where tWR+tRP starts on the falling DQS edge that strobed in the last valid data and ends on the rising clock edge that strobes in the Bank Activate command. During write with autoprecharge, the initiation of the internal precharge occurs at the same time as the earliest possible external Precharge command without interrupting the Write burst as described in 1 above.
4. In all cases, a Precharge operation cannot be initiated unless tRAS(min) [minimum Bank Activate to Precharge time] has been satisfied. This includes Write with autoprecharge commands where tRAS(min) must still be satisfied such that a Write with autoprecharge command has the same timing as a Write command followed by the earliest possible Precharge command which does not interrupt the burst.

13. WRITE INTERRUPTED BY A READ & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention Mobile DDR SDRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

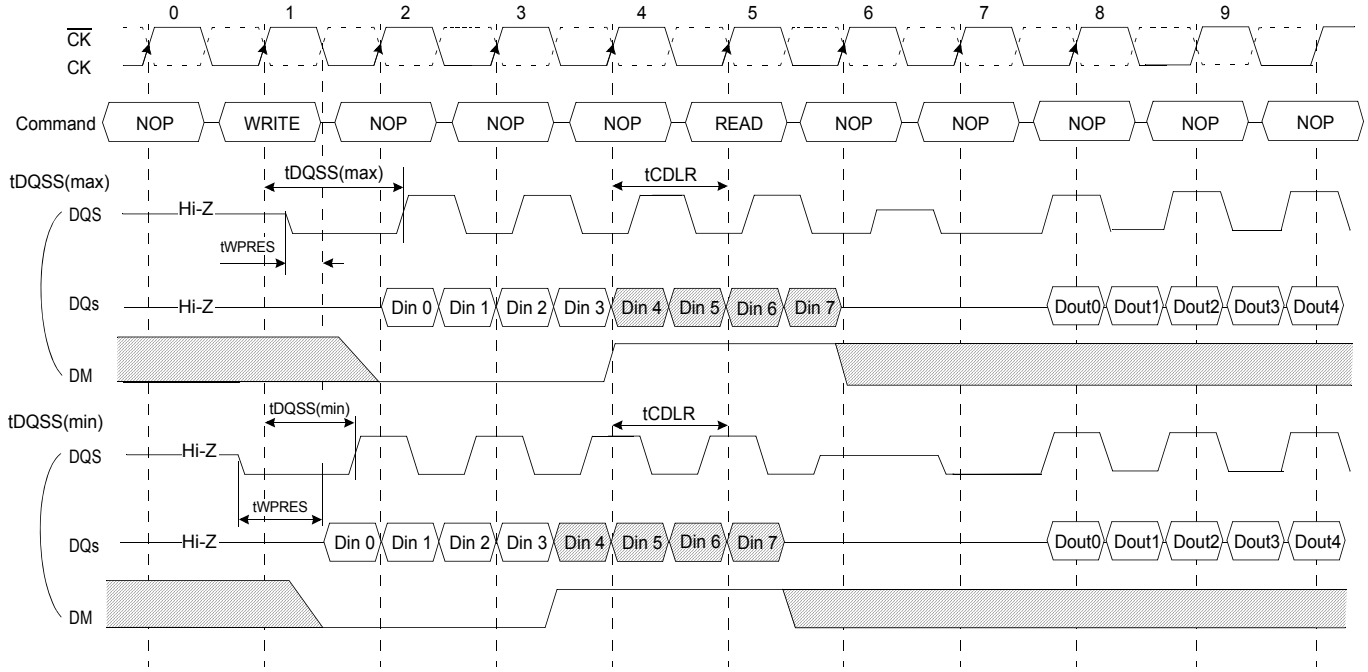


Figure 9. Write interrupted by a Read and DM timing

NOTE :
1) Burst Length=8, $\overline{CAS}$ Latency=3 .

The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a burst Write, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For Read commands interrupting a burst Write, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the Mobile DDR SDRAM drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the Mobile DDR SDRAM.
5. Refer to Burst write operation.

14. BURST STOP

The burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock(CK). The burst stop command has the fewest restrictions making it the easiest method to use when terminating a burst read operation before it has been completed. When the burst stop command is issued during a burst read cycle, the pair of data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the CAS latency set in the mode register. However, the burst stop command is not supported during a burst write operation.

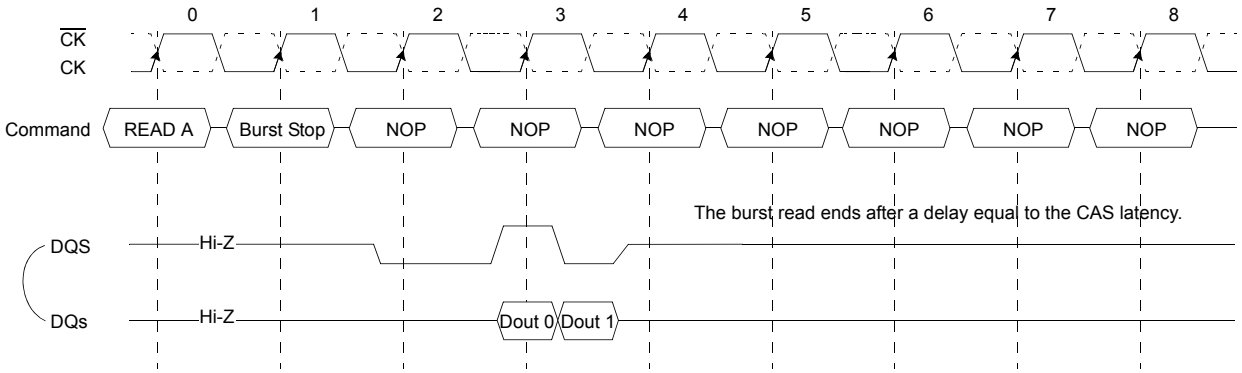


Figure 10. Burst stop timing

NOTE :
1) Burst Length=4, $\overline{CAS}$ Latency= 3.

The Burst Stop command is a mandatory feature for Mobile DDR SDRAM. The following functionality is required:

1. The Burst Stop command may only be issued on the rising edge of the input clock, CK.
2. Burst Stop is only a valid command during Read bursts.
3. Burst Stop during a Write burst is undefined and shall not be used.
4. Burst Stop applies to all burst lengths.
5. Burst Stop is an undefined command during Read with autoprecharge and shall not be used.
6. When terminating a burst Read command, the BST command must be issued L_{BST} (“BST Latency”) clock cycles before the clock edge at which the output buffers are tristated, where L_{BST} equals the CAS latency for read operations.
7. When the burst terminates, the DQ and DQS pins are tristated.

The Burst Stop command is not byte controllable and applies to all bits in the DQ data word and the(all) DQS pin(s).

15. DM MASKING

The Mobile DDR SDRAM has a data mask function that can be used in conjunction with data write cycle, not read cycle. When the data mask is activated(DM high) during write operation, Mobile DDR SDRAM does not accept the corresponding data.(DM to data-mask latency is zero). DM must be issued at the rising or falling edge of data strobe.

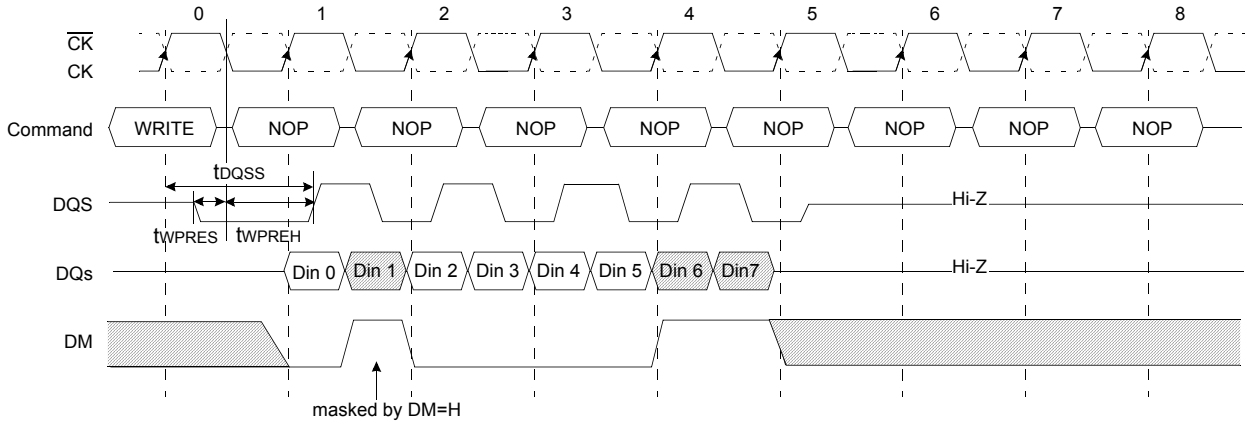


Figure 11. DM masking timing

NOTE :
1) Burst Length=8.

16. READ WITH AUTO PRECHARGE

If A10/AP is high when read command is issued, the read with auto-precharge function is performed. If a read with auto-precharge command is issued, the Mobile DDR SDRAM automatically enters the precharge operation BL/2 clock later from a read with auto-precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the precharge time(tRP) has been satisfied.

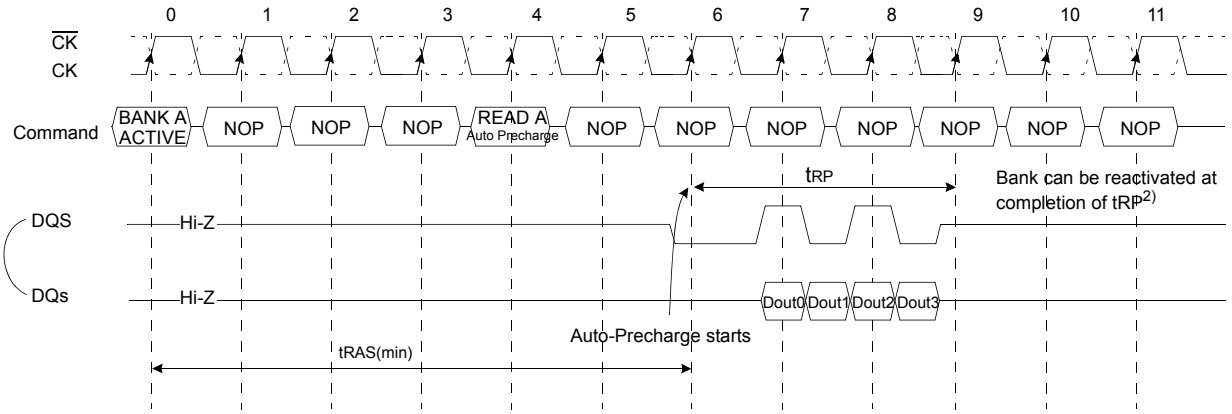


Figure 12. Read with auto precharge timing

NOTE :
1) Burst Length=4, CAS Latency= 3.
2) The row active command of the precharge bank can be issued after tRP from this point.

Asserted command	For same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ +No AP1)	READ+No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

NOTE :
1) AP = Auto Precharge.

17. WRITE WITH AUTO PRECHARGE

If A10/AP is high when write command is issued, the write with auto-precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

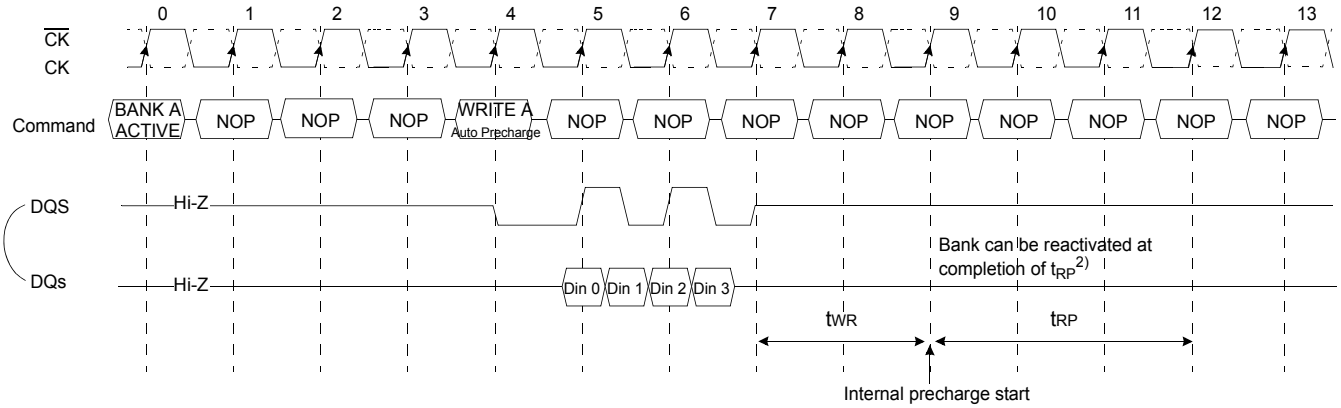


Figure 13. Write with auto precharge timing

NOTE :
1) Burst Length=4.
2) The row active command of the precharge bank can be issued after tRP from this point.

Asserted command	For same Bank						For Different Bank				
	5	6	7	8	9	10	5	6	7	8	9
WRITE	WRITE+ No AP1)	WRITE+ No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ+ NO AP+DM2)	READ+ NO AP+DM	READ+ NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ+AP	Illegal	READ + AP+DM	READ + AP+DM	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

NOTE :
1) AP = Auto Precharge.
2) DM : Refer to "27. *Write Interrupted by Precharge & DM* ".

18. AUTO REFRESH & SELF REFRESH

18.1. Auto Refresh

An auto refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock(CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. Once this cycle has been started, no control of the external address pins are required because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tRFC(min).

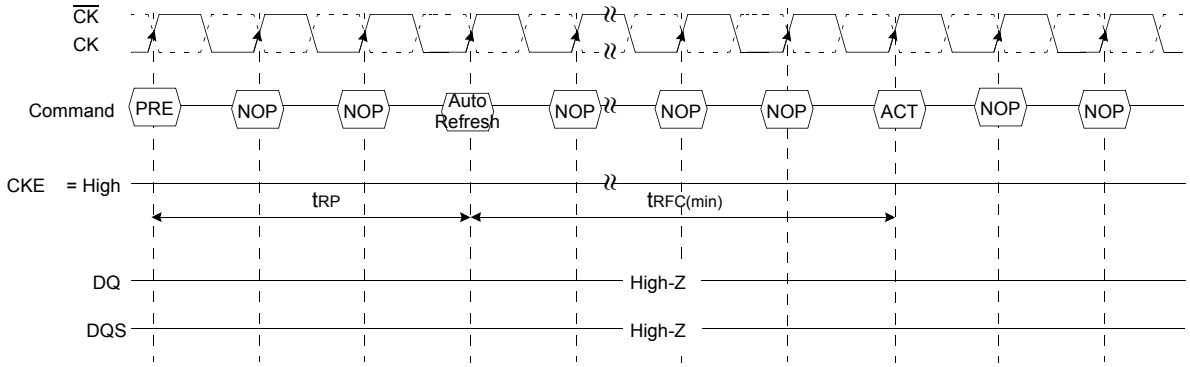


Figure 14. Auto refresh timing

NOTE :
1) tRP=3CLK
2) Device must be in the all banks idle state prior to entering Auto refresh mode.

18.2. Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 1 clock cycle from the self refresh command, all of the external control signals including system clock(CK, $\overline{CK}$) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. Before returning CKE high to exit the Self Refresh mode, apply stable clock input signal with Deselect or NOP command asserted.

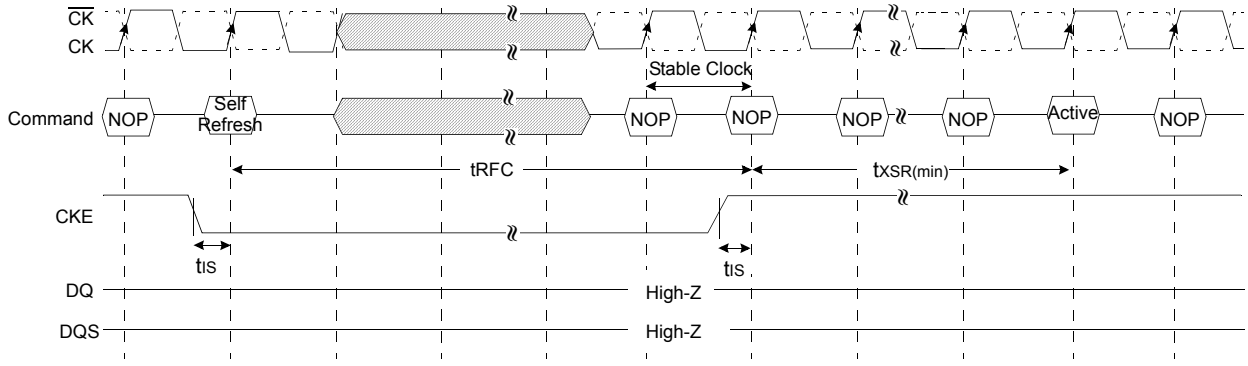


Figure 15. Self refresh timing

NOTE :
1) Device must be in the all banks idle state prior to entering Self Refresh mode.
2) The minimum time that the device must remain in Self Refresh mode is tRFC.

19. POWER DOWN

The device enters power down mode when CKE Low, and it exits when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set in high for at least tPDEX prior to Row active command. Refresh operations cannot be performed during power down mode, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.

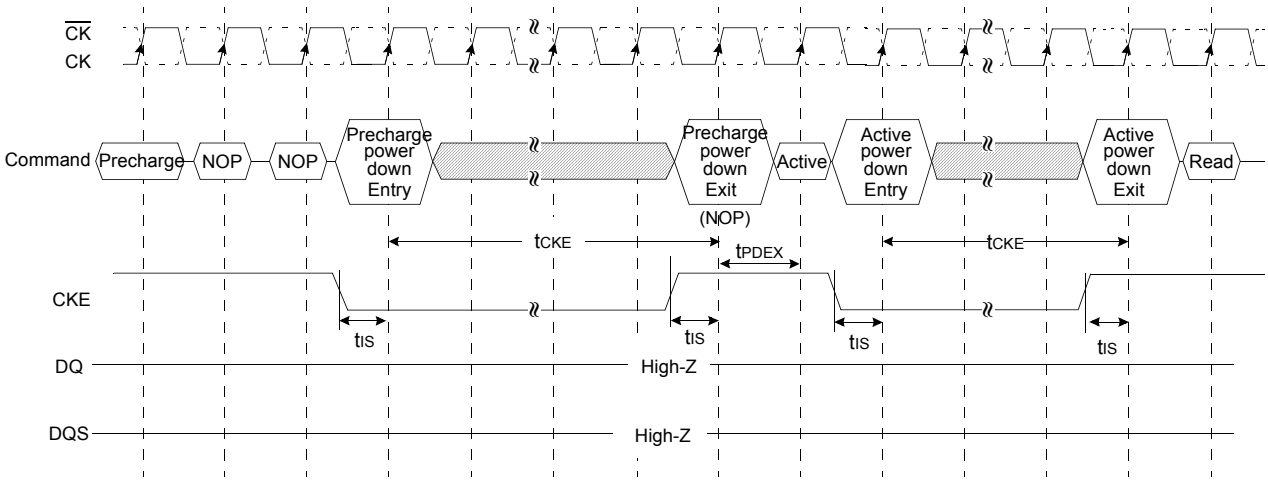


Figure 16. Power down entry and exit timing

NOTE :
1) Device must be in the all banks idle state prior to entering Power Down mode.
2) The minimum power down duration is specified by tCKE.

20. CLOCK STOP

Stopping a clock during idle periods is an effective method of reducing power consumption.

The LPDDR SDRAM supports clock stop under the following conditions :
- the last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- the related timing conditions (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held High

When all conditions have been met, the device is either in "idle state"or "row active state" and clock stop mode may be entered with CK held Low and $\overline{CK}$ held Hight.
Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command any be applied. Additional clock pulses might be required depending on the system characteristics.

Figure shows clock stop mode entry and exit.
- Initially the device is in clock stop mode
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command is completed.
- Tn is the last clock pulse required by the access command latched with T1
- The clock can be stopped after Tn.

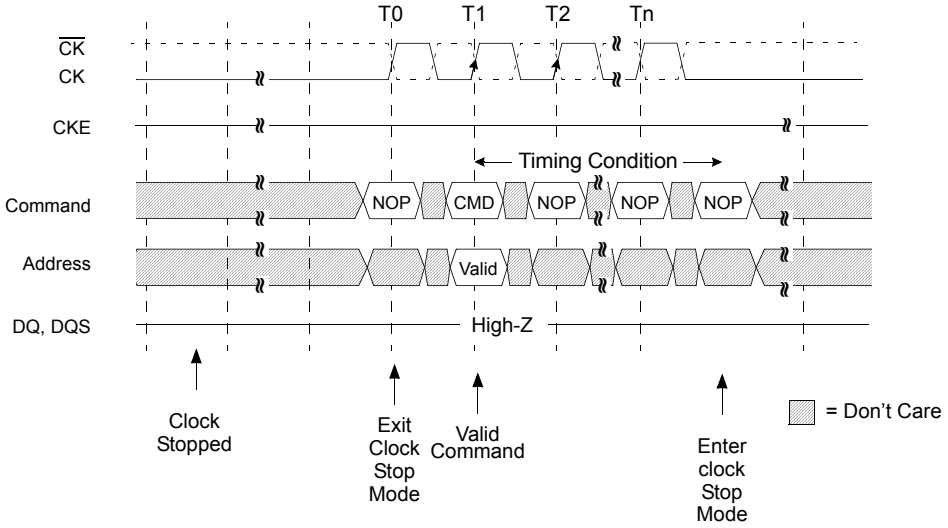


Figure 17. Clock Stop Mode Entry and Exit

Timing Diagram

1. POWER UP SEQUENCE FOR MOBILE DDR SDRAM

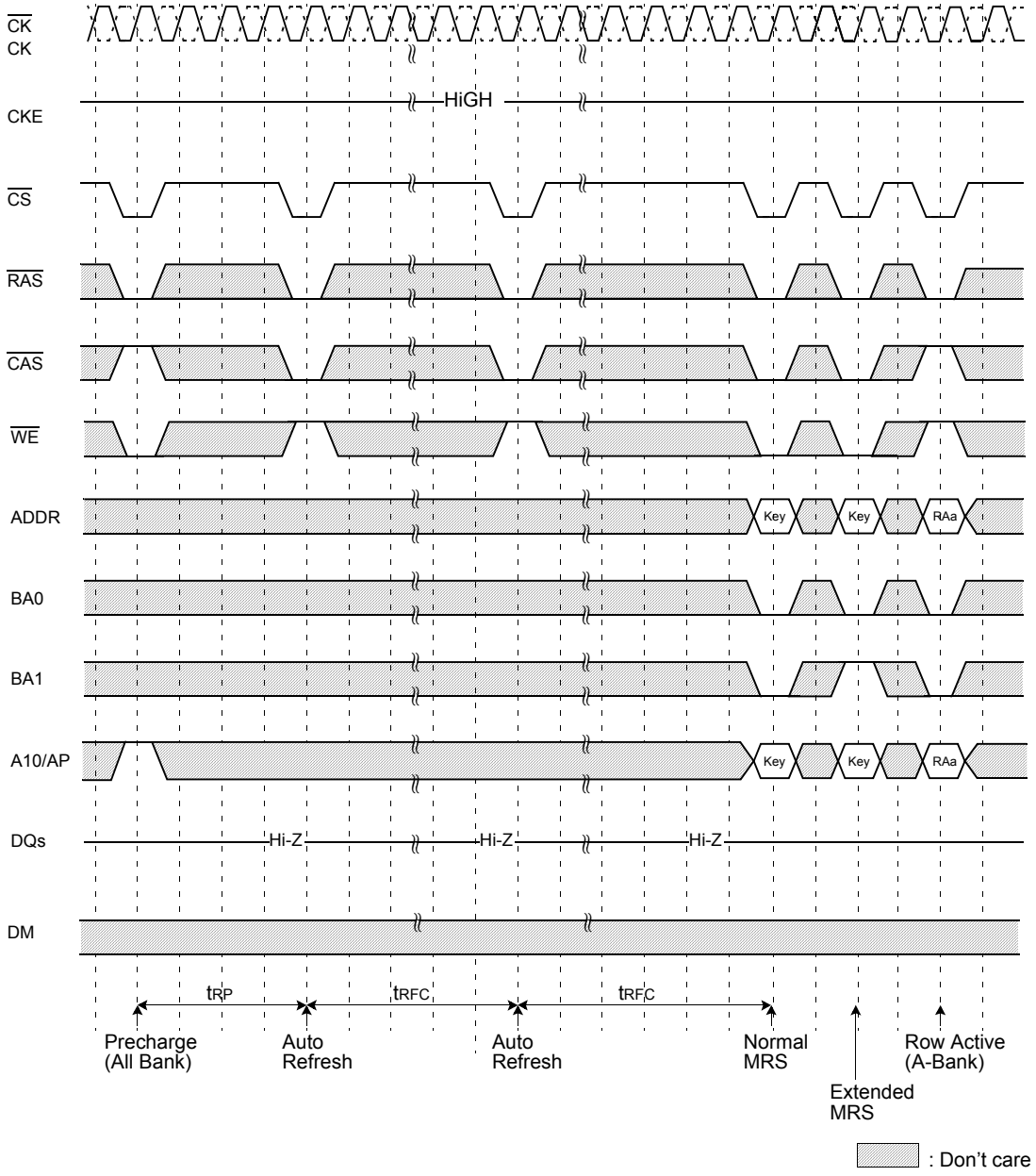


Figure 18. Power Up Sequence for Mobile DDR SDRAM

NOTE :
1) Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
 - Apply VDD before or at the same time as VDDQ.
2) Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3) Issue precharge commands for all banks of the devices.
4) Issue 2 or more auto-refresh commands.
5) Issue a mode register set command to initialize the mode register.
6) Issue a extended mode register set command for the desired operating modes after normal MRS.

The Mode Register and Extended Mode Register do not have default values.
If they are not programmed during the initialization sequence, it may lead to unspecified operation.
All banks have to be in idle state prior to adjusting MRS and EMRS set.

2. BASIC TIMING

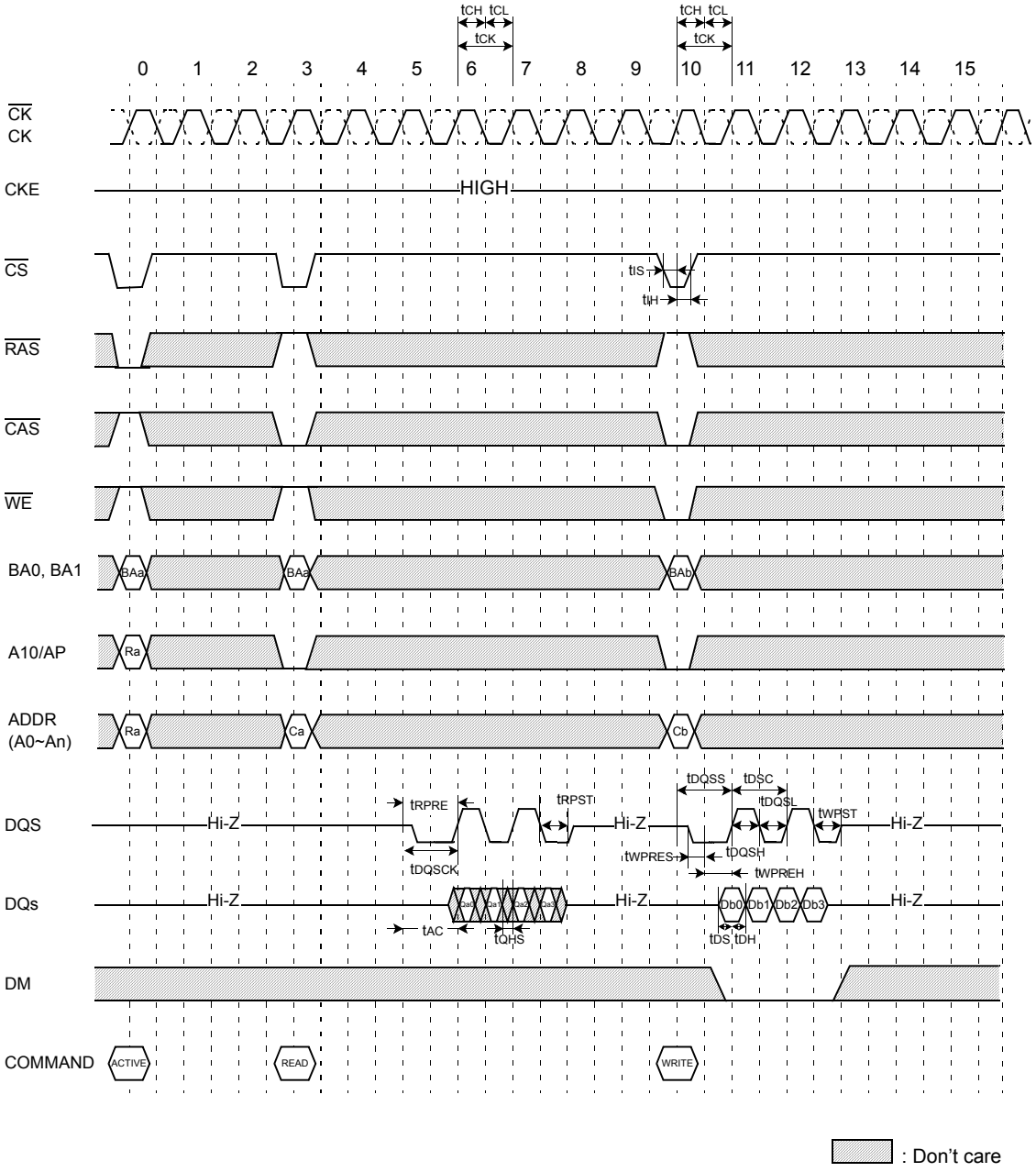


Figure 19. Basic Timing (Setup, Hold and Access Time @BL=4, CL=3)

3. MULTI BANK INTERLEAVING READ

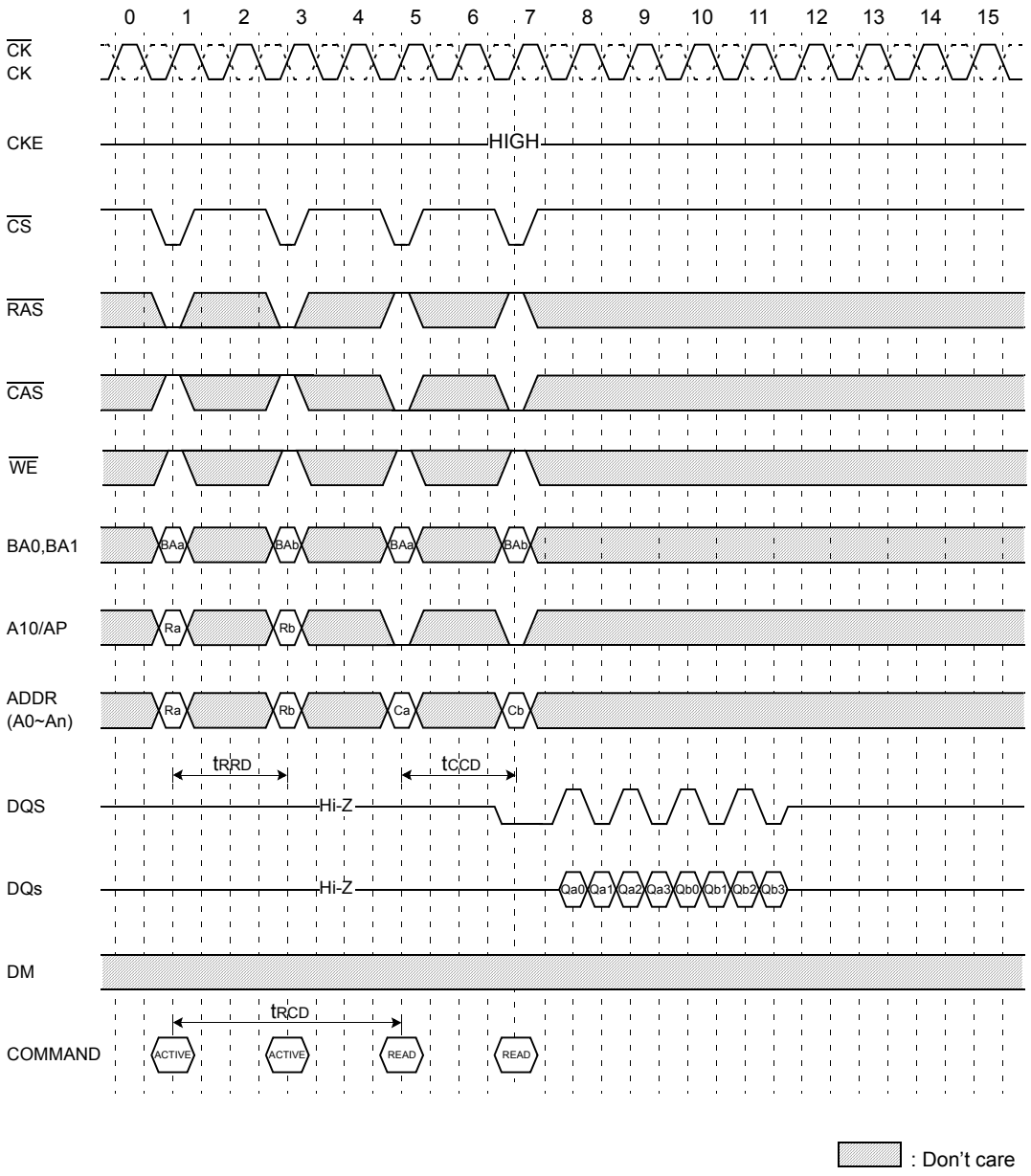


Figure 20. Multi Bank Interleaving READ (@BL=4, CL=3)

4. MULTI BANK INTERLEAVING WRITE

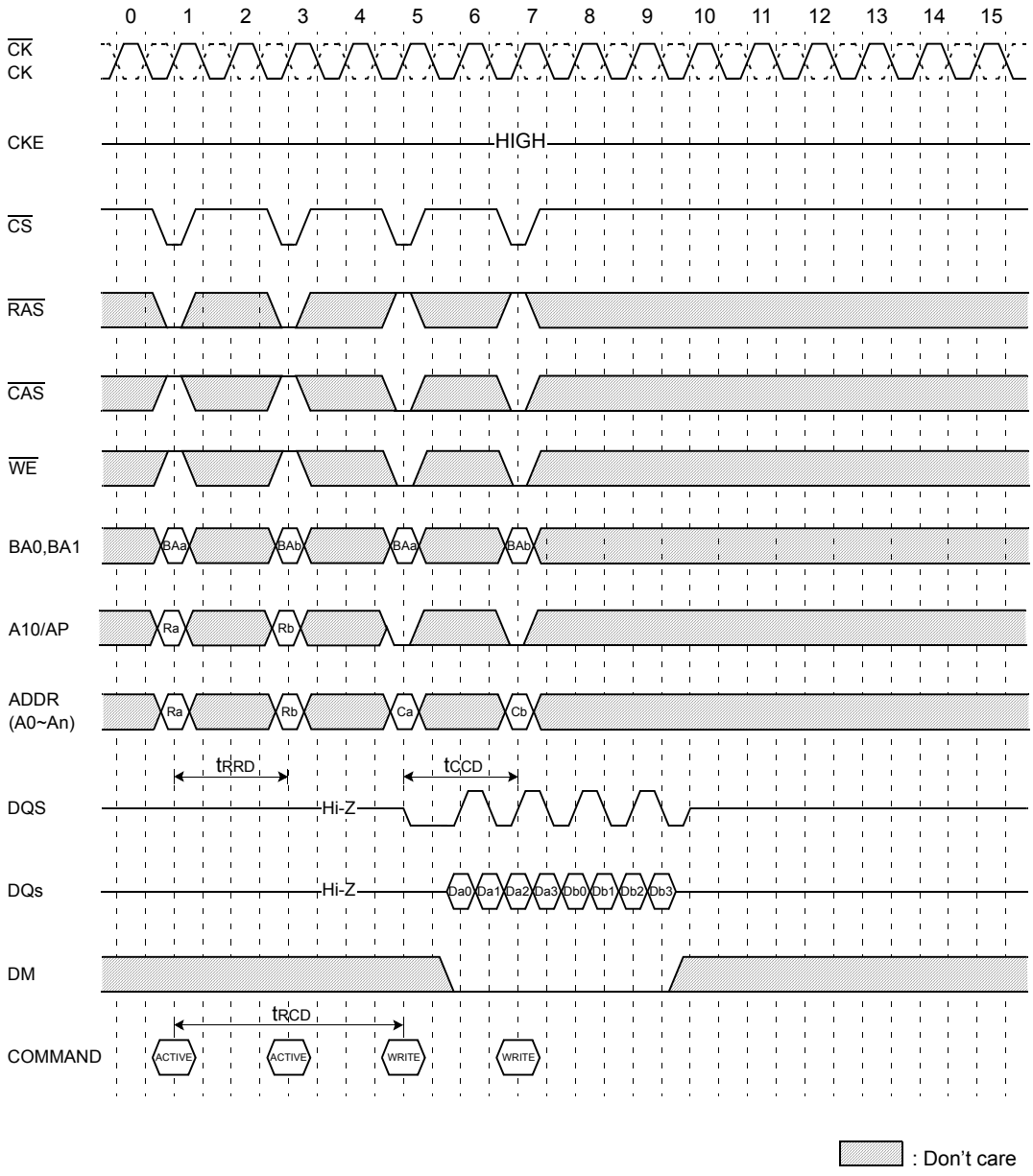


Figure 21. Multi Bank Interleaving WRITE (@BL=4)

5. READ WITH AUTO PRECHARGE

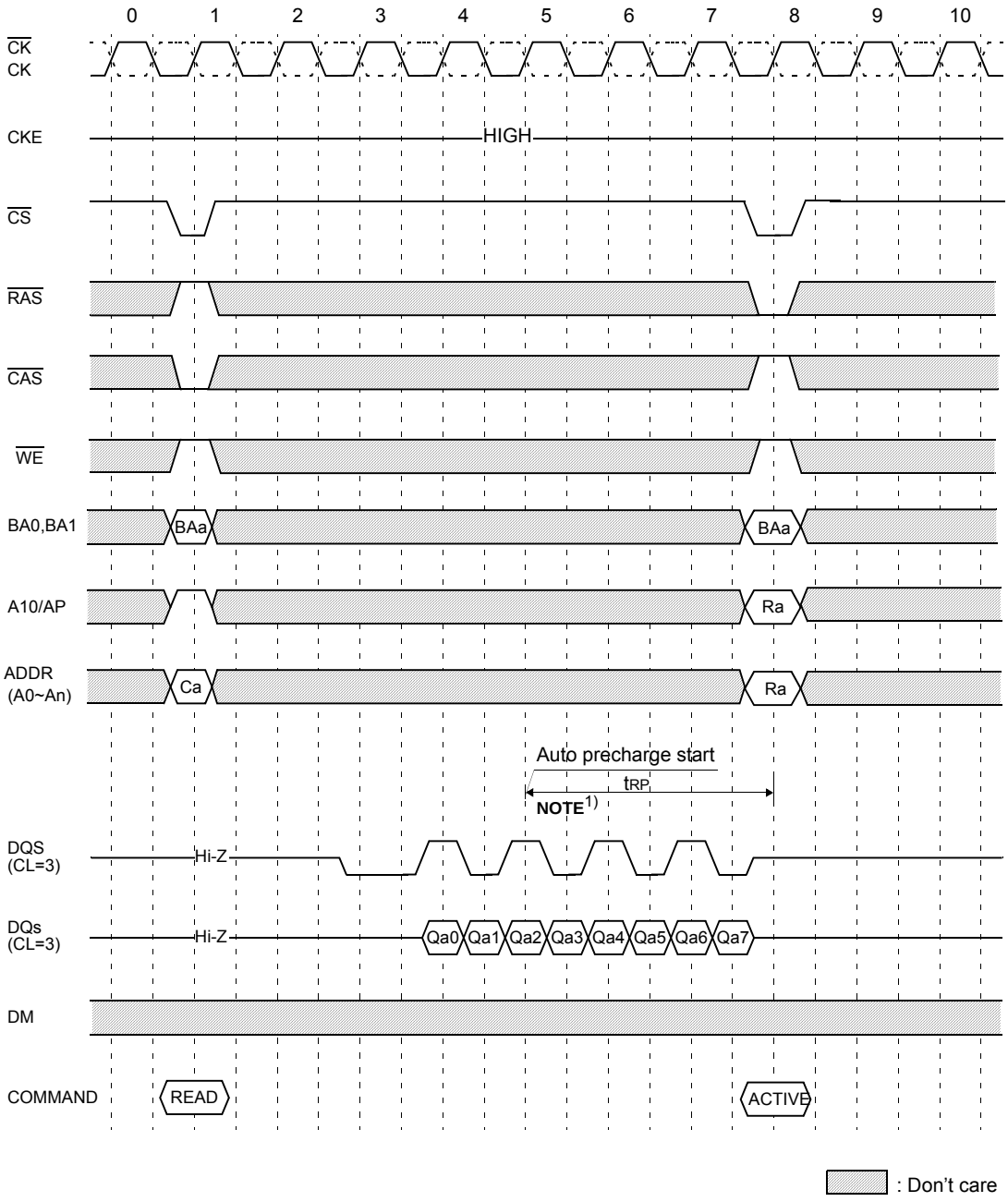


Figure 22. Read with Auto Precharge (@BL=8)

NOTE :
1) The row active command of the precharge bank can be issued after tRP from this point.

6. WRITE WITH AUTO PRECHARGE

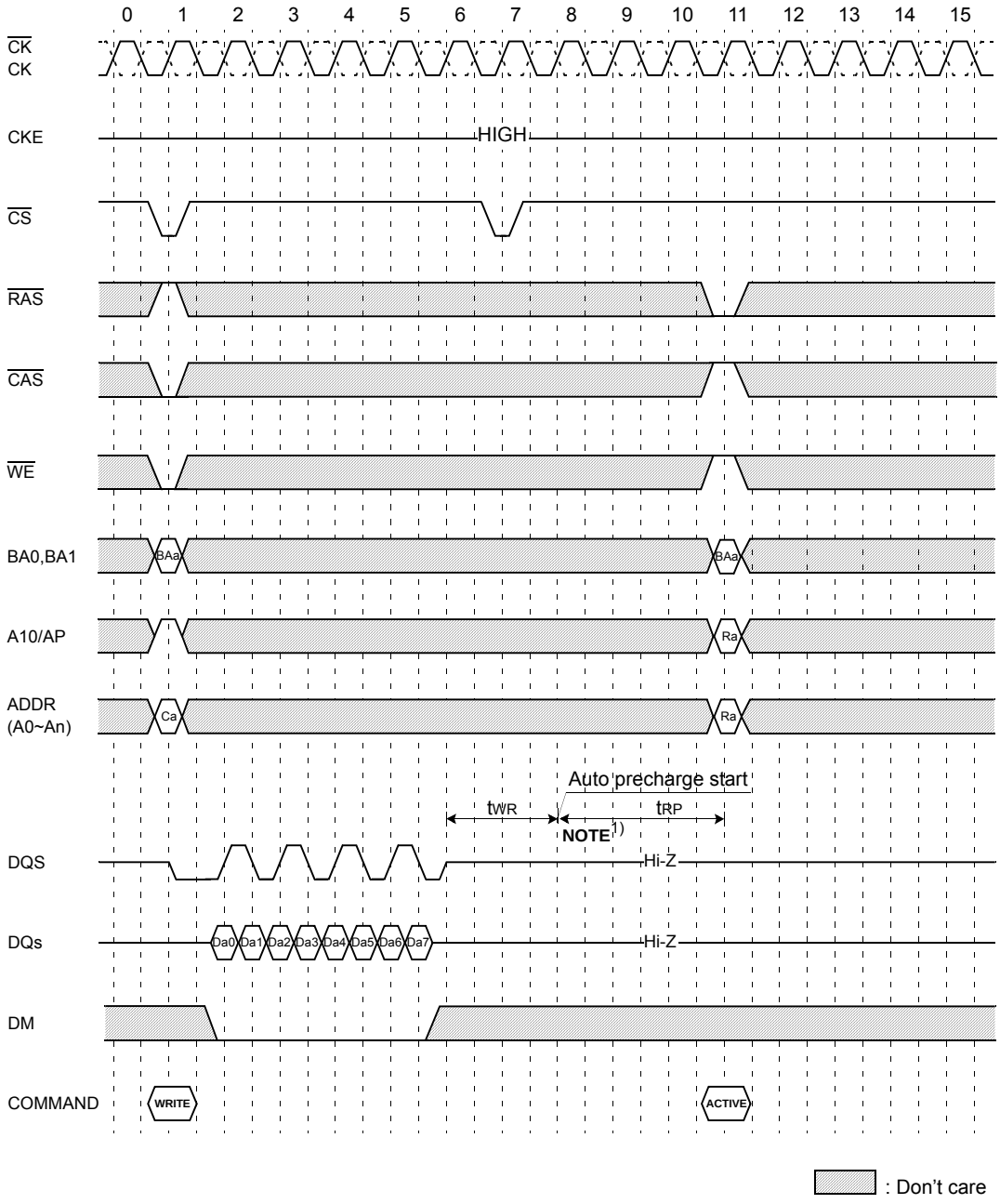


Figure 23. Write with Auto Precharge (@BL=8)

NOTE :
1) The row active command of the precharge bank can be issued after tRP from this point

7. WRITE FOLLOWED BY PRECHARGE

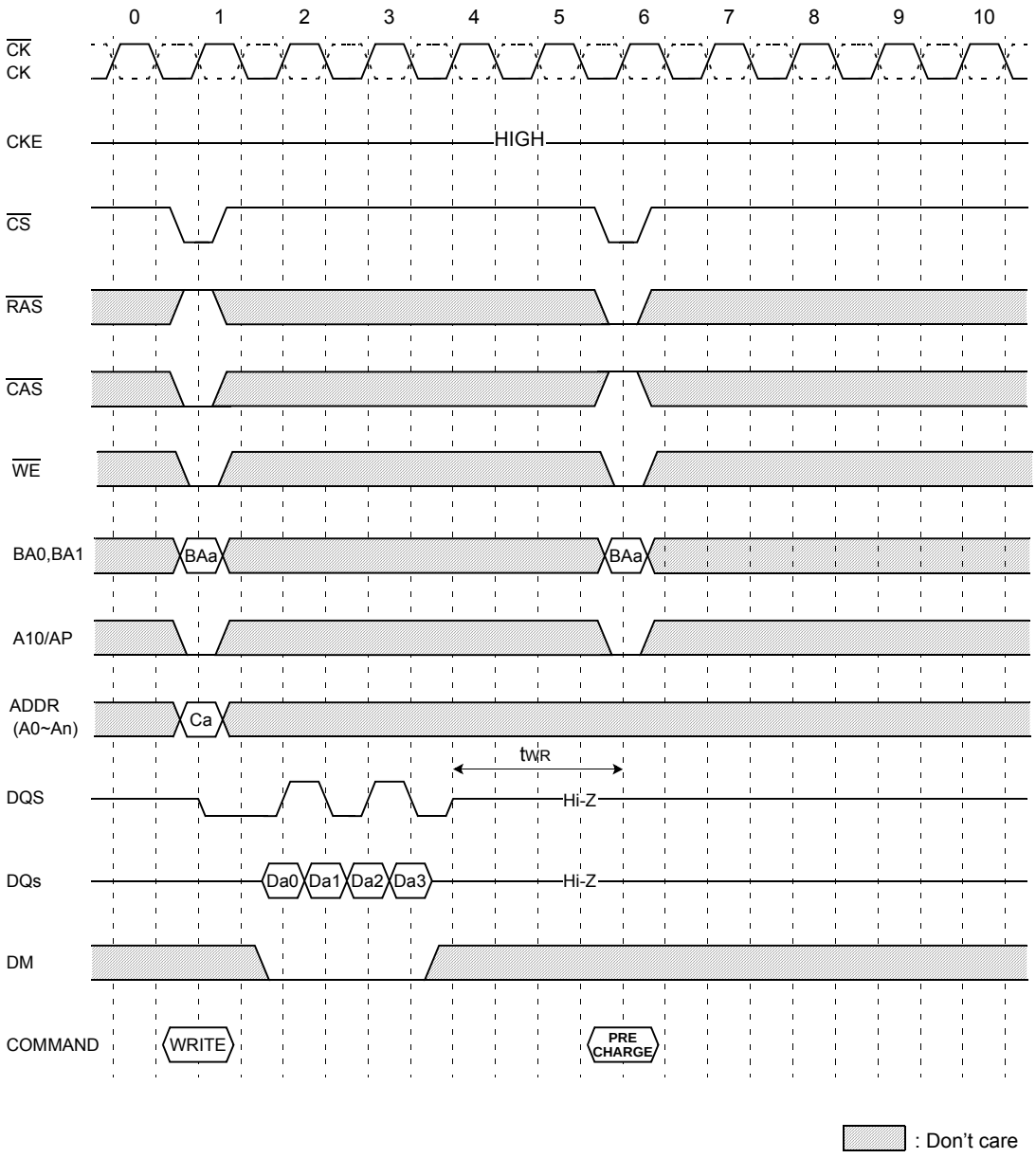


Figure 24. Write followed by Precharge (@BL=4)

8. WRITE INTERRUPTED BY PRECHARGE & DM

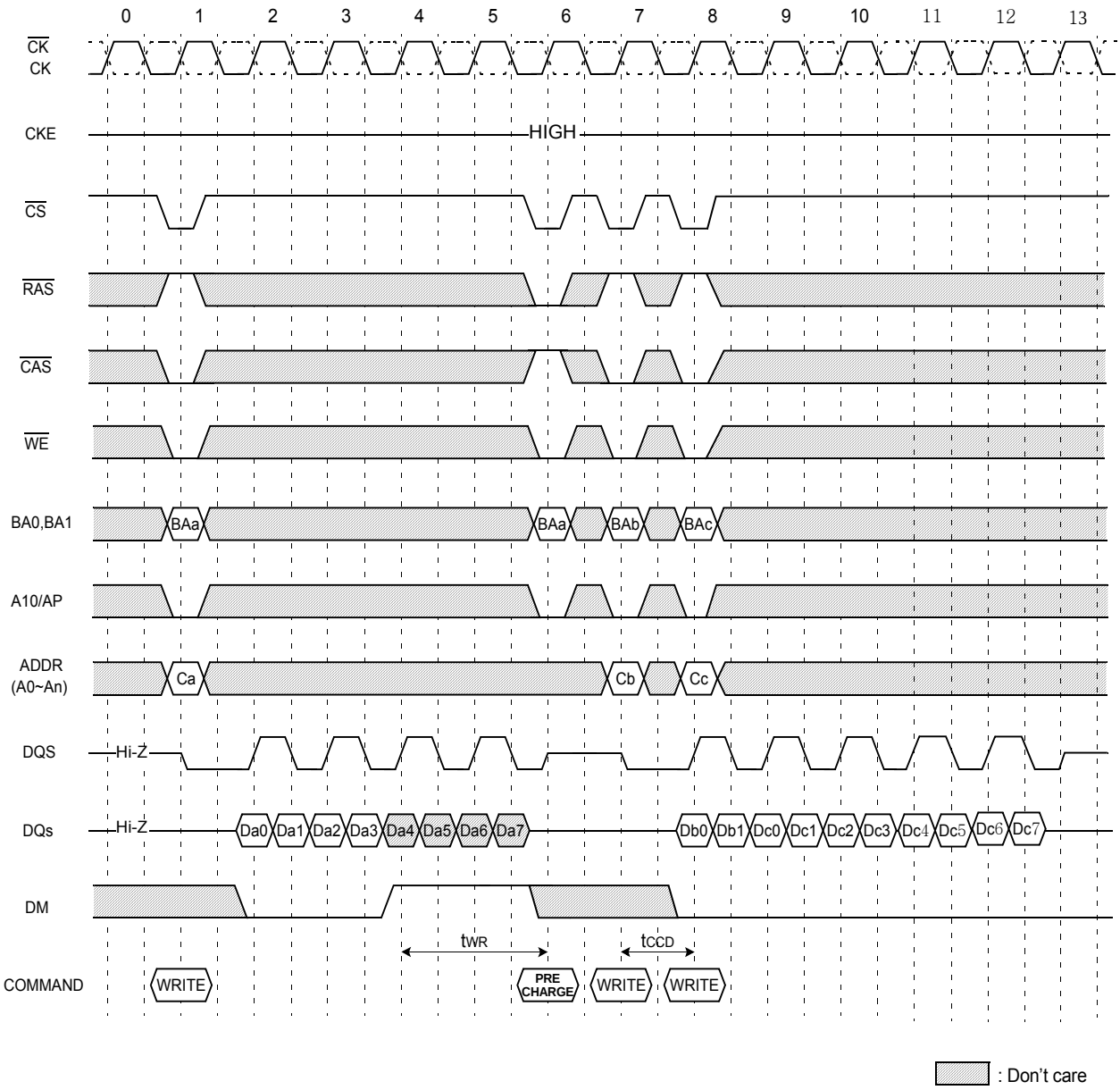


Figure 25. Write Interrupted by Precharge & DM (@BL=8)

9. WRITE INTERRUPTED BY A READ

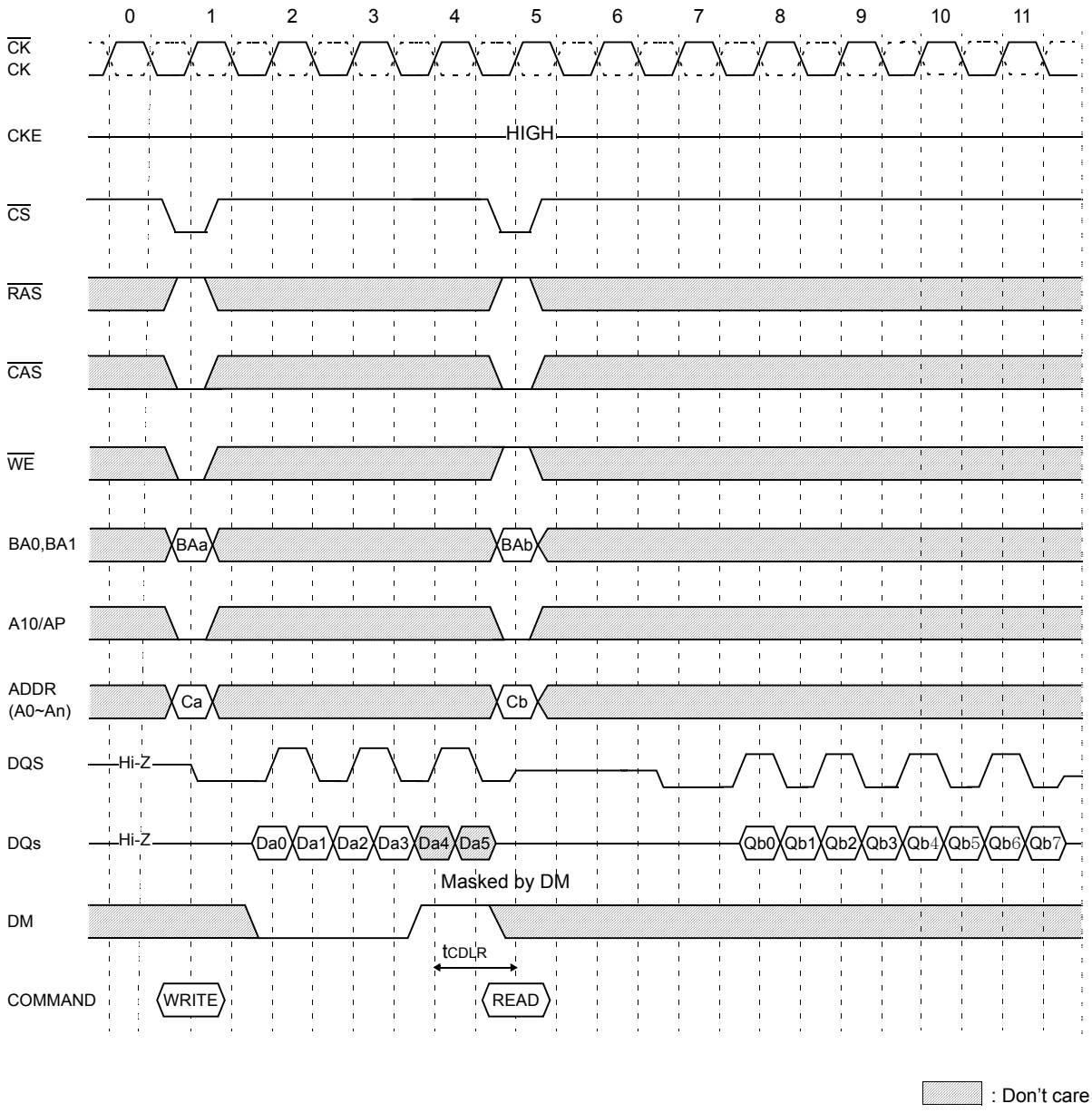


Figure 26. Write Interrupted by a Read (@BL=8, CL=3)

10. READ INTERRUPTED BY PRECHARGE

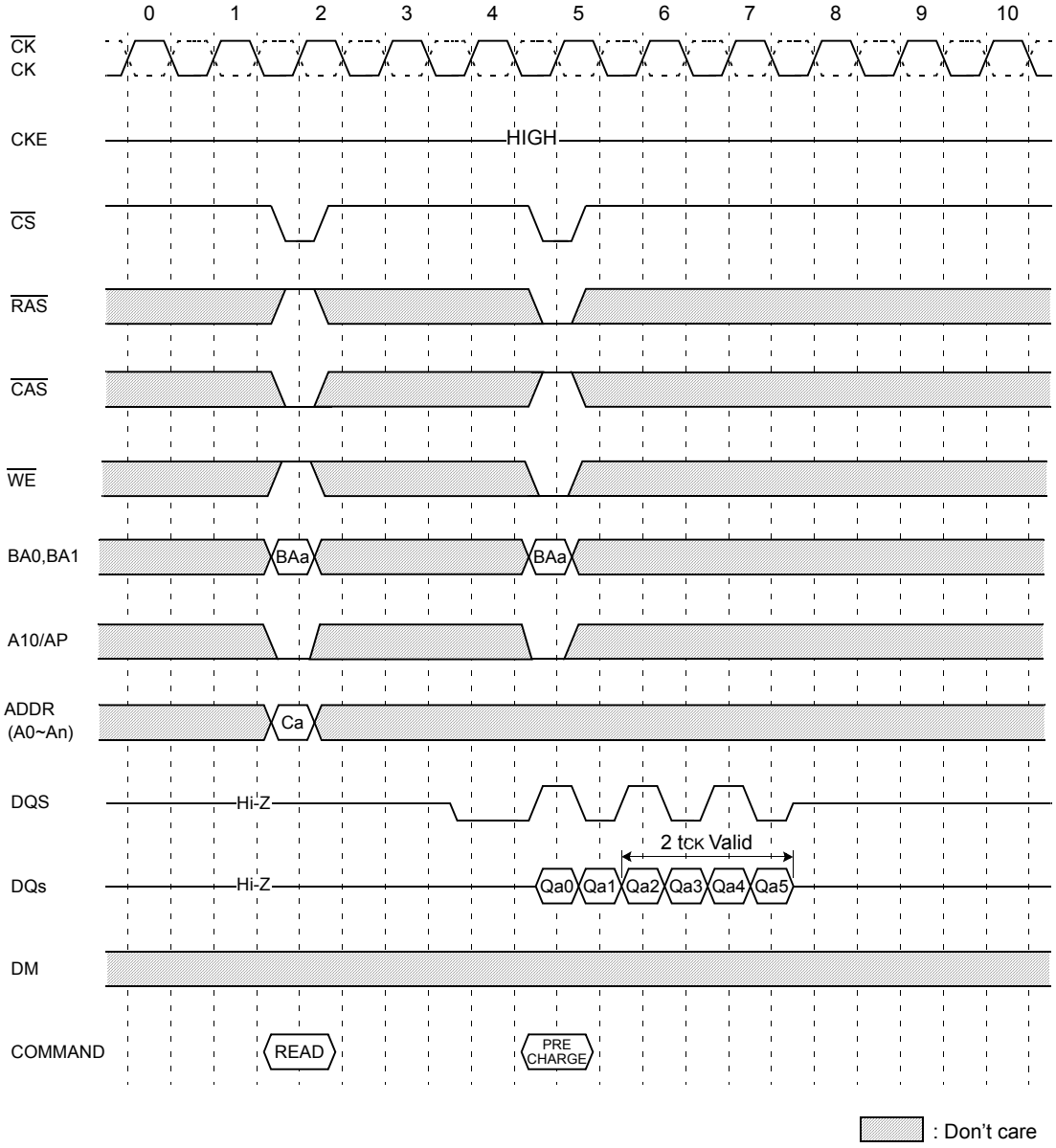


Figure 27. Read Interrupted by Precharge (@BL=8, CL=3)

11. READ INTERRUPTED BY A WRITE & BURST STOP

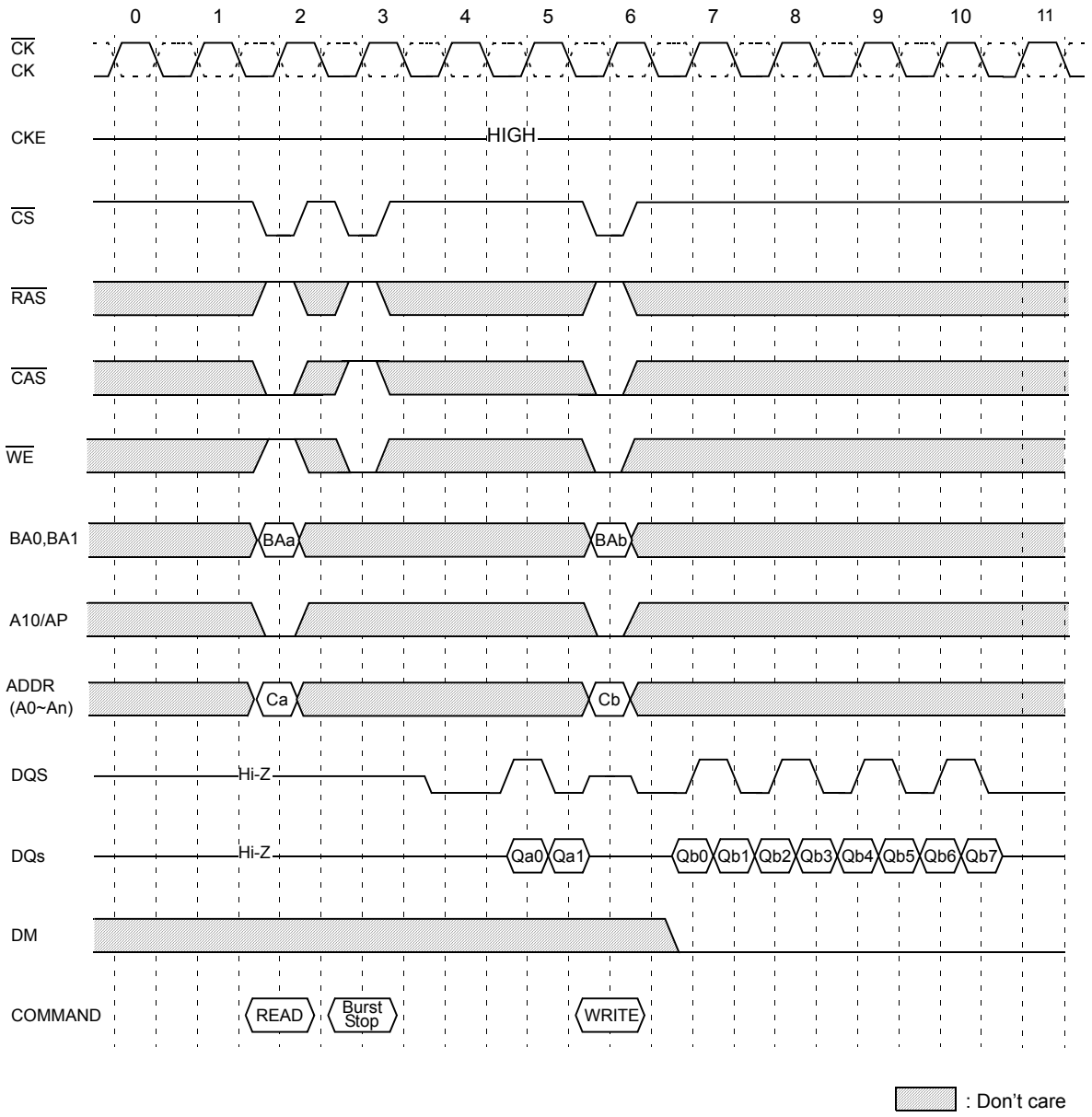


Figure 28. Read Interrupted by a Write & Burst Stop (@BL=8, CL=3)

12. READ INTERRUPTED BY A READ

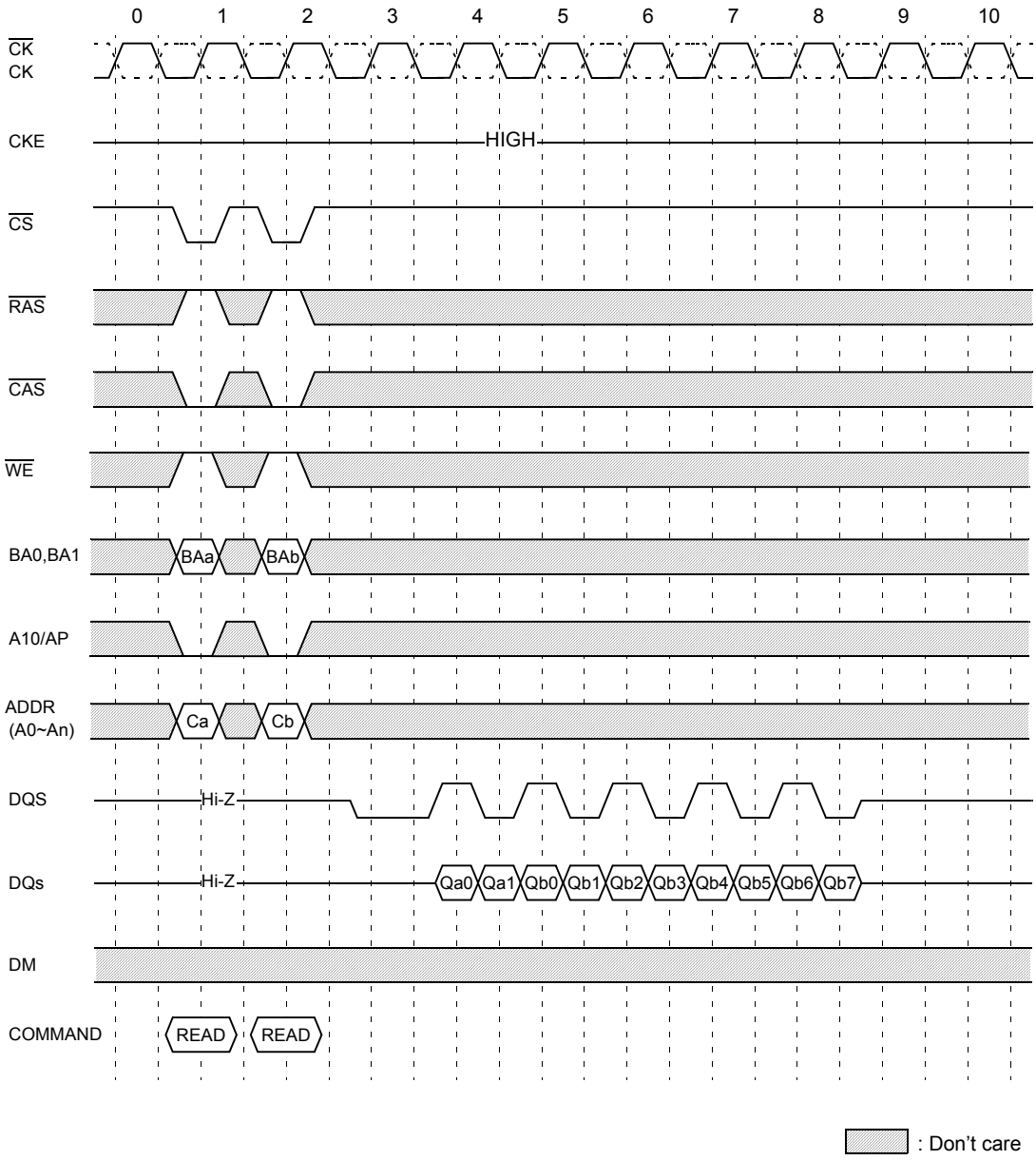


Figure 29. Read Interrupted by a Read (@BL=8, CL=3)

13. DM FUNCTION

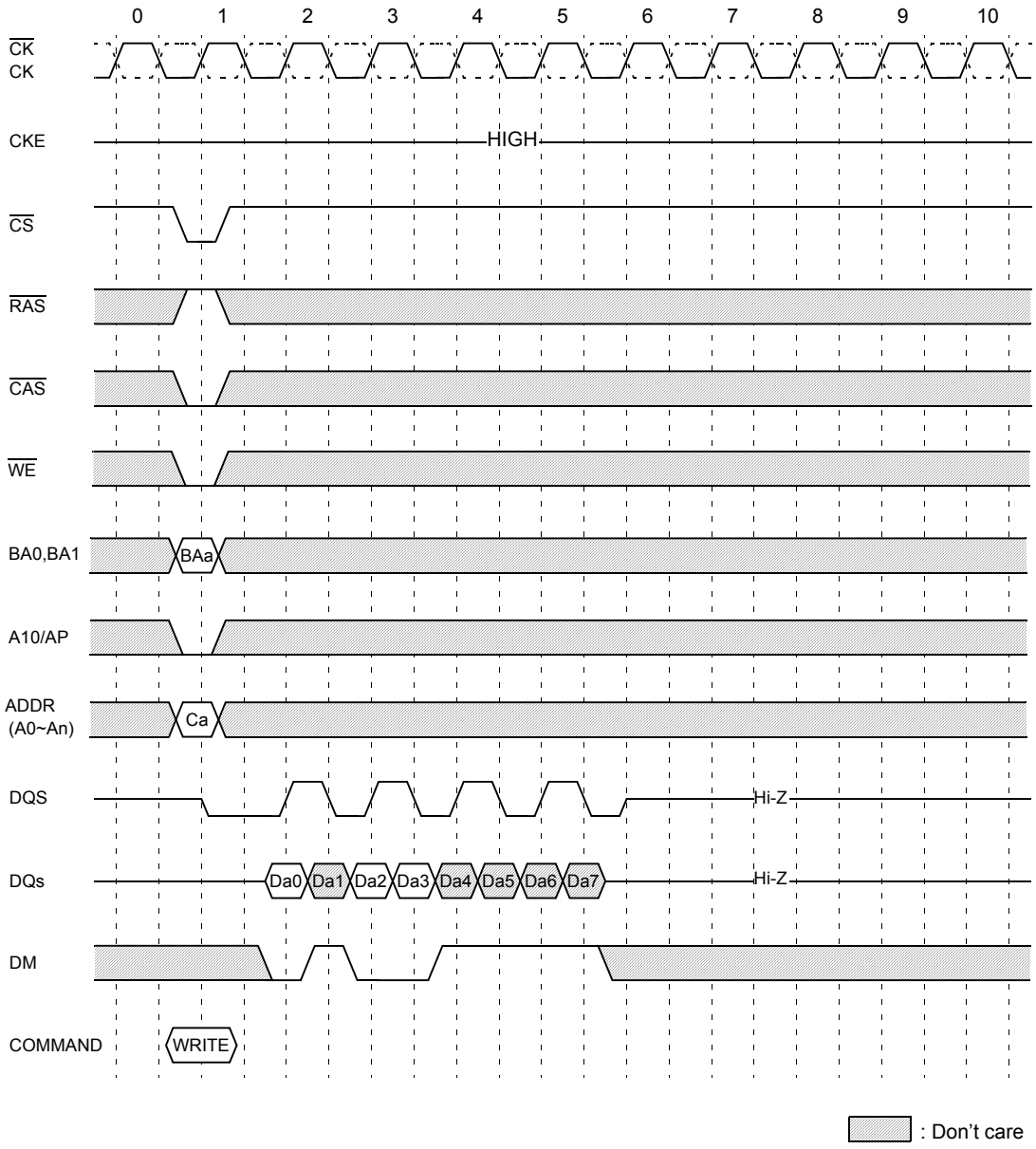


Figure 30. DM Function (@BL=8) only for write

14. DEEP POWER DOWN MODE ENTRY & EXIT CYCLE

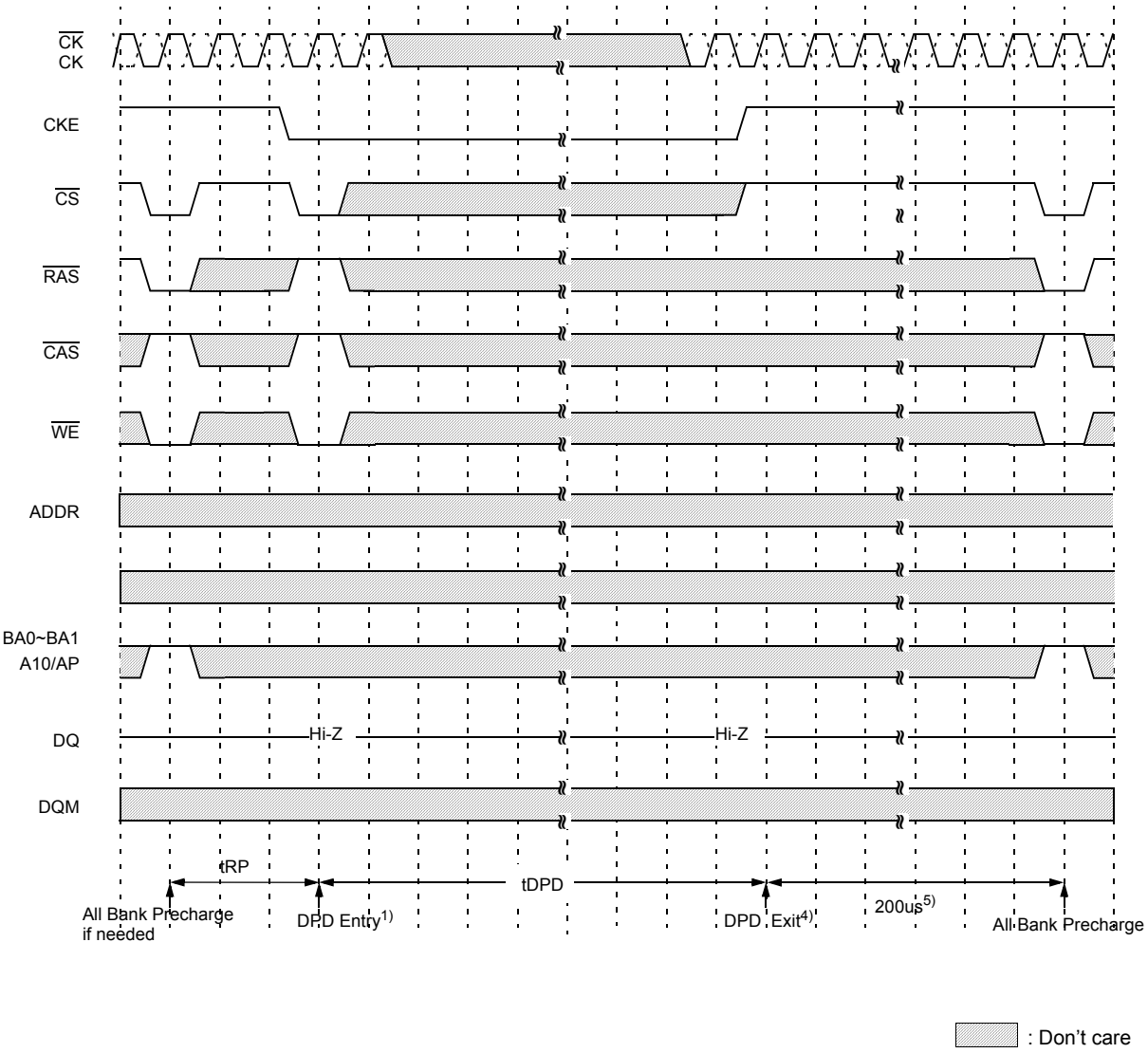


Figure 31. Deep Power Down Mode Entry & Exit Cycle

NOTE :

DEFINITION OF DEEP POWER DOWN MODE FOR Mobile DDR SDRAM :

Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory of the devices. Once the device enters in Deep Power Down Mode, data will not be retained. Full initialization is required when the device exits from Deep Power Down Mode.

TO ENTER DEEP POWER DOWN MODE

1) The deep power down mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock while CKE is low.
2) Clock must be stable before exiting deep power down mode.
3) Device must be in the all banks idle state prior to entering Deep Power Down mode.

TO EXIT DEEP POWER DOWN MODE

4) The deep power down mode is exited by asserting CKE high.
5) In case of 2 /CS, 2 CKE device with 2/CS & 2CKE, 200us wait time is required even if only 1 device exits from Deep Power Down.
6) Upon exiting deep power down, an all bank precharge command must be issued followed by two auto refresh commands and a load mode register sequence.