Technical Data

PST KP1003

HIGH POWER PHASE CONTROL THYRISTOR
FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 1600 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		1600		V	Tj = -40 °C to 125 °C
Repetitive peak off-state voltage	V_{DRM}		1600		V	Tj = -40 °C to 125 °C
Non repetitive peak reverse voltage	V_{RSM}		1700		V	Tj = -40 °C to 125 °C
Repetitive peak reverse current	I_{RRM}		50		mA	Tj = Tjmax , V = V_{RRM}
Repetitive peak off-state current	I_{DRM}		50		mA	Tj = Tjmax ,V = V_{DRM}

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		1350		A	50 Hz sine wave,180° conduction, T_c = 85 °C
RMS value of on-state current	$I_{T(RMS)}$		2120		A	50 Hz sine wave,180° conduction, T_c = 85 °C
Surge non repetitive current	I_{TSM}		27		kA	50 Hz sine wave Half cycle
I square t	I^2t		3645		kA^{2}s	V_R = 0 T_j = T_{jmax}
Peak on-state voltage	V_{TM}		1.39		V	On-state current 2900 A, Tj= Tjmax
Threshold voltage	$V_{T(TO)}$		0.80		V	T_j = T_{jmax}
On-state slope resistance	r_T		0.21		mΩ	T_j = T_{jmax}
Holding current	I_H			400	mA	V_D = 12 V; I_T = 2.5 A
Latching current	I_L			800	mA	V_D = 12 V; R_L = 12 Ω

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		350		mA	$V_D = 6$ V, $R_L = 3$ Ω, Tj = - 40 °C
			250		mA	$V_D = 6$ V, $R_L = 3$ Ω, Tj = 25 °C
			125		mA	$V_D = 6$ V, $R_L = 3$ Ω, Tj = 125 °C
Gate voltage	V_{GT}		5		V	$V_D = 6$ V, $R_L = 3$ Ω, Tj = - 40 °C
			3		V	$V_D = 6$ V, $R_L = 3$ Ω, Tj = 0 ÷ 125 °C
		0.3			V	$V_D = V_{DRM}$, $R_L = 1$ kΩ, Tj = 125 °C
Peak gate current	I_{GM}		10		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		200		W	
Average gate power dissipation	$P_{G(AV)}$		5		W	

Switching

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	di/dt		200		A/µs	$I_G = 5 \cdot I_{GT}$, $t_r = 1$µs, $V_{DRM} \leq 1000$V, $T_j = T_{jmax}$
Critical rate of rise of on-state voltage	dv/dt		500		V/µs	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d		3		µs	$I_{TM} = 50$ A, $V_D = 67\% V_{DRM}$, $V_G = 20$ V $R_G = 20$ Ω, $t_r = 0.1$ µs, $t_p = 20$ µs
Turn-off time	t_q		250		µs	$I_{TM} = 1000$ A; di/dt = 10 A/µs; $V_R \geq 100$ V dV/dt = 20 V/µs linear to 67% V_{DRM} $V_G = 0$ V; $T_j = T_{jmax}$
Reverse recovery charge	Q_{rr}				µC	$I_T = 500$ A di/dt = 20 A/µs
Reverse recovery current	I_{rr}				A/µs	$V_R \geq 50$ V $T_j = T_{jmax}$

Thermal and mechanical

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		°C	
Storage temperature	T_{stg}	-40	150		°C	
Thermal resistance junction to case	$R_{th(j-c)}$		0.020		°C/W	Double side cooled, 180° SIN
Thermal resistance case to sink	$R_{th(c-s)}$		0.006		°C/W	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	F	20	24		kN	
Weight	W			480	g	

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Thermal impedance junction to case

On-state characteristic

Tj = Tjmax

Surge current vs number of cycles

Tj = Tjmax

$V_R = 0$
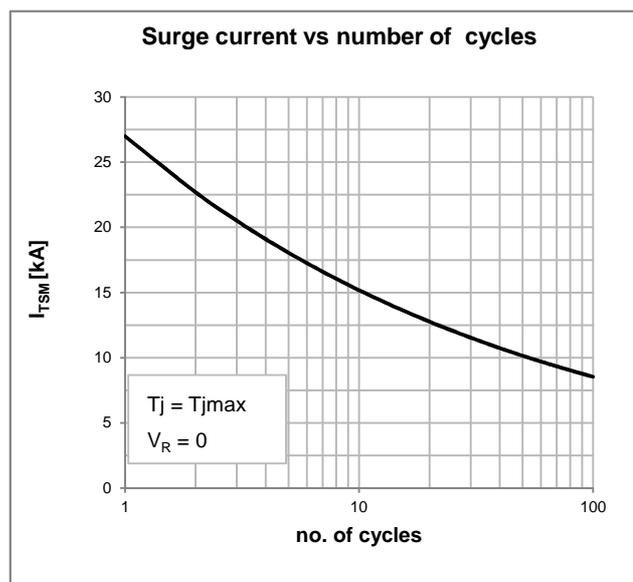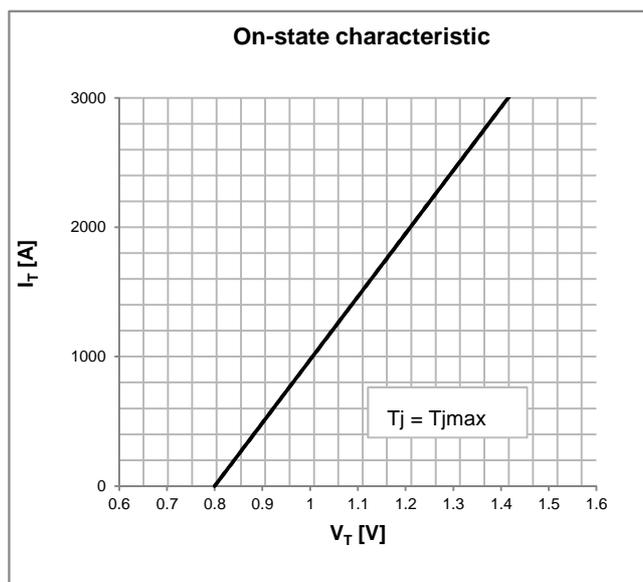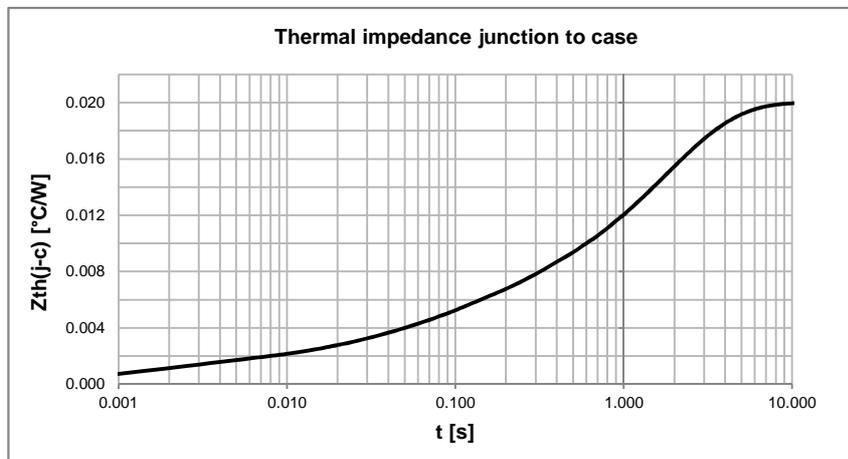
OUTLINE AND DIMENSIONS

$\phi\ 3.5 \times 2$

20°

MARKING
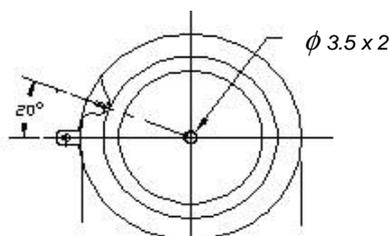
mm	A	B	C	E
	47	75	66	26 ± 0.5
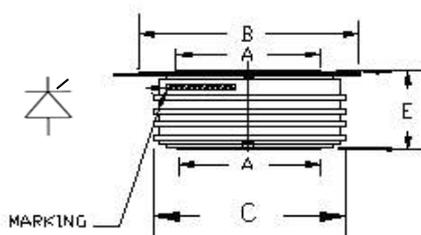
- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2μm