

### Feature

- Full diffusion process, capsule type ceramic package
- Amplifying gates
- Double sided cooling

### Typical Application

- High power transmission
- DC and AC motor control, Controlled rectifier
- AC DC switch, phase-controlled rectifying
- Active and reactive invresion

$I_{T(AV)}$	2000A
$V_{DRM}/V_{RRM}$	100-6500V
$I_{TSM}$	25KA
$I^2t$	$6125 \cdot 10^3 a^2s$

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_J$ (°C)	VALUE		UNIT
				Min	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, THS=97°C	125		2000	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, THS=55°C	125		2418	A
$V_{DRM}$ $V_{RRM}$	Repetitive peak off-state voltage Repetitive peak reverse voltage	$V_{DRM} \& V_{RRM} t_p = 10ms$ $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100V$	125	100	6500	V
$I_{DRM}$ $I_{RRM}$	Repetitive peak current	$V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$	125		200	mA
$I_{TSM}$	Surge on-state current	10ms half sine wave	125		25	KA
$I^2t$	$I^2t$ for fusing coordination	$V_R = 0.6V_{RRM}$			6125	$A^2S^*10$
$V_{TO}$	Threshold voltage		125		0.87	V
$r_T$	On-state slop resistance				0.14	mΩ
$V_{TM}$	Peak on-state voltage	$I_{TM} = 5000A, F = 15KN$	25		2.4	V
dv/dt	Critical rate of rise of-state voltage	$V_{DM} = 0.67V_{DRM}$	125		1000	V/us
di/dt	Critical rate of rise of on-state current	$V_{DM} = 67\% V_{DRM}$ TO 1000A, Gate pulse $t_r \leq 0.5us$ $I_{GM} = 1.5A$	125		250	A/us
$I_{TM}$	Reverse recovery current	$I_{TM} = 5000A, t_q = 1000us$ $Di/dt = -20A/us.$ $V_i = 50V$	125		170	A
$t_{rr}$	Reverse recovery time				20	us
$Q_{rr}$	Recovery charge				1700	uC
$I_{GT}$	Gate trigger current	$V_A = 12V, I_A = 1A$	25	40	300	mA
$V_{GT}$	Gate trigger voltage			0.8	3.0	V
$I_H$	Holding current			20	300	mA
$V_{GD}$	Npn-trigger gate voltage	$V_{DM} = 0.67V_{DRM}$	125	0.3		V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180° sine double side cooled Clamping force 5.0kn			0.011	°C/W
$F_M$	Mounting force			35	47	KN
$T_{stq}$	Stored temperature			-40	140	°C
$W_t$	Weight					g
Outline						

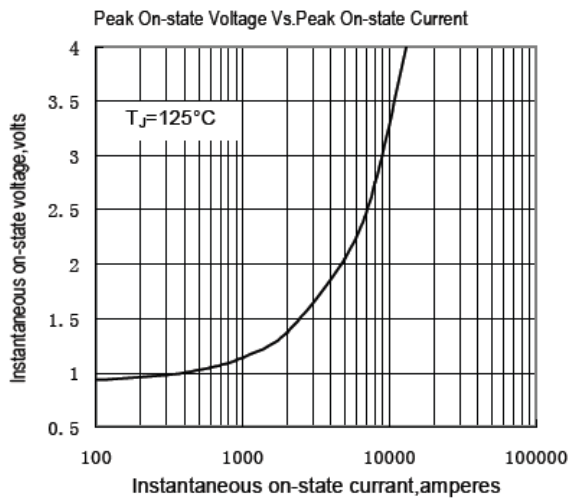


Fig.1

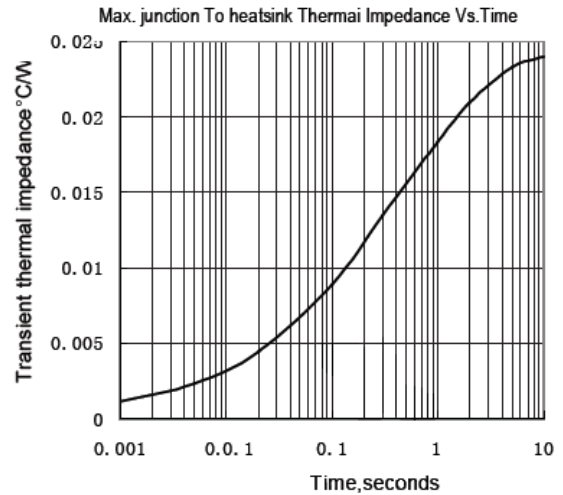


Fig.2

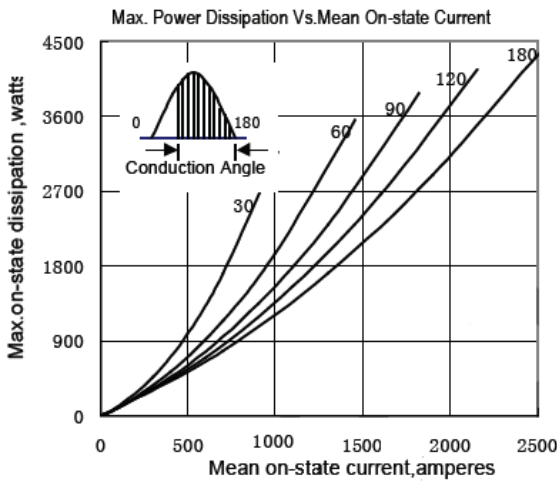


Fig.3

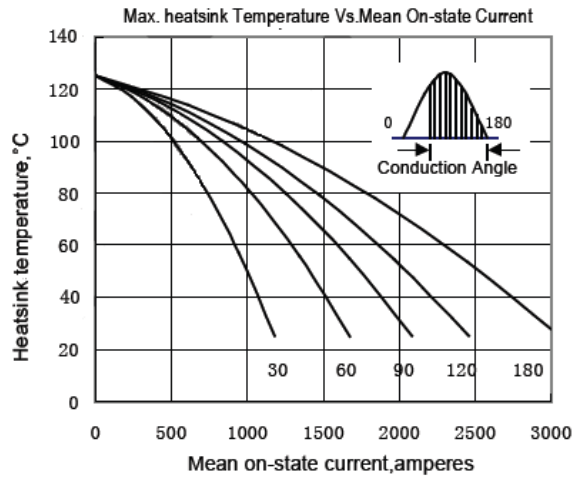


Fig.4

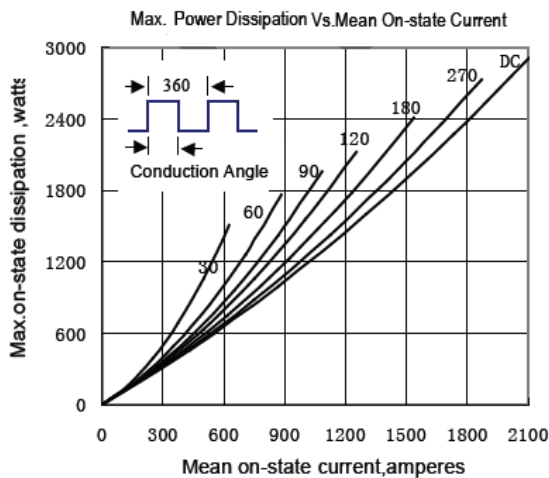


Fig.5

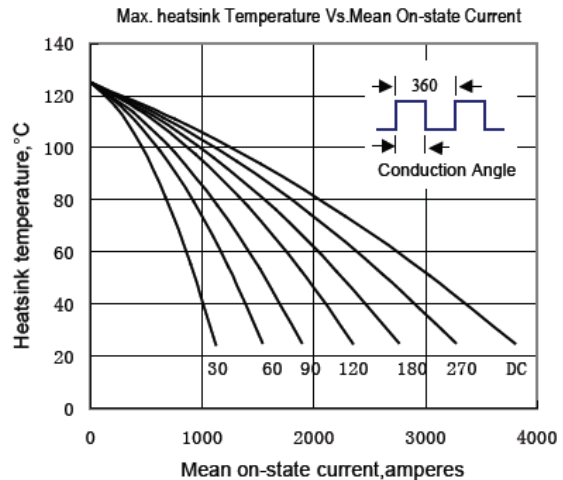


Fig.6

Surge Current Vs.Cycles

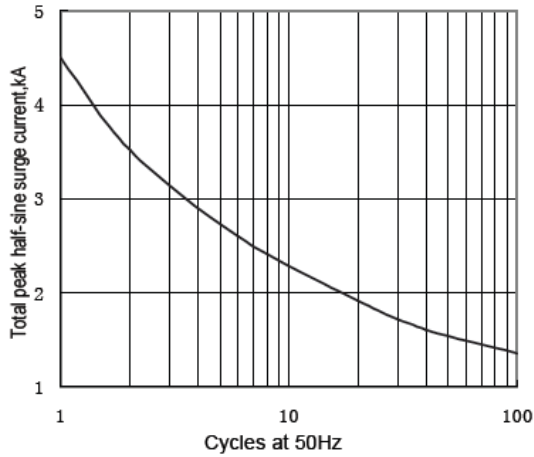


Fig.7

$I^2t$  Vs.Time

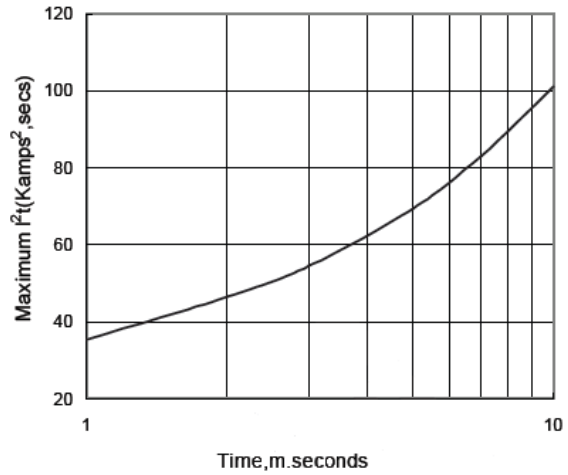


Fig.8

Gate characteristic at 25°C junction temperature

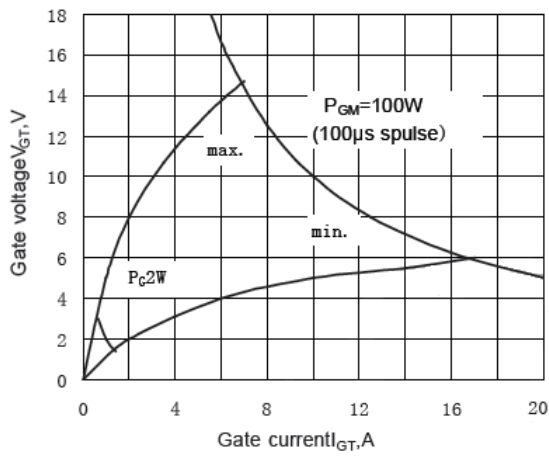


Fig.9

Gate Trigger Zone at varies temperature

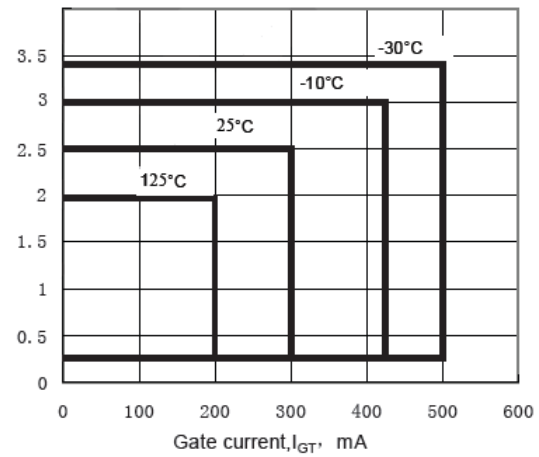


Fig.10

### Outline:

