Offline Current Mode PWM Controller with Built-in CC Regulation

FEATURES

- **Primary Side Constant-Current (CC) Control for DCM and CCM Operation**
- **±5% CC Regulation; ±1% CV Regulation**
- **Less than 75mW Standby Power**
- **Fixed 65kHz Switching Frequency**
- **Green Mode and Burst Mode Control**
- **Very Low Startup and Operation Current**
- **Built-in Frequency Shuffling to Reduce EMI**
- **Built-in Current Mode Control with Internal Slope Compensation**
- **Built-in Line & Inductance Compensation for CC Operation**
- **Built-in Protections with Auto Recovery:**
  - **VDD Under Voltage Lockout (UVLO)**
  - **VDD Over Voltage Protection (OVP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **Cycle-by-Cycle Current Limiting**
  - **Over Load Protection (OLP)**
  - **Short Circuit Protection (SCP)**
  - **Leading Edge Blanking (LEB)**
  - **CS Pin Float Protection**
- **Available with SOT23-6L Package**

APPLICATIONS

- **Chargers and Adapter**
- **Motor Driver Power Supply**

GENERAL DESCRIPTION

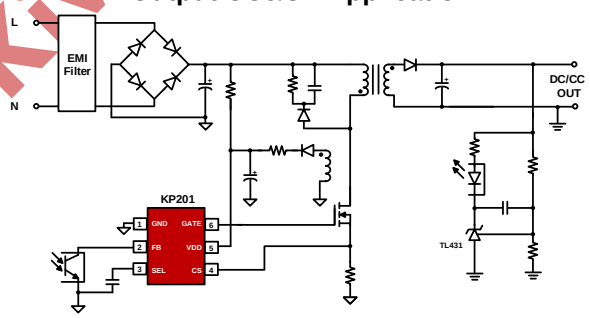
KP201 is a high performance current mode PWM controller for offline flyback converter applications. The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

In KP201, PWM switching frequency with shuffling is fixed to 65 kHz and is trimmed to tight range. The IC has built-in green and burst mode control for light and no load condition, which can achieve less than 75mW standby power.

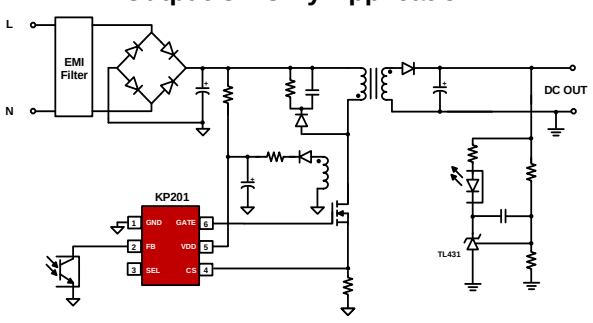
KP201 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Circuit Protection (SCP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD clamping and CS Pin Float Protection, etc.

TYPICAL APPLICATION CIRCUIT

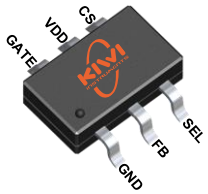
Output CC&CV Application



Output CV Only Application



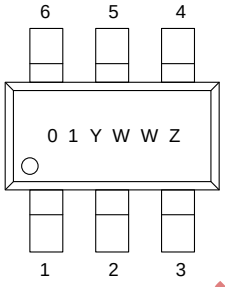
Pin Configuration



SOT23-6L

Marking Information

01: Specified Part Number for KP201
Y: Year Code
WW: Week Code, 01-52
Z: Serial Number, 1-9 or A-Z



SOT23-6L

Pin Description

Pin Number	Pin Name	I/O	Description
1	GND	P	The Ground of the IC
2	FB	I	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4
3	SEL	I	Connect a capacitor (typically value is 10-47nF) between SEL and GND to make the IC work in CC/CV mode. If SEL pin is floated, the IC will work in CV mode only
4	CS	I	Current Sense Input Pin
5	VDD	P	IC Power Supply Pin
6	GATE	O	Totem-pole Gate Driver Output to Drive the External MOSFET

Ordering Information

Part Number	Description
KP201LGA	SOT23-6L, Halogen free, in T&R,3000 Pcs/Reel

Note: Suffix "A" - Tape&Reel

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	-0.3 to 33	V
VDD DC Clamp Current	10	mA
FB, CS, SEL voltage range	-0.3 to 7	V
GATE voltage range	-0.3 to 20	V
Package Thermal Resistance---Junction to Ambient (SOT23-6L)	250	˚C/W
Maximum Operating Junction Temperature	150	˚C
Storage Temperature Range	-65 to 150	˚C
Lead Temperature (Soldering, 10sec.)	260	˚C
ESD Capability, HBM (Human Body Model)	3	kV

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, VDD	10 to 28	V
Chip Operating Junction Temperature	-40 to 125	˚C

Electrical Characteristics (TA= 25˚C, VDD=24V, if not otherwise noted)

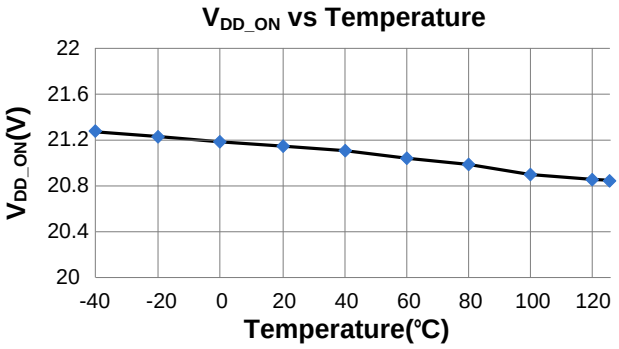
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin	VDD Before Start up		2	15	μA
I_{VDD_Op}	Operation Current			1.2		mA
I_{VDD_sb}	Standby Current	V_{FB}=0V,VDD=22.5V	0.3	0.6	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		18.5	21	22.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8	9	10	V
V_{DD_OVP}	VDD OVP Threshold		29	31	33	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	33	35	38	V
Feedback Input Section (FB Pin)						
V_{FB_Open}	FB Open Voltage			5.5		V
I_{FB_Short}	FB Short Circuit Current	V_{FB}=0V		0.3		mA
Z_{FB_IN}	FB Input Impedance			20		kΩ
V_{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V

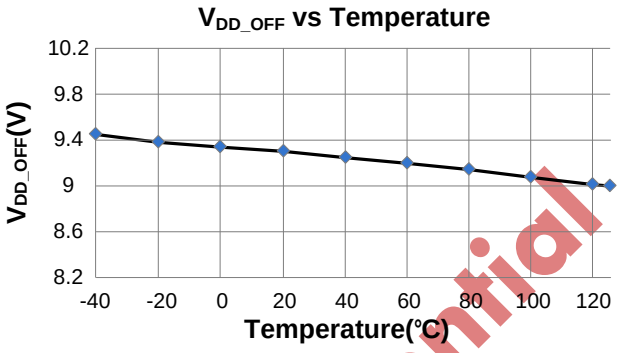
T_{D_OLP}	Power Limiting Debounce Time	SEL Pin is floating		75		ms
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{cs\_max\_CV\_H}$	Current limiting threshold in CV	Duty>50%	0.97	1.0	1.03	V
$V_{cs\_max\_CV\_L}$		Duty<10%	0.73	0.76	0.79	V
$V_{cs\_max\_CC}$	Current limiting threshold in CC			1.2		V
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	kHz
$\Delta F(shuffle)/F_{OSC}$	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling Period			32		ms
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Bust}	Burst Mode Base Frequency			22		kHz
CC Loop Regulation Section (SEL = Capacitor)						
$V_{CC\_Reg\_SEL}$	Internal Reference for CC Loop Regulation			300		mV
$I_{CC\_SEL\_Source}$	Internal Source Current for CC Loop Regulation			20		μA
$V_{CC\_SLP\_SEL}$	Short Load Protection (SLP) Threshold			0.7		V
$T_{CC\_Short\_SEL}$	Short Load Protection (SLP) Debounce Time			210		ms
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 2)		165		℃
T_{RC}	Thermal Recovery	(Note 2)		140		℃
Driver Section (GATE Pin) (Note 2)						
V_{OL}	Output Low Level	Igate_sink=20mA			1	V
V_{OH}	Output High Level	Igate_source=20mA	7.5			V
V_{G_Clamp}	Output Clamp Voltage Level	VDD=24V		13		V
T_r	Output Rising Time	GATE=1nF		150		ns
T_f	Output Falling Time	GATE=1nF		60		ns

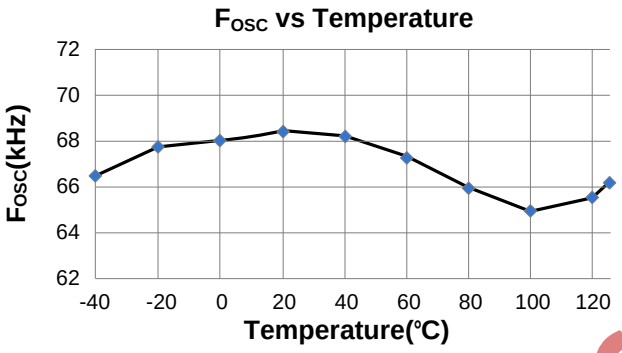
Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

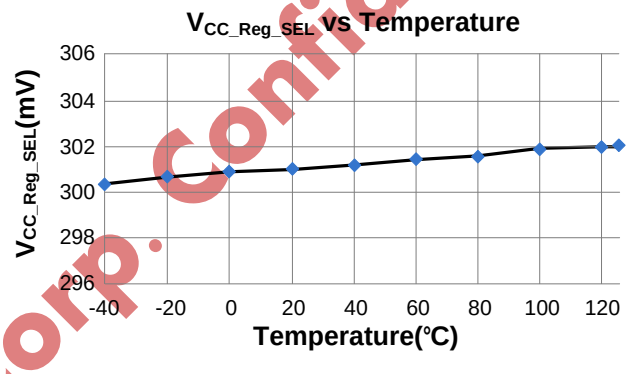
Note 2. Guaranteed by the Design.

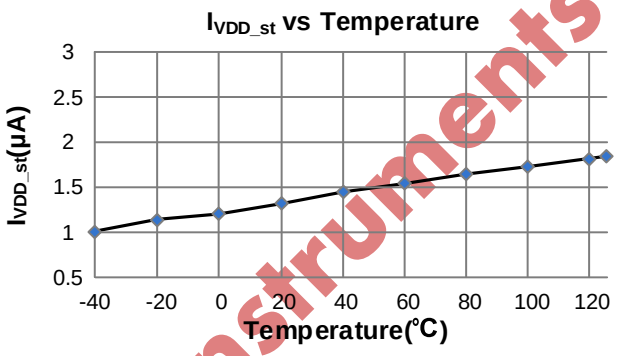
Characterization Plots

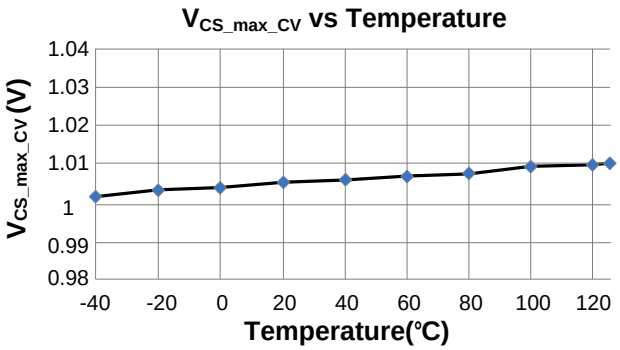












Operation Description

KP201 is a high performance current mode PWM controller for offline flyback charger, motor driver power supply, and adapter applications. The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

• System Start-Up Operation and IC Operation Current

Before the IC starts to work, it consumes only startup current (typically 2uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches turn on threshold V_{DD_ON} (typical 21V), KP201 begins switching and the IC operation current is increased to be 1.2mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. When the IC enters into burst mode, the IC operation current will decrease further, thus less than 75mW standby power can be achieved.

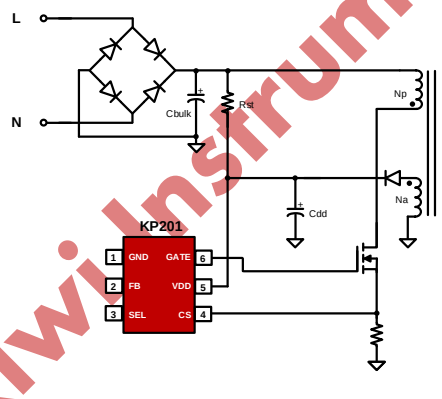


Fig.1

• General Primary Side Constant Current Modulation for DCM/CCM

Compared to conventional flyback DCM Primary Side Regulation (PSR) Constant Current (CC) method, a General Primary Side Constant Current Modulation algorithm is adopted in KP201, which supports transformer DCM and CCM operation simultaneously.

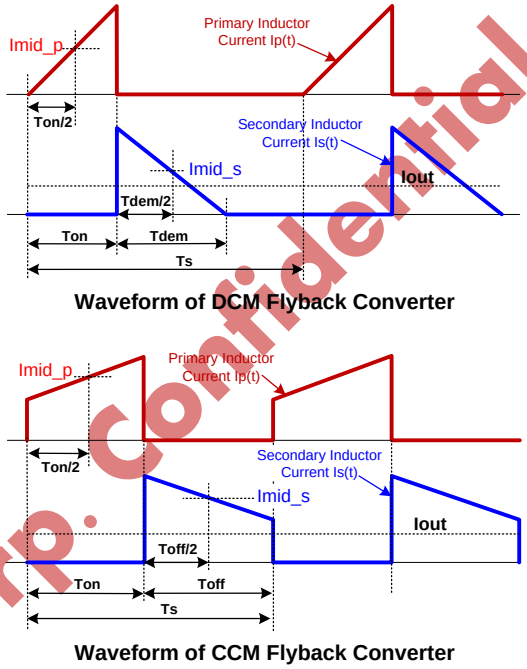


Fig.2

Fig.2 illustrates the key waveform of a flyback converter operating in DCM and CCM, respectively. The output current Iout of each mode is estimated by calculating the average current of secondary or primary inductor over one switching cycle:

$$I_{OUT} = \frac{\int_0^{T_S} I_S(t)dt}{T_S} = N \times \frac{\int_0^{T_S} I_P(t)dt}{T_S} \quad (1)$$

In Eq(1) above, Is(t) is the secondary inductor or rectification diode current, Ip(t) is the primary inductor current, N is primary-to-secondary transformer turn ratio.

The average secondary inductor current in both DCM and CCM can be expressed in a same form, as a product of secondary inductor discharge time T_{DIS} and secondary inductor current at the middle of T_{DIS}, such as:

$$\int_0^{T_S} I_S(t)dt = I_{mid\_S} \times T_{DIS} = N \times I_{mid\_P} \times T_{DIS} \quad (2)$$

In Eq.(2), I_{mid_S} and I_{mid_P} are the secondary and primary inductor current at the middle of T_{DIS} and T_{ON} respectively, as shown in Fig.2. T_{DIS} can be given by the following equation:

$$T_{DIS} = \begin{cases} T_{DEM} & (\text{for DCM mode}) \\ T_{OFF} & (\text{for CCM mode}) \end{cases} \quad (3)$$

In Eq(3), $T_{DIS}=T_{DEM}$ for DCM operation and $T_{DIS}=T_{OFF}$ for CCM operation respectively.

Combined with Eq.(1) to Eq. (3), the average output current Ioutcan be expressed as:

$$I_{OUT} = N \times I_{mid\_P} \times \frac{T_{DIS}}{T_S} = N \times \frac{V_{mid\_P}}{R_{CS}} \times \frac{T_{DIS}}{T_S} \quad (4)$$

InEq(4), R_{CS} is the sensing resistor connected between the power MOSFET source to GND. V_{mid_P} is sampled R_{CS} voltage at the middle of primary power MOSFET conduction time.

In KP201, the product of V_{mid_P} and T_{DIS} is kept constant by the IC's internal PWM CC regulation loop. The switching frequency is trimmed to 65KHz in KP201. Therefore, the average output current Iout will be well regulated and given by:

$$I_{CC\_OUT}(mA) = N \times \frac{V_{CC\_Reg}}{Rcs} \cong N \times \frac{300mV}{Rcs(\Omega)} \quad (5)$$

● Demagnetization Detection without Auxiliary Winding

In KP201, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor Crss between the drain and gate of power MOSFET. When the transformer is fully demagnetized, the drain voltage evolution is governed by the resonating energy transfer between the transformer inductor and the parasitic capacitance of the drain. These voltage oscillations create current oscillation in the parasitic capacitor Crss. A negative current takes place during the decreasing part of the drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion of the current by detecting this point, as shown in Fig.3.

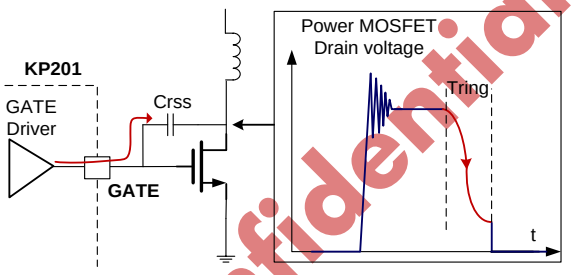


Fig.3

● Mode Selection for CV and CC/CV

The load of SEL pin determines the operation mode of IC. In KP201, the IC will work in CC/CV mode if an external capacitor is connected between SEL pin and GND. Otherwise, if SEL pin is floating, the IC will work in only CV mode.

● ± 5% CC Regulation, ±1% CV Regulation with Fast Dynamic Response

The CC algorithm in KP201 compensates line variation and transformer inductance tolerance. The IC can achieve ±5% CC regulation. The IC can also achieve ±1% CV regulation and fast dynamic response , due to the same control method as convention PWM controllers.

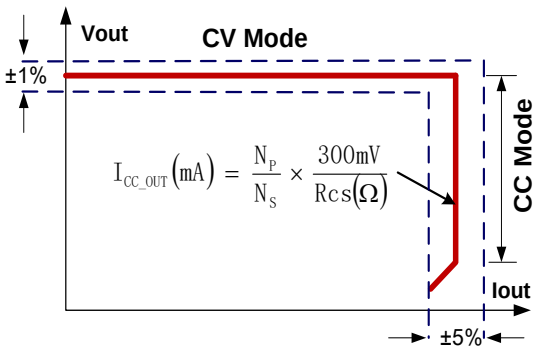


Fig.4

Oscillator with Frequency Shuffling

PWM switching frequency in KP201 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, KP201 operates the system with 4% frequency shuffling around setting frequency.

Green Mode Operation

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency. To meet green mode requirement, it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Foldback

In KP201, a Proprietary "Smooth Frequency Foldback" function is integrated to foldback the PWM switching frequency when the loading is light. Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

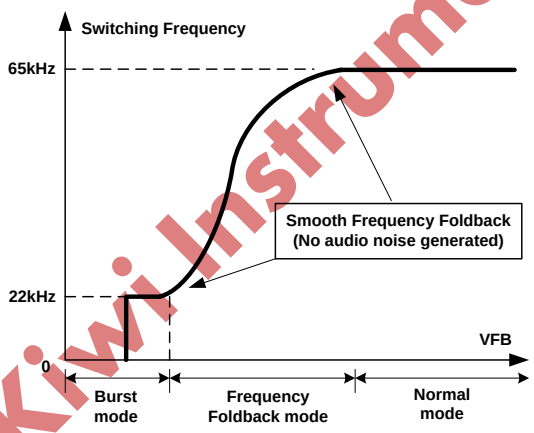


Fig.5

Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vs kip, KP201 will stop switching and output voltage starts to drop (as shown in Fig.6), which causes the VFB to rise. Once VFB rises above Vs kip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

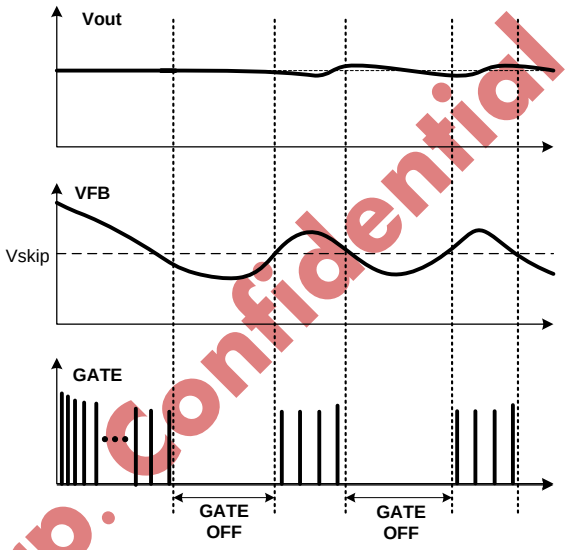


Fig.6

Built-in Slope Compensation

In the conventional application, the problem of the stability is a critical issue for current mode controlling, when it operates in higher than 50% of the duty-cycle. In KP201 the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver.

On Chip Thermal Shutdown (OTP)

When the IC temperature is over 165°C, the IC shuts down. Only when the IC temperature drops to 140°C, IC will restart.

Soft Start

KP201 features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

Constant Power Limiting in CV Mode

In CV mode, a proprietary "Constant Power Limiting" block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

Short Circuit Protection (SCP) in CC/CV Mode

In KP201, if the IC works in CC/CV mode and CC voltage is below 0.7V for over 210ms, the IC will enter into Short Circuit Protection (SCP) mode, in which the IC will enter into auto recovery protection mode.

Over Load Protection (OLP) in CV Mode

In CV mode and if over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient.

VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than 31V (typical), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typical 9V) and then the system will restart up again. An internal 35V (typical) zener clamp is integrated to prevent the IC from damage.

CS Pin Float Protection

When VDD voltage is higher than V_{DD_ON} (21V typical), IC firstly starts to check whether CS pin is floated. If CS pin is floated, switching is blocked and IC enters auto-recovery mode; otherwise, normal work begins. With this protection, system stability is enhanced.

Auto Recovery Mode Protection

As shown in Fig.7, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to V_{DD_OFF}(typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to V_{DD_ON} (typical21V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

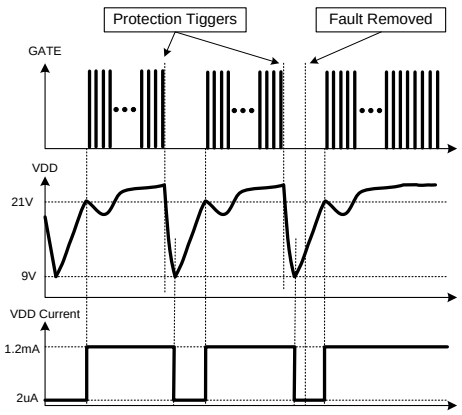


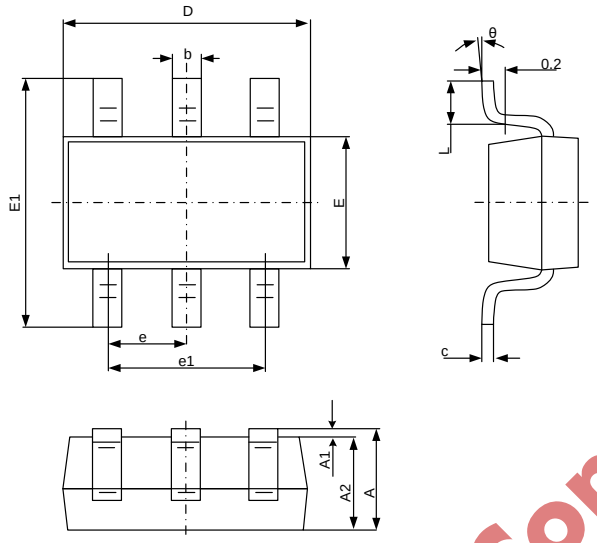
Fig.7

Soft Gate Driver

The output stage of KP201 is a totem-pole gate driver with 400mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 13V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

Package Dimension

SOT23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.350	-	0.053
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.220	0.004	0.009
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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