HUAJING

KP30A Standard Rectifier Diode

Feature

■ Hermetic ceramics-metal stud structure
■ Capacity of supporting high surge current

Typical Application

■ DC motor control,Control DC power supplie
■ AC swith and thermal control,Synchronous motor excitation

$I_{T(AV)}$	30A
V_{DRM}/V_{RRM}	100-3000V
I_{TSM}	415A
I^2t	725 A^2s

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} max. repetitive peak and off-state voltage (1) V	V_{RSM} maximum peak non-repetitive voltage (2) V	$I_{DRM}/I_{RRM} @T_J=T_J$ mA
KP30A	10	100	150	20
	20	200	300	10
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	
	140	1400	1500	
	160	1600	1700	

On-state Conduction

Symbol	Charteristic	KP30A 10-120	KP30A 140-160	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current @ Case temperature	30	30	A	180℃sinusoidal conduction		
$I_{T(RMS)}$	Max. RMS on-state current	40	40	A			
I_{TSM}	Max. peak, one-cycle non-repetitive surge current	420	398	A	t=10ms	No voltage reapplied	Sinusoidal half wave Initial$T_J=T_J$ Max
		440	415		t=8.3ms		
		350	335		t=10ms	100%V_{RRM} reapplied	
		370	350		t=8.3ms		
I^2t	Maximum I2t for fusing	790	795	A^2s	t=10ms	No voltage reapplied	
		867	725		t=8.3ms		
		560	560		t=10ms	100%V_{RRM} reapplied	
		615	510		t=8.3ms		
$V_{T(TO)1}$	Low level value of threshold voltage	0.99	0.99	V	(16.7% x x $I_{T(AV)}$ < I < π x $I_{T(AV)}$, $T_J=T_J$ Max		
$V_{T(TO)2}$	High level value of threshold voltage	1.40	1.15		(I > x $I_{T(AV)}$),$T_J=T_J$ Max		
R_{t1}	Low level value of on-state slope resistance	10.1	11.73	m Ω	(16.7% x x $I_{T(AV)}$ < I < π x $I_{T(AV)}$, $T_J=T_J$ Max		
R_{t2}	High level value of on-state slope resistance	5.7	10.05		(I > x $I_{T(AV)}$),$T_J=T_J$ Max		
V_{TM}	Max. on-state voltage	1.70	1.80		$I_{PK}=79A$,$T_J=25℃$		
I_H	Maximum holding current	130		mA	$T_J=25℃$，Anode supply 6V,resistive load		
I_L	Latching current	200					

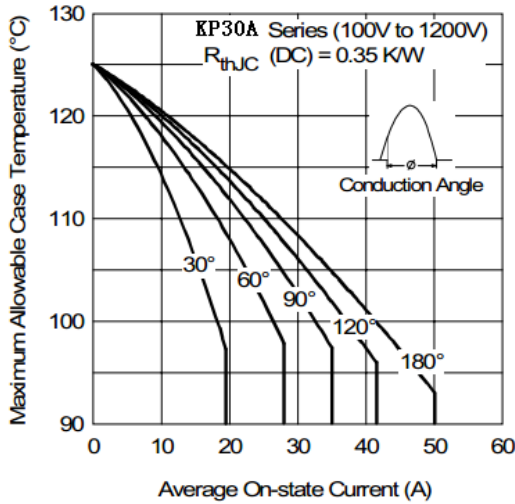| Symbol	Charteristic	KP30A	Units	Conditions
di/dt	Critical rate of rise of on-state current $V_{DRM} \leqq 600V$ $V_{DRM} \leqq 800V$ $V_{DRM} \leqq 1000V$ $V_{DRM} \leqq 1600V$	200 180 160 150	A/us	$T_J = T_J$ max., $V_{DM} = V_{DRM}$,15Ω ,$t_q \leqq 6us$, t_r= 0.1us max I_{TM}= (2×rated di/dt) A
t_{qt}	Typical turn-on time	0.9	us	T_J=25℃ At=V_{DRM}/V_{RRM},T_J=125℃
t_{rr}	Typical reverse recovery time	4	us	$T_J=T_J$ max, $I_{TM}=I_{T(AV)}$,$t_q >$ 200us,di/dt=-10A/us
t_q	Typical turn-off time	110	us	$T_J=T_J$ max,$I_{TM}=I_{T(AV)}$,$t_q >$ 200us,V_R=100V di/dt=-10A/us,dv/dt=-20A/us,$V_{DM}=67\%$ V_{DRM} 0V-100W
dv/dt	Max. critical rate of rise of off-state voltage	100	V/us	$T_J=T_J$ max,$V_{DM}=67\%V$ $_{DRM}$
P_{GM}	Gate trigger current	8.0	W	$T_J=T_J$ max
$P_{G(AV)}$	Gate trigger voltage	2.0	W	$T_J=T_J$ max
I_{GM}	Stored temperature	1.5	A	$T_J=T_J$ max
-V_{GM}	Thermal impedance node to the shell	10	V	$T_J=T_J$ max
I_{GT}	Thermal impedance (shell to powder)	90 60 35	mA	T_J=-65℃T_J=25℃T_J=125℃
V_{GT}	Mounting torque	3.0 2.0 1.0	V	T_J=-65℃T_J=25℃T_J=125℃
I_{GD}	Approximate weight	2.0	mA	$T_J=T_J$ max，67％V_{DRM}
V_{GD}	Critical rate of rise of on-state current $V_{DRM} \leqq 600V$ $V_{DRM} \leqq 800V$ $V_{DRM} \leqq 1000V$ $V_{DRM} \leqq 1600V$	0.2	V	$T_J=T_J$ max，67％V_{DRM}
T_J	Typical turn-on time	-65-125	℃	
T_{stg}	Typical reverse recovery time	-65-125	℃	
$R_{th(j-c)}$	Typical turn-off time	0.75	K/W	
$R_{th(c-s)}$	Max. critical rate of rise of off-state voltage	0.35	K/W	
T	Gate trigger current	3.1	Nm	
W_t	Gate trigger voltage	112	g	

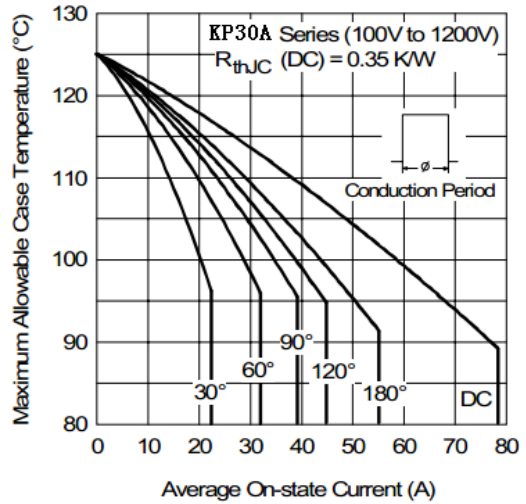Fig. 1 - Current Ratings Characteristic

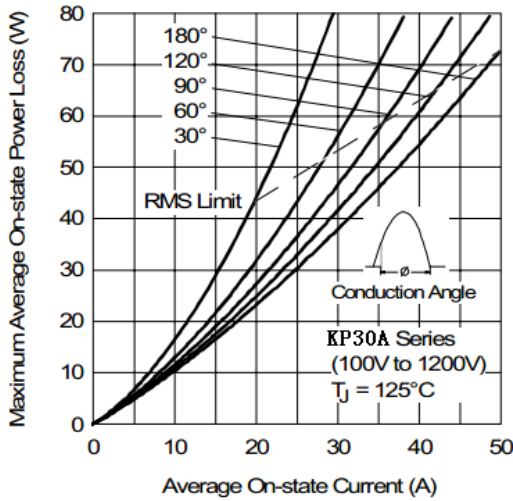Fig. 2 - Current Ratings Characteristic

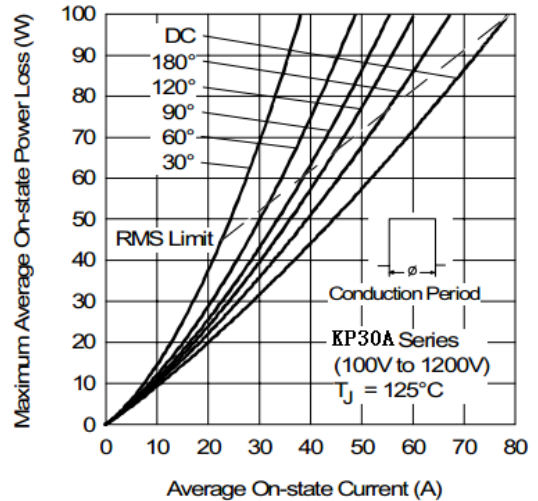Fig. 3 - On-state Power Loss Characteristics

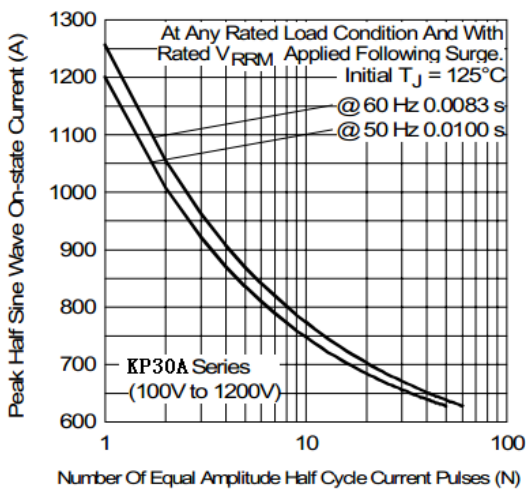Fig. 4 - On-state Power Loss Characteristics

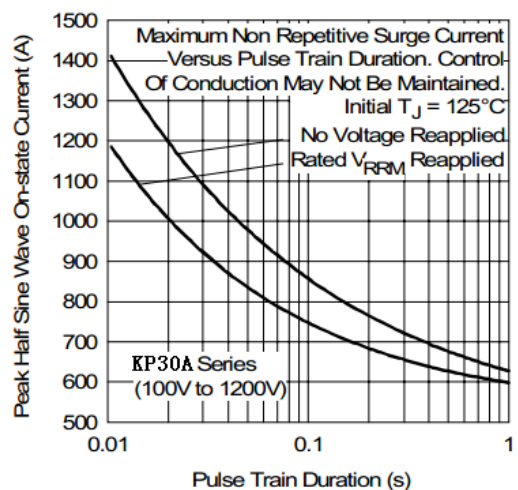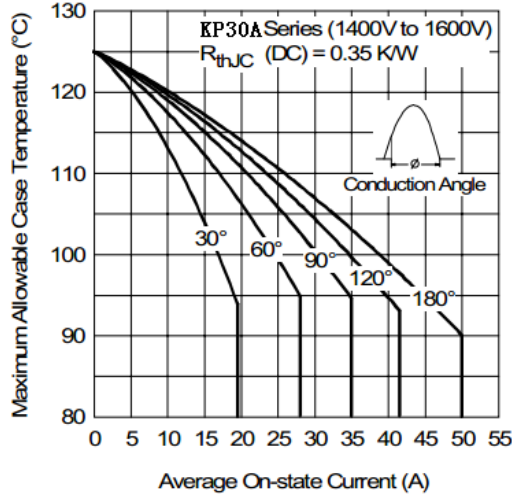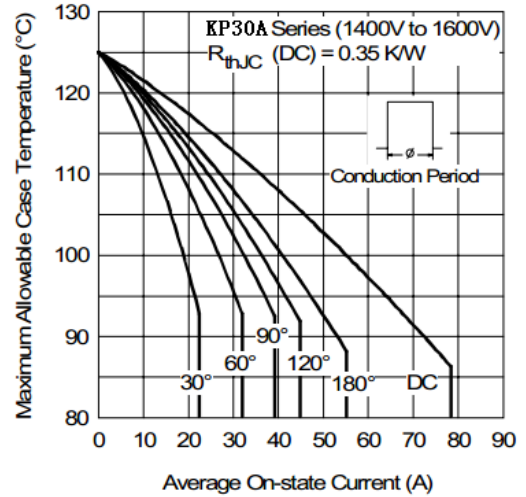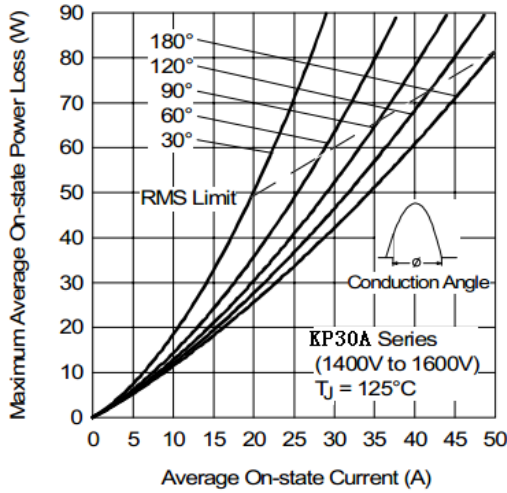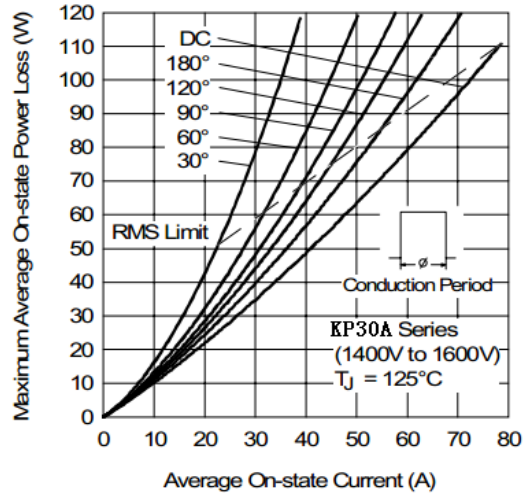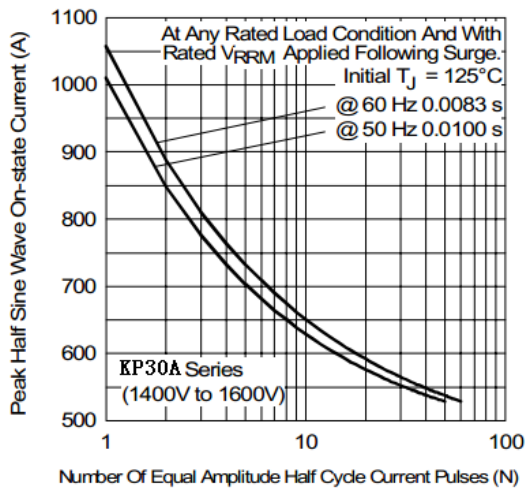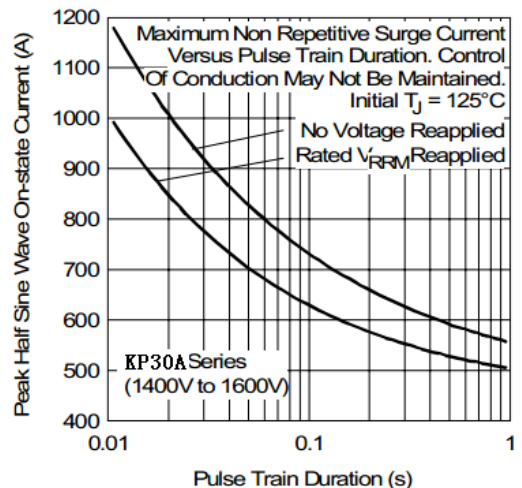Fig. 5 - Maximum Non-Repetitive Surge Current

Fig. 6 - Maximum Non-Repetitive Surge Current

Fig. 7 - Current Ratings Characteristics

Fig. 8 - Current Ratings Characteristics

Fig. 9 - On-state Power Loss Characteristics

Fig. 10 - On-state Power Loss Characteristics

Fig. 11 - Maximum Non-Repetitive Surge Current
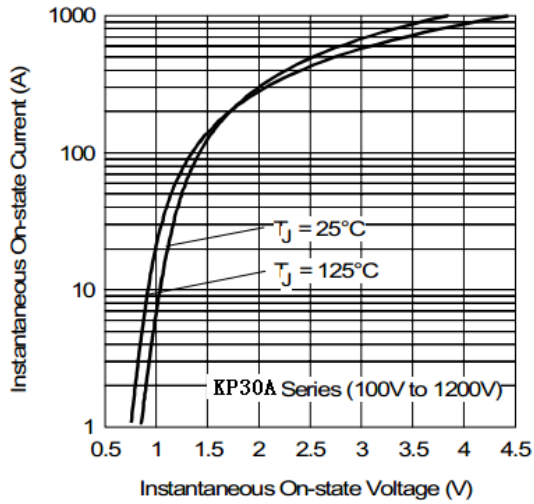
Fig. 12 - Maximum Non-Repetitive Surge Current

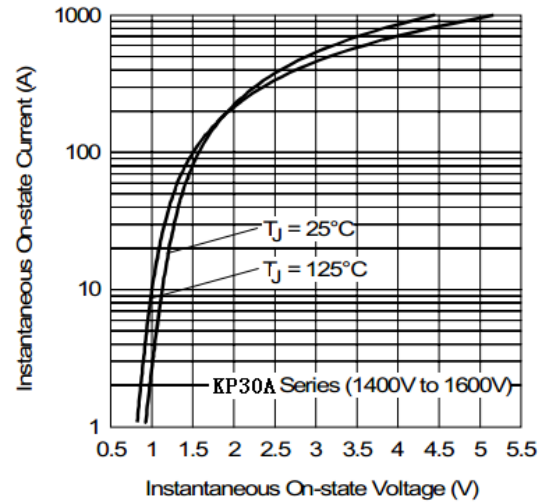Fig. 13 - Forward Voltage Drop Characteristics

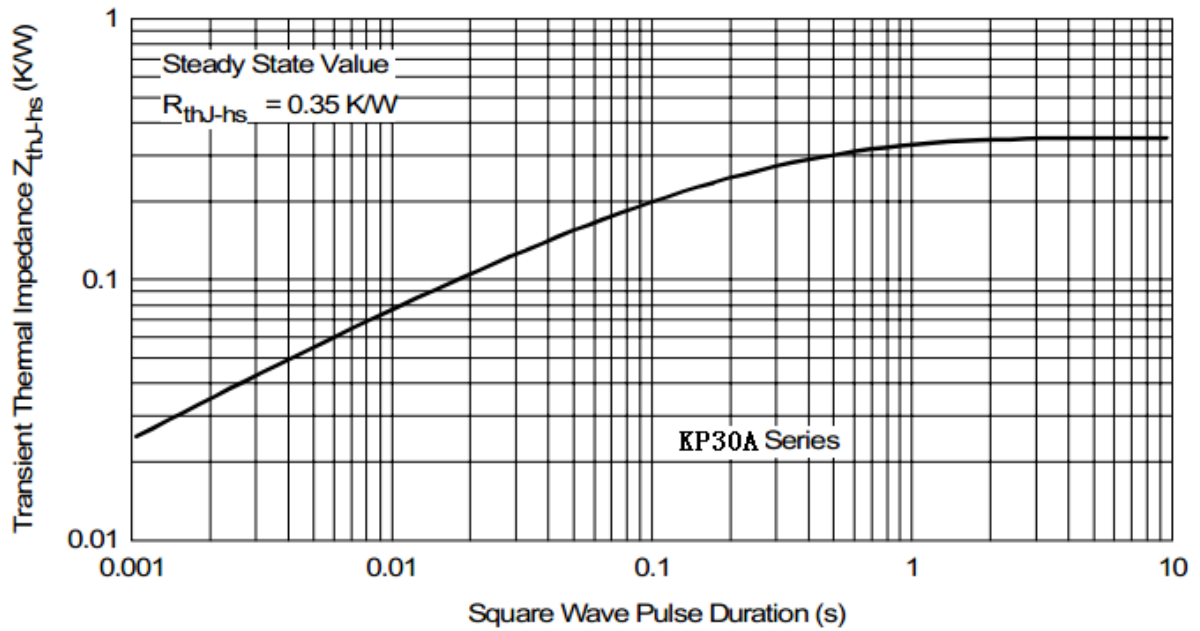

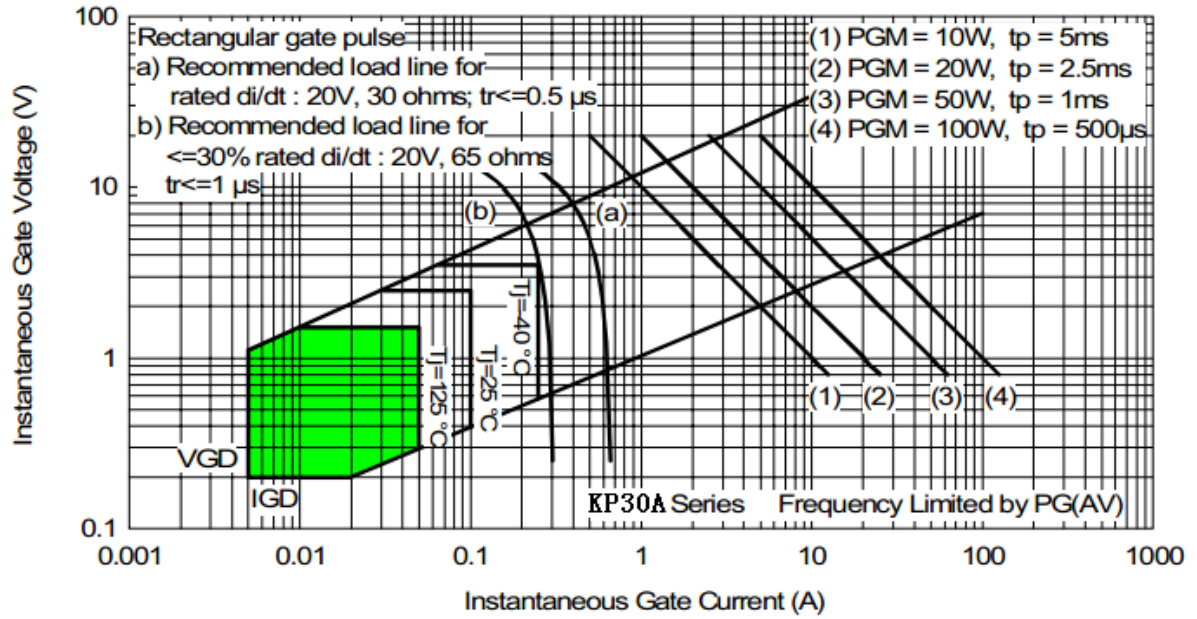Fig. 14 - Forward Voltage Drop Characteristics

Fig. 15 - Thermal Impedance Z_{thJC} Characteristics

Fig. 16 - Gate Characteristics

Outline：