KP3114

High Performance Low Cost Off-line PWM Power Switch

FEATURES

- **Integrated with 700V Power MOSFET and HV Startup Circuit**
- **Integrated rectifier Bridge and Freewheeling Diode**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Flyback, Buck and Buck-Boost Topologies**
- **Support Ultra-low Input Voltage (>20V)**
- **Less than 100mW Standby Power**
- **Up to 30kHz Maximum Frequency**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
    - **Over Load Protection (OLP)**
    - **Cycle-by-Cycle Current Limiting (OCP)**
    - **Abnormal Over Current Protection (AOCP)**
    - **Output OVP**
    - **On-chip OTP**
- **Available with ASOP-7 Package**

APPLICATIONS

- **Small Home Appliances**

GENERAL DESCRIPTION

KP3114 is a high Performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This IC has built-in high break down voltage MOSFET to withstand high surge input.

Unlike conventional PWM control, there's no fixed internal clock in KP3114 to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP3114 integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Abnormal Over Current Protection (AOCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP) with Auto Recovery Mode Protection, etc.
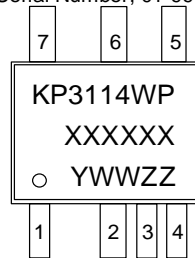
TYPICAL APPLICATION CIRCUIT
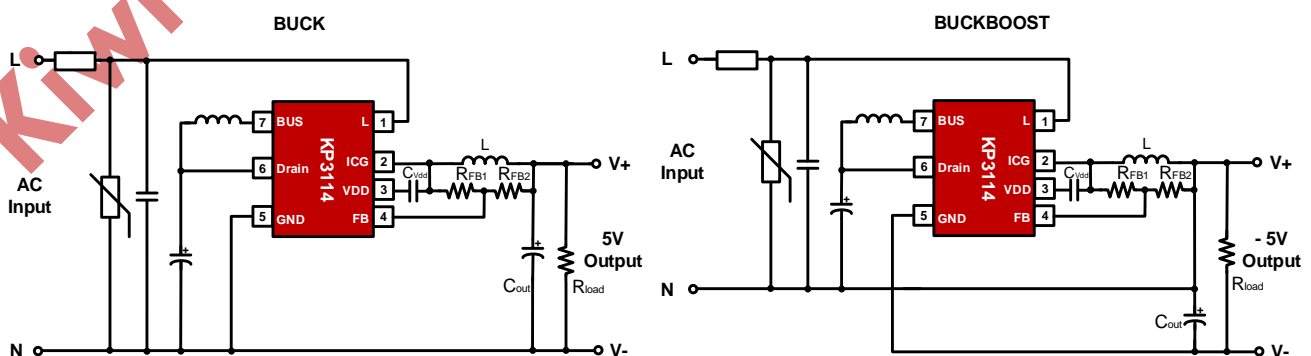
Pin Configuration
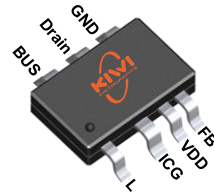
ASOP-7

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ

KP3114WP
XXXXXX
○ YWWZZ

ASOP-7

Typical Output Power Table

Product	Package	Rdson	Output Voltage	Output Current @85-265Vac，BUCK@85℃
KP3114	ASOP-7	20Ω	>2V	Io<250mA

Note:

1. Default for Buck Converter Application

2. The practical output power is determined by the output voltage and thermal condition

Pin Description

Pin Number	Pin Name	I/O	Description
1	L	P	Internal rectifier bridge input
2	ICG	P	Chip Ground
3	VDD	P	Chip power Supply Pin
4	FB	I	Feedback Input Pin
5	GND	P	Circuit Ground
6	Drain	P	Drain of internal high-voltage MOSFET
7	BUS	P	Positive output of internal rectifier bridge

Ordering Information

Part Number	Description
KP3114WPA	ASOP-7, Pb free in T&R, 5000Pcs/Reel

Note: Suffix "A" – Tape & Reel

Block Diagram
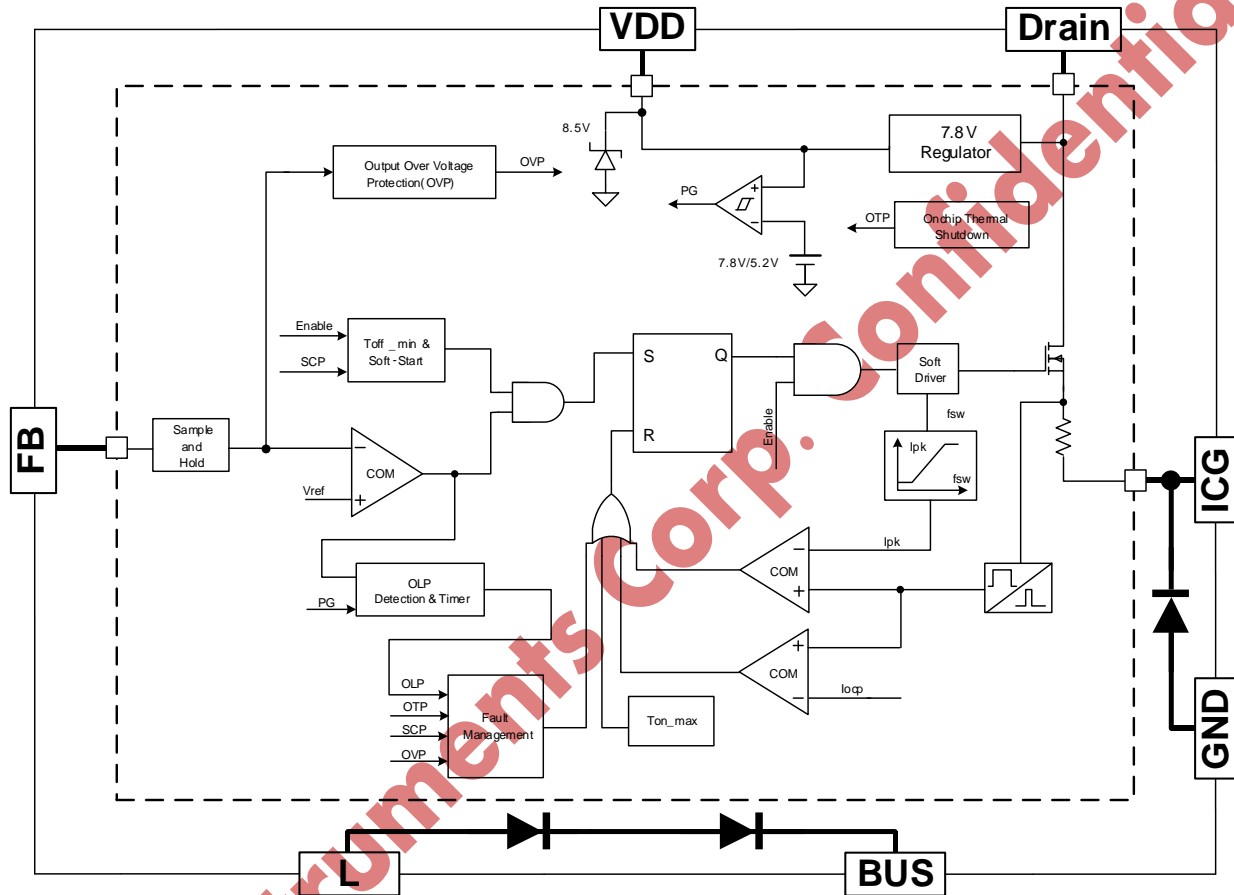
Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
Drain - ICG Voltage Range	-0.3 to 700	V
BUS - L Voltage Range	-1.2 to 1600	V
ICG - GND Voltage Range	-0.6 to 600	V
VDD - ICG Voltage Range	-0.3 to 9	V
VDD Pin Clamp Current	10	mA
FB - ICG Voltage Range (Note 2)	-0.3 to 9	V
Package Thermal Resistance – Junction to Ambient (ASOP-7)	150	°C/W
Maximum Junction Temperature	160	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec)	260	°C
ESD Capability, HBM (Human Body Model)	3000	V
Maximum Internal MOSFET DC Drain Current	0.5	A
Drain Maximum Pulse Current (Tpulse=100μs)	2	A

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C
Operation Switching Frequency	20 to 30	kHz

Electrical Characteristics (Ta = 25°C, If Not Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
High Voltage Startup Section (Drain Pin)						
I_{HV1}	HV Charging Current1	Drain=700V, VDD=0V		0.6		mA
I_{HV2}	HV Charging Current2	Drain=700V, VDD=4V		5		mA
$I_{HV\_leakage}$	HV Leakage Current	Drain=700V, VDD=8.5V		9	20	μA
V_{BR}	HV MOSFET Breakdown Voltage		700			V
R_{dson}	Static Drain-Source On Resistance			20		Ω
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit		7.6	7.8	8	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			5.1		V
V_{CLAMP}	VDD Clamp Voltage	I_{CLAMP}=2mA		8.5		V

I_{VDD_Op}	Operation Current	Fsw=30kHz		240	300	µA
I_{VDD_Q}	Quiescent Current	No Switching		150	190	µA
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.75	1.78	1.81	V
V_{FB_OVP}	Output Over Voltage Protection (Output OVP) Threshold			2.2		V
N_{FB_OVP}	OVP Debounce Cycle			3		
V_{FB_OLP}	Output Over Load Protection (Output OLP) Threshold			1.66		V
T_{D_OLP}	Over Loading Debounce Time			150		ms
Current Sense Section						
T_{LEB}	Leading Edge Blanking Time			380		ns
T_{D_OCP}	Over Current Detection and Control Delay			50		ns
I_{OCP}	Over Current Detection Value			400		mA
I_{AOCP}/I_{OCP}	AOCP/OCP Ratio			1.33		
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF time	Stable state	27	30	33	µs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			2		ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		µs
T_{ON_max}	Maximum ON Time		26	37	48	µs
T_{ss}	Internal Soft Start Time			3		ms
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			500		ms
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown Trigger Point	(Note 3)		155		°C
Freewheeling Diode (ICG-GND)						
Vf	Diode Forward Voltage	ES1J		0.4		V

Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note2. In the range of 50µs pulse width and 5mA pulse current, the negative voltage limit of FB is - 1V

Note3. Guaranteed by design.

Characterization Plots

V_{DD_ON} vs Temperature

V_{DD_OFF} vs Temperature

I_{VDD_Q} (µA) vs Temperature

$T_{OFF\_nom\_max}$ (ms) vs Temperature
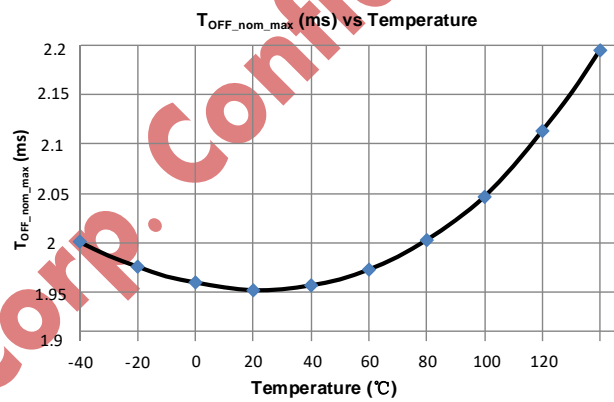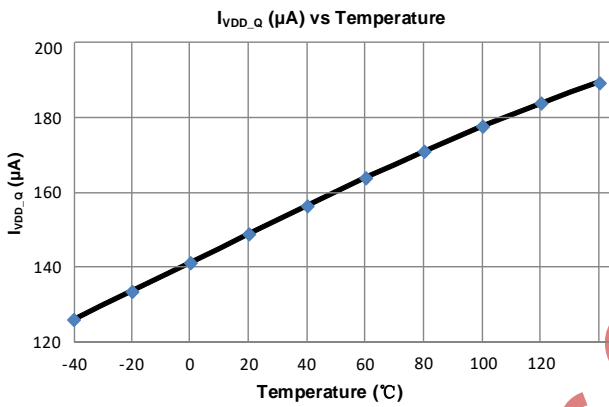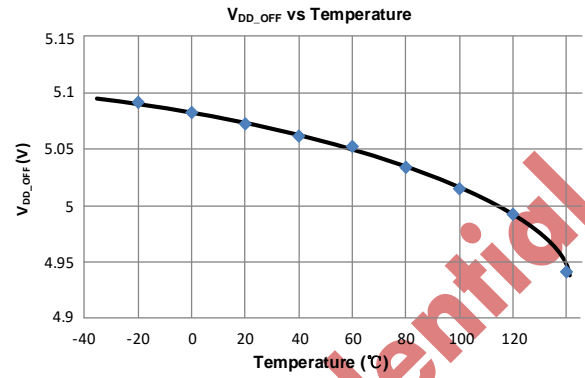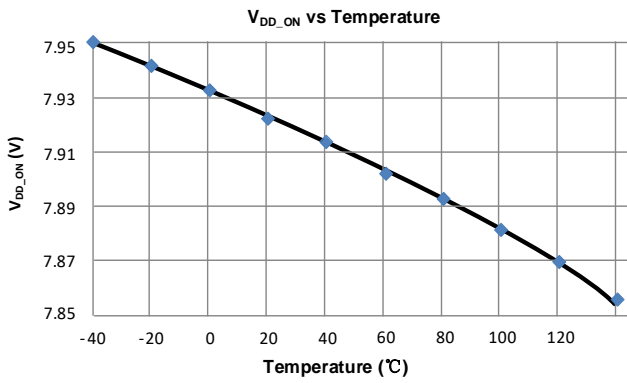
Operation Description

KP3114 integrates a multi-mode PWM controller with high voltage power MOSFET switch on the IC. It is optimized for off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi-mode PWM control to regulate output with high precision and lowest components count.

● **Very Low Operation Current**

The standby operating current in KP3114 is as small as 150µA (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

● **High Voltage Start-Up Operation**

In KP3114, a 700V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in "Block Diagram". When VDD reaches turn-on voltage (7.8V typical), the IC begins switching and the IC current consumed increased to 0.24mA (typical). The VDD is always charged by the high voltage startup cell in steady state.
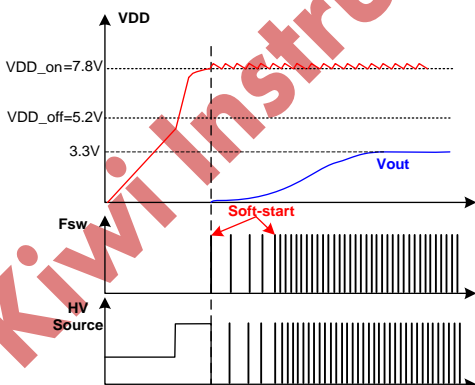

Fig.1

● **Constant Voltage Control**

During the power MOSFET off period, KP3114 samples the FB pin signal which indicates the output voltage, then using the internal Sample & Hold circuit and constant voltage control circuit to guarantee FB pin voltage meet the internal reference V_{FB_REF} (1.78V, typical). So that constant output voltage is achieved.

Below equation approximately determines the output voltage:

$$Vo = 1.78V * \frac{Rup + Rdown}{Rdown} - V_F$$

VF---Freewheeling Diode Voltage. This parameter is offset by the forward current in practical application.

● **Current Limit and Leading Edge Blanking**

There's a programmable current limit for current sensing voltage, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (380ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

● **Multi-Mode PWM Control**

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP3114 which is shown in the Fig 2.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent

regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction.
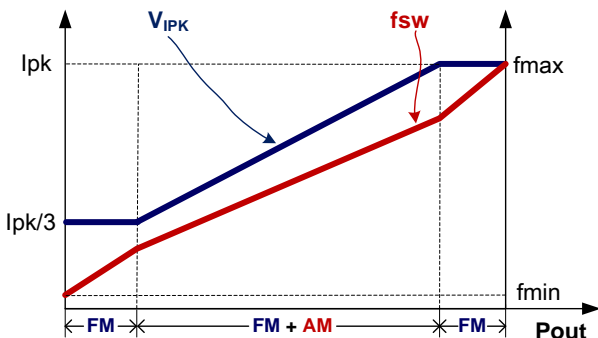

Fig.2

● **Soft Start**

KP3114 features an internal 3ms (typical) soft start that slowly increases the switching frequency (Toff reduce from 100μs to 30μs linearly) during startup sequence. Every restart attempt is followed by the soft start activation.

● **Output Over Voltage Protection (OVP)**

In KP3114, if the sampled FB voltage is larger than 2.2V and lasts for three continuous PWM cycles, the IC will enter into Output Over Voltage Protection (Output OVP) mode, in which auto recovery mode will be followed.

● **Over Load Protection (OLP) / Short Load Protection (SLP)**

If over load or short load condition occurs, the output and the feedback voltage drop down to be lower than V_{FB_OLP}. If this fault is present for more than 150ms (typical), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

● **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To

avoid system components damaged, there's a abnormal over current limit (typically 1.33*OCP). When the current sense voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 60μs.

● **On Chip Thermal Shutdown**

KP3114 integrates thermal shutdown function. When the IC junction temperature is higher than 155°C, IC shuts down and enters into auto-restart mode (as mentioned below).

● **Enhanced Dynamic Response**

In KP3114, the dynamic response performance is optimized to reduce output drop in load transient.

● **Audio Noise Free Operation**

In KP3114, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

● **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 500ms had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

● **Soft Totem-Pole Gate Driver**

KP3114 has a soft totem-pole gate driver with optimized EMI performance.

Application Information
● **PCB Layout Guidelines**

PCB layout design has a significant impaction on the performance of power supply，which helps

KP3114 to improve system reliability, EMC and thermal performance. Follow below guidelines to optimize performance.

1. The main power loop (Loop1&Loop2) should be as small as possible, and the trace should be wide for better efficiency performance.

2. Feedback Routing (Loop3): a) Put the feedback loop out of the main power loop，and minimize this loop area as small as possible; b) Do not route FB pin line too long and beneath the IC, or system may not operation normally; c) Put the components of this loop close to IC as much as possible, and far away from the power inductor; d) Place the output feedback point at the positive of the output capacitor, and do not route this line beneath the power inductor or freewheeling diode in case high-frequency noise coupled; e) Make sure signal ground of FB line and IC are connected firstly, then connect to power ground of inductor through a single point.

Place VDD capacitor close to the IC to ensure the VDD loop is small.

3. Additional Notes: a) When π filter circuit is added after the bridge, make sure power inductor far away from the π filter inductor; b) Connect the drain pin of KP3114 to a large cooper area to improve thermal performance if possible.

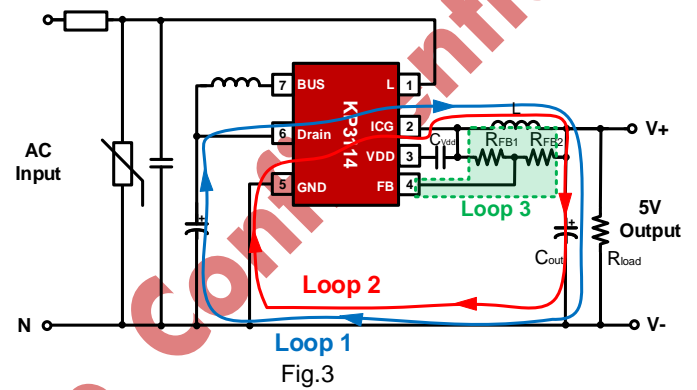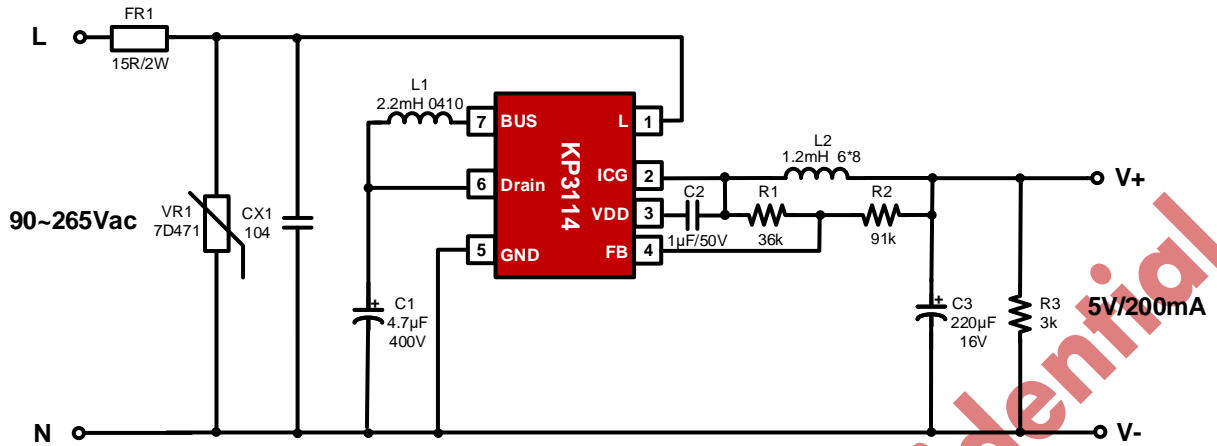Fig.3

Typical Application Diagram
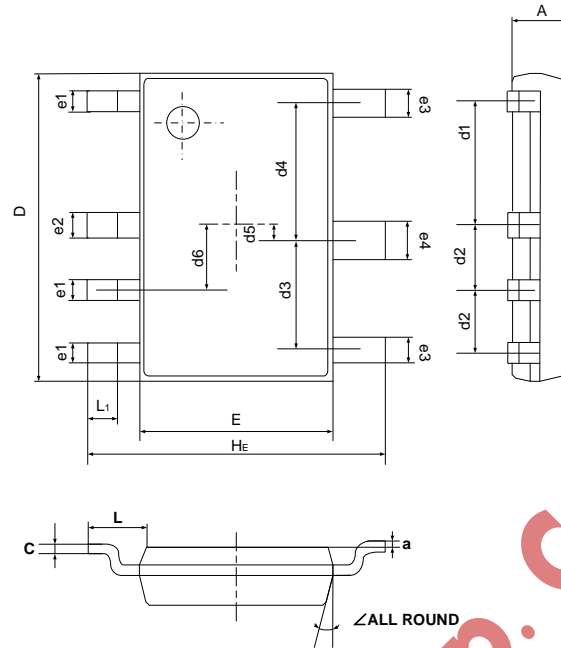

Fig.4 Typical Application Circuit

Package Dimension

ASOP-7

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.05	1.25	0.041	0.049
C	0.15	0.22	0.006	0.009
D	6.1	6.3	0.240	0.248
E	3.8	4.0	0.149	0.157
H$_E$	5.9	6.1	0.232	0.240
d1	2.41	2.61	0.094	0.103
d2	1.23	1.43	0.048	0.056
d3	2.08	2.28	0.081	0.090
d4	2.58	2.78	0.101	0.109
d5	0.25		0.010	
d6	1.28		0.050	
e1	0.3	0.5	0.012	0.020
e2	0.41	0.61	0.016	0.024
e3	0.45	0.65	0.017	0.025
e4	0.7	0.9	0.027	0.035
L	0.95	1.15	0.037	0.045
L1	0.5	1.0	0.019	0.039
a	0.2 (ref.)		0.008 (ref.)	
∠	12°			

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