KP311AWPA

High Performance Low Cost Off-line PWM Power Switch

FEATURES

- **Integrated with Rectifier diode, Freewheeling diode, Feedback diode**
- **Integrated with 500V MOSFET and High Voltage Startup Circuit**
- **High Precision 5V Default Output**
- **No External Rsense needed, Low BOM Cost**
- **Support Ultra-low Input Voltage (>12V)**
- **Support Buck Topology**
- **On/OFF Peak Current Mode Control**
- **Less than 50mW Standby Power**
- **Built-in 31KHz Oscillator with Frequency Shuffling**
- **Built-in Soft Start**
- **Very Low VDD Operation Current**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Abnormal Over Current Protection (AOCP)**
  - **Leading Edge Blanking (LEB)**
  - **VDD UVLO**
- **ASOP-7 Package Available**

APPLICATIONS

- **Small Home Appliance**
- **Linear Regulator / RCC Replacement**

GENERAL DESCRIPTION

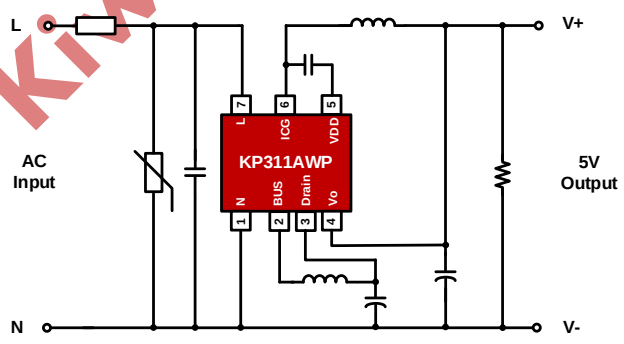
KP311AWP is a low cost, highly integrated PWM power switch for non-isolated buck applications.

KP311AWP combines a 500V power MOSFET with the ON/OFF PWM controller in one chip. The IC can achieve high precision 5V default Output at universal AC input. In KP311AWP, Toff_min is set to 32μs with frequency shuffling. The IC has built-in green mode control for light and zero loadings, which can achieve less than 50mW standby power.

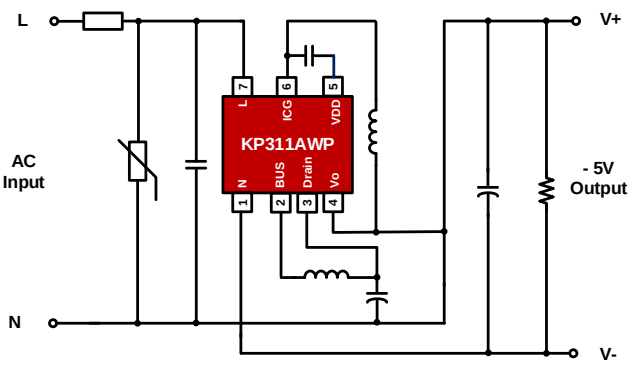
KP311AWP integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), On-chip Thermal Shutdown (OTP), Abnormal Over Current Protection (AOCP), Over Load Protection (OLP) Short Load Protection (SLP), etc.

TYPICAL APPLICATION CIRCUIT

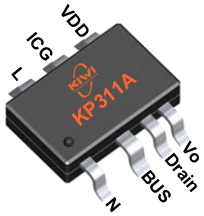
BUCK



BUCKBOOST



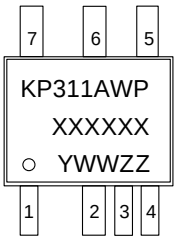
Pin Configuration



ASOP-7

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ



ASOP-7

Typical Output Power Table

Package	Maximum Load Current @ 85-265 Vac,5V
ASOP-7	100mA

Note:

1. Default 5V Buck output
2. The practical output power is determined by the output voltage and thermal condition

Pin Description

Pin Number	Pin Name	I / O	Description
1	N	P	AC input, also used as circuit ground
2	BUS	P	Positive output of internal half-bridge rectifier bridge
3	Drain	P	Internal power MOSFET drain
4	Vo	I	Sampling the output voltage as an internal feedback signal
5	VDD	I	Power Supply Pin of the Chip,
6	ICG	I	The Ground of the IC.
7	L	P	AC input, also used as half-bridge rectifier bridge input

Ordering Information

Part Number	Description
KP311AWPA	ASOP-7, Pb free in T&R, 5000 Pcs/Reel

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD – GND Voltage Range	-0.3 to 7	V
Drain – GND Voltage Range	-0.3 to 500	V
Package Thermal Resistance (ASOP-7)	150	°C / W
Maximum Junction Temperature	160	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	7.5	kV
Internal MOSFET Pulse drain current(Continues 100μs)	1	A

Recommended Operation Conditions

Parameter	Value	Unit
Operating Junction Temperature	-40 to 125	°C

Electrical Characteristics (Ta = 25℃, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section (VDD Pin)						
$I_{VDD\_standby}$	Standby Operation Current	VDD=6V		150	300	μA
V_{DD_Op}	VDD Operation Voltage	@ Full Load	5.34	5.46	5.58	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			4.38		V
V_{DD_ON}	VDD Under Voltage Lockout Exit			4.87		V
V_{out_Reg}	System Output Regulation Voltage		4.95	5	5.075	V
Oscillator Section						
Toff_min	Minimum Turn Off Time	VDD=5.46V	29	32	35	μs
Δ Toff /Toff	Frequency Shuffling Range		-5		5	%
Ton_max	Maximum Turn On Time	(Note 2)	45	50	55	μs
T_{D_OLP}	Over Loading Debounce Time	VDD=4.9V		128		ms
Internal Current Sense Input Section						
T_{LEB}	CS Input Leading Edge Blanking Time		300	400	500	ns

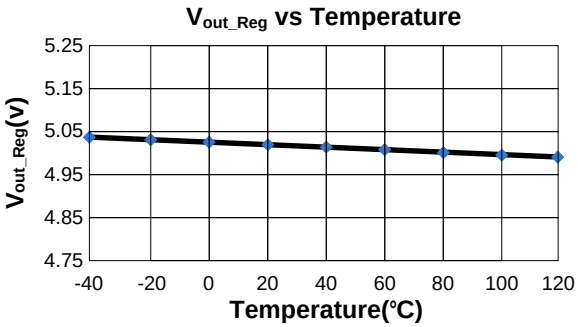
I_{peak_limit}	Peak Current Limit		200	210	220	mA
I_{peak_AOCP}	AOCP Current Limit			250		mA
T_{D_OCP}	Over Current Detection and Control Delay			200		ns
Over Temperature Protection						
T_{SD}	Thermal Shutdown Trigger Point	(Note 2)		155		℃
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		500			V
R_{dson}	Static Drain-Source On Resistance	I (Drain)=50mA		25		Ω
$I_{Drain\_to\_VDD}$	High Voltage VDD Charging Current Source	Drain=500V, VDD=0V		1	3	mA
$I_{Drain\_leakage}$	Drain Leakage Current	HV=500V, VDD=6V			50	μA
V_{Drain_on}	HV-Startup Voltage		7	8	9	V

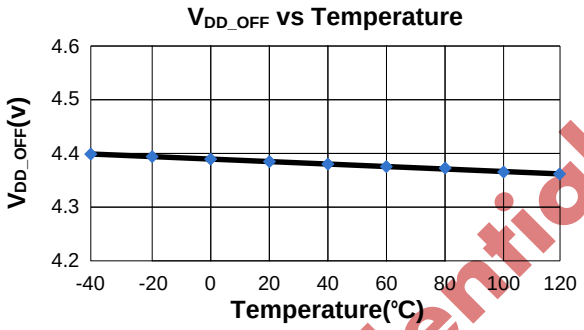
Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

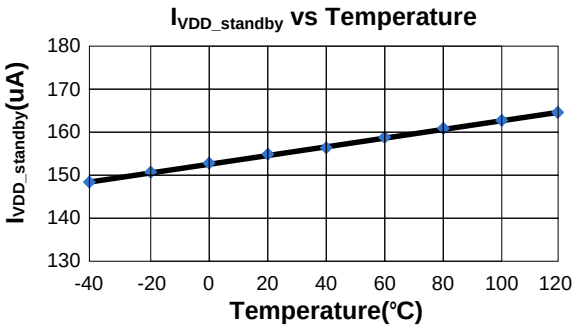
Note 2. Guaranteed by design.

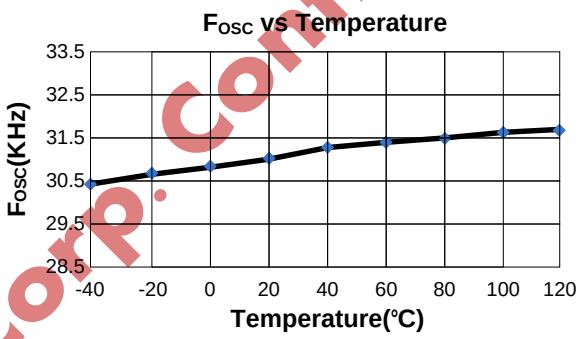
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Characterization Plots









Operation Description

KP311AWP combines a high voltage power MOSFET switch with power controller in one chip. It is optimized for off-line non-isolated buck or applications for small home appliances and linear regulator replacement. The IC utilizes the ON/OFF current mode PWM control to regulate a 5V default output with high precision and lowest components count. Additionally, KP311AWP supports ultra-low input voltage (>12V) under normal load.

● Very Low Operation Current

The standby operating current in KP311AWP is as small as 150μA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement. Normally 0.1-1μF ceramic capacitor is recommended.

● Oscillator with Frequency Shuffling

Minimum Toff Time in KP311AWP is fixed to 32μs. To improve system EMI performance, KP311AWP operates the system with ± 5% frequency shuffling around setting frequency. The practical system switching frequency is determined by the load condition and the comparison of VDD voltage over output reference, which cause system works in the pulse-skipping mode.

● Current Limit and Leading Edge Blanking

The current limit circuit samples the differential voltage on the internal current sense resistor, as shown in “Block Diagram”. When the sampled differential voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (400ns, typical), the cycle-by-cycle current limiting KP311AWP integrates thermal shutdown function. When the IC temperature is over 155 °C, the IC comparator is disabled and cannot switch off the GATE driver.

● Green Mode Operation

In light/zero load condition, the system usually works in DCM mode. Therefore, the main power dissipation is proportional to the square of peak current limit. In KP311AWP, the IC can automatically reduce the peak current limit under such load conditions, thus less than 50mW standby power can be achieved.

● Soft Start

KP311AWP features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. Every restart attempt is followed by the soft start activation.

● Over Load Protection (OLP) / Short Load Protection (SLP)

If over load or short load occurs, a fault is detected. If this fault is present for more than 128ms (typical), the protection will be triggered, the IC will experience an auto-restart mode protection as mentioned below.

● Abnormal Over Current Protection (AOCP)

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there’s a abnormal over current limit (typically 250mA). When the current sense voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 2 cycles.

● On Chip Thermal Shutdown (OTP)

shuts down and enters into auto-restart mode as mentioned below.

Protections with Auto-Restart

In the event of OTP or OLP, the IC enters into auto-restart and VDD oscillation mode begins, wherein the power MOSFET is disabled. In VDD oscillation mode, the VDD hold-up capacitor voltage will periodically ramp up and down between 4.87V and 4.38V with a digital counter counting the oscillation cycle. When 511 cycles had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

Soft Totem-Pole Gate Driver

KP311AWP has a soft totem-pole gate driver with optimized EMI performance.

Typical Reference Design

● Inductor Calculation

In order to ensure stable system operation, KP311AWP is recommended to work under light CCM condtion, which means inductor current ripple ΔI is close to Max CS-PK (210mA). Detail calculation shows below:

$$L=(Vo+Vf)*Toff\_min/\Delta I$$

Vo：Output Voltage;

Vf：Forward voltage on freewheeling diode；

Toff_min：Internal Toff-min, ~32μs；

ΔI：inductor current ripple,2* (Iocp-Io_max) under CCM condition.

For example, take 5V-100mA as the output spec, Io_max is set to 1.2 times of the normal output current (120mA);

L=(5V+0.7V)*32μs / (210-120)mA/2=1.01mH.

Choose L=1mH & Isaturation>210mA as the specific inductor parameter demand.

● Output Capacitor and Dummy Load Selection

Output Capacitor Selection: for 5V-100mA application, Output capacitor is choose between 100μF-220μF according to actual output voltage ripple.

Dummy Load Selection: heavy dummy load could suppress the output voltage from floating up, but too heavy dummy load would enlarge the standby power loss; take balance among load regulation and standby power loss.

1k-2k dummy load is recommended in KP311AWP system for good output regulation and low dummy load power loss (10-15mW).

● PCB Layout Guide

Good PCB layout is very important to KP311AWP's operation, which helps to improve system reliability, EMC and thermal performance. Follow below guidelines to optimize performance.

(1) Power Loop Routing：

As shown in fig.1, minimize the power loop area of ① and ② as small as possible. Power loop ① is formed by input capacitor – IC – inductor – output capacitor. Power loop ② is formed by inductor – output capacitor – freewheeling diode (Integrated in IC). Make sure these two loop area reduce to its minimum.

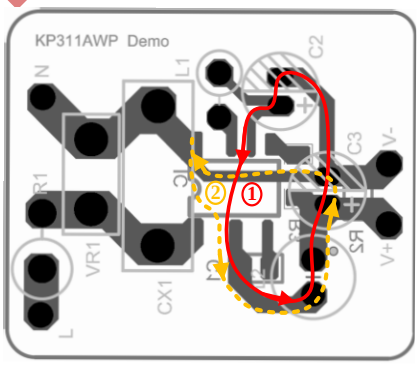


Fig.1

(2) EMC Layout：

a) In order to improve the EMC of KP311AWP, it is recommended to add X-cap on the input ;b) When π filter circuit is added after the bridge(Integrated in IC), make sure power inductor far away from the π filter inductor; c) It is recommended to properly increase the inductance of the filter inductance, cooperate with the pre-stage fuse resistor and varistor to ensure the IC's ability to resist surge.

Typical Application Diagram

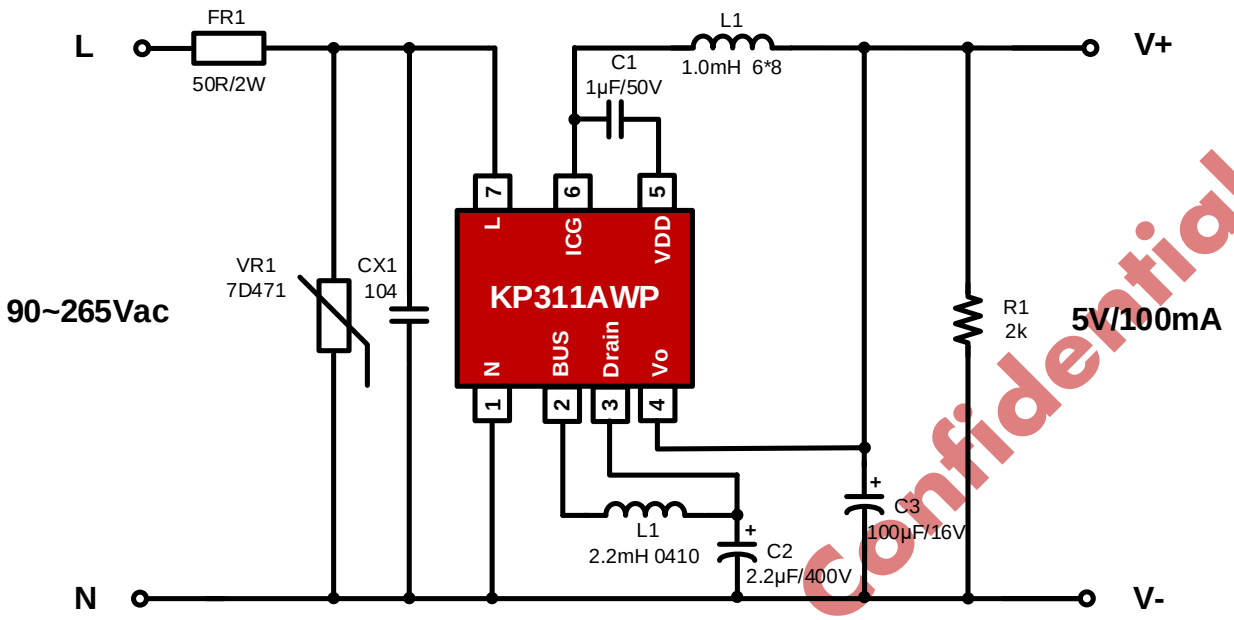
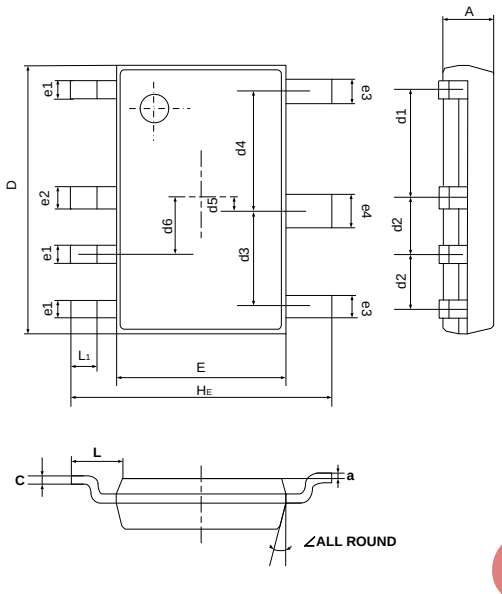


Fig.2

Package Dimension

ASOP-7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.05	1.25	0.041	0.049
C	0.15	0.22	0.006	0.009
D	6.1	6.3	0.240	0.248
E	3.8	4.0	0.149	0.157
H_E	5.9	6.1	0.232	0.240
d1	2.41	2.61	0.094	0.103
d2	1.23	1.43	0.048	0.056
d3	2.08	2.28	0.081	0.090
d4	2.58	2.78	0.101	0.109
d5	0.25		0.010	
d6	1.28		0.050	
e1	0.3	0.5	0.012	0.020
e2	0.41	0.61	0.016	0.024
e3	0.45	0.65	0.017	0.025
e4	0.7	0.9	0.027	0.035
L	0.95	1.15	0.037	0.045
L1	0.5	1.0	0.019	0.039
a	0.2(ref.)		0.008(ref.)	
∠	12°			

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