High Performance Low Cost Off-line PWM Power Switch

FEATURES

- **Integrated with 650V Power MOSFET and HV Startup Circuit**
- **Multi-Mode Control with Audio Noise Free Operation**
- **Supports Buck and Buck-Boost Topologies**
- **Default 12V Output with FB floated**
- **Less than 50mW Standby Power**
- **Green Mode Operation for High Efficiency**
- **Good Line and Load Regulation**
- **Built-in Soft Start**
- **Build in Protections:**
  - **Over Load Protection (OLP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **Output OVP**
  - **VDD OVP, UVLO & Clamp**
- **Available with SOP-8 and DIP-8 Package**

APPLICATIONS

- **Small Home Appliance**
- **Industry Controls**

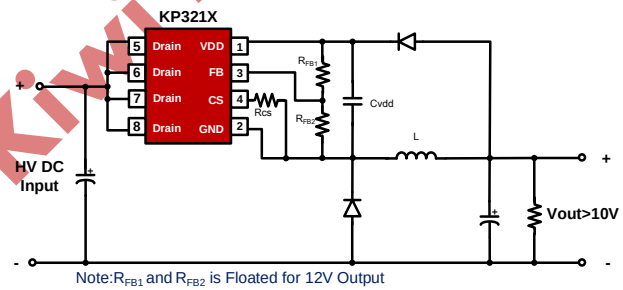
GENERAL DESCRIPTION

KP321X family is a high performance Switch Mode Power Supply Switcher for low power off-line application with minimum components in typical buck solution. This family has built-in high break down voltage MOSFET to withstand high surge input.

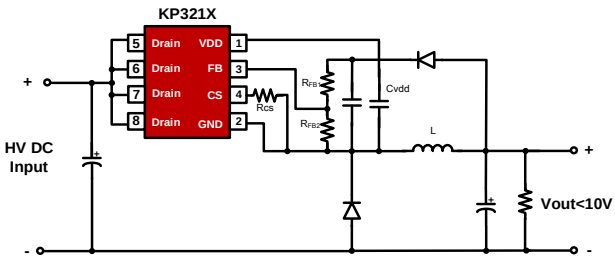
Unlike conventional PWM control, there's no fixed internal clock in KP321X family to trigger the GATE driver, the switching frequency is changed according to the load condition. The multi-mode PWM control is integrated to simplify circuit design and achieve good line and load regulation without audio noise generated. The peak current limit changes according to the real load condition for low standby power in no load.

KP321X integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Output OVP, On-chip Thermal Shutdown, Over Load Protection (OLP), VDD OVP with Auto Recovery Mode Protection, etc.

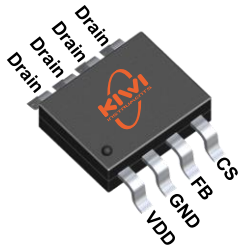
TYPICAL APPLICATION CIRCUIT



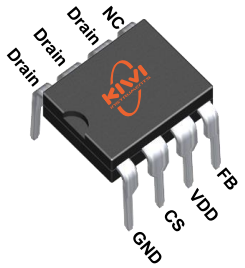
Note:R_{FB1} and R_{FB2} is Floated for 12V Output



Pin Configuration



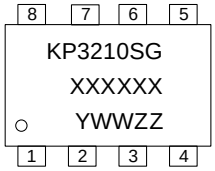
SOP-8



DIP-8

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ：Serial Number,01-99 or A0-ZZ



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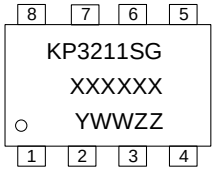

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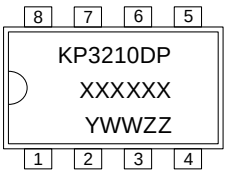

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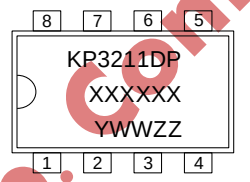

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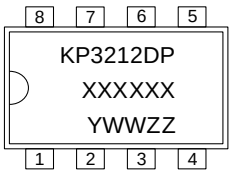


DIP-8

Typical Output Power Table(1)

Product	Package	R_{dson}	Vo	Load Current@85-265Vac, BUCK
KP3210	SOP-8	9.5Ω	>2V	200mA<Io<400mA
	DIP-8			
KP3211	SOP-8	4Ω	>2V	350mA<Io<700mA
	DIP-8			
KP3212	DIP-8	2.1Ω	>2V	650mA<Io<900mA

(1) Default for Buck Converter Application. The practical output power is determined by the output voltage and thermal condition.

Pin Description

SOP-8	DIP-8	Pin Name	I/O(2)	Description
1	3	VDD	P	The power supply and the output voltage feedback pin. For the normal operation, a capacitor with 1μF is recommended to connect to this pin
2	1	GND	G	The ground reference for the IC
3	4	FB	I	Feedback Input. Left open for default 12V output
4	2	CS	I	Current Sensing Input
5, 6, 7, 8	6,7,8	Drain	P	The Power MOSFET Drain
/	5	NC	-	No Function Pin and Left Floating in Application

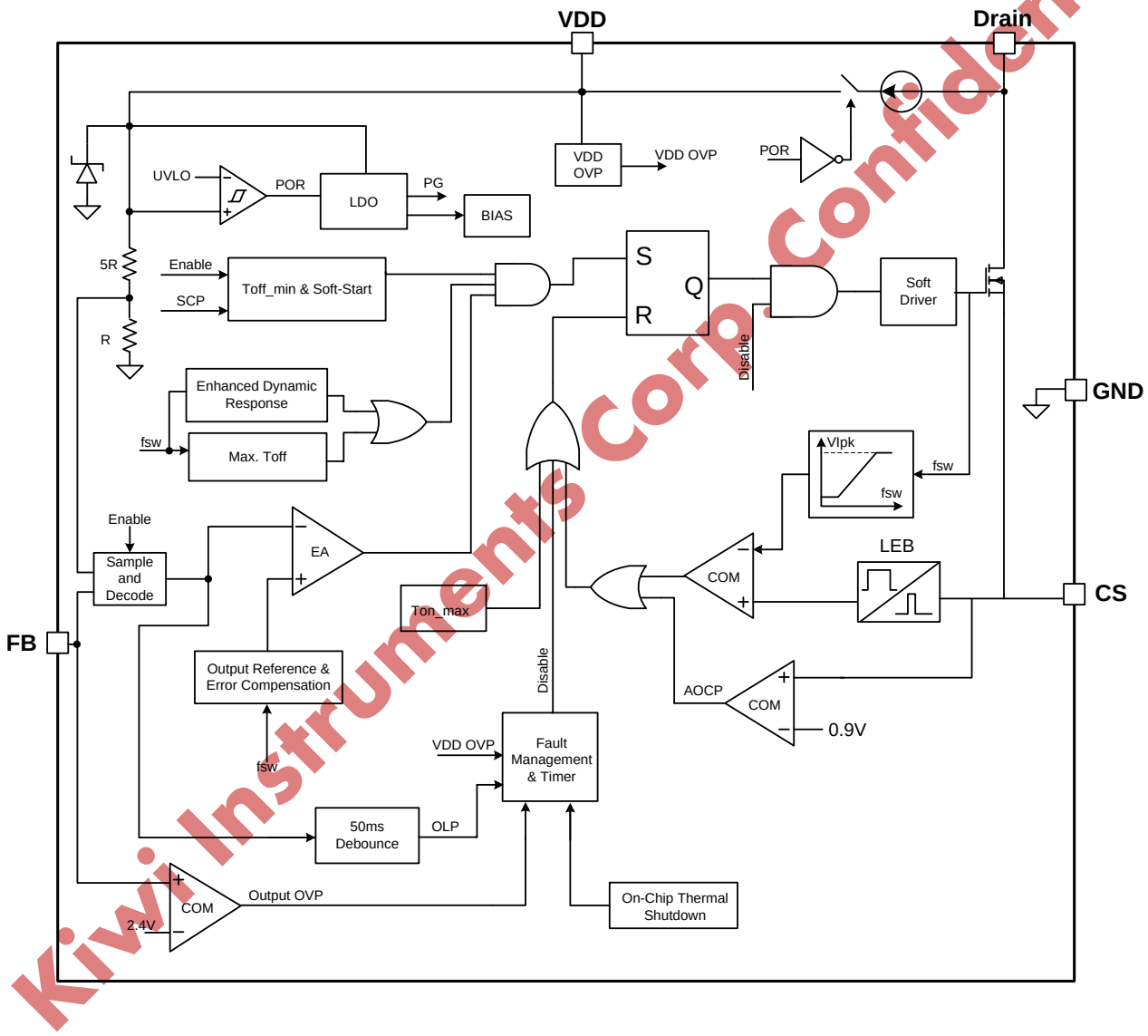
(2) I – Input, O – Output, P - Power, G – Ground.

Ordering Information

Part Number (3)	Description
KP3210SGA, KP3211SGA	SOP-8, Halogen free in T&R, 4000Pcs/Reel
KP3210DP, KP3211DP, KP3212DP	DIP-8, Halogen free, 50Pcs/Tube

(3) Suffix "A" - Tape&Reel.

Block Diagram



Absolute Maximum Ratings (4)

Parameter		Value	Unit
Drain - GND Voltage Range		-0.3 to 650	V
VDD - GND Voltage Range		-0.3 to 30	V
VDD Pin Clamp Current		10	mA
FB, CS - GND Voltage Range		-0.3 to 7	V
Package Thermal Resistance – Junction to Ambient (SOP-8)		165	˚C/W
Package Thermal Resistance – Junction to Ambient (DIP-8)		105	˚C/W
Maximum Junction Temperature		150	˚C
Storage Temperature Range		-65 to 150	˚C
Lead Temperature (Soldering, 10sec.)		260	˚C
ESD Capability, HBM (Human Body Model) (5)		3	kV
Maximum Internal MOSFET DC Drain Current	KP3210	1	A
	KP3211	2	A
	KP3212	4	A
Maximum Internal MOSFET Pulse Drain Current (Continues 100μs)	KP3210	4	A
	KP3211	8	A
	KP3212	16	A

(4) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(5) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Operation Junction Temperature	-40 to 125	˚C
Operation Switching Frequency	40 to 60	kHz

Electrical Characteristics (Ta = 25˚C, If Not Otherwise Noted)

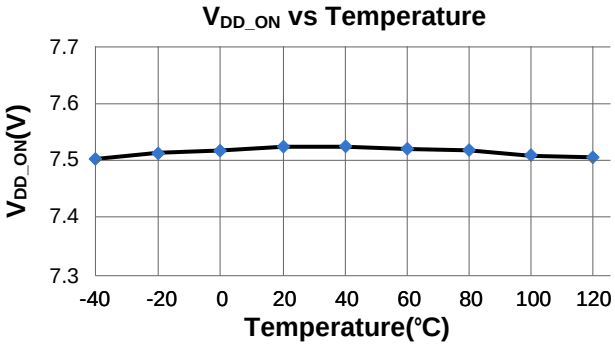
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High Voltage Startup Section (HV Pin)						
I_{HV}	HV Charging Current	Drain=650V, VDD=0V	1	2		mA
$I_{HV\_leakage}$	HV Leakage Current	Drain=650V, VDD=12V			10	μA

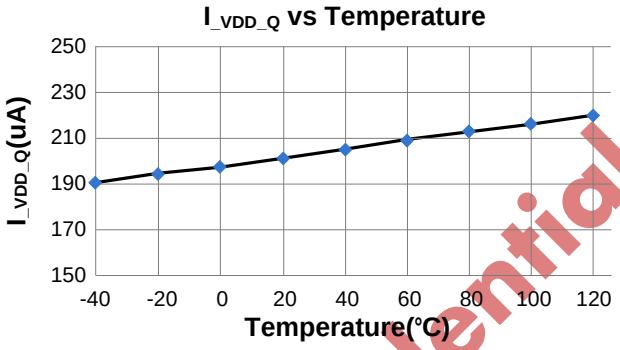
Supply Voltage Section (VDD Pin)						
V_{DD_ON}	VDD Under Voltage Lockout Exit		6.4	7.5	8.6	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		6.1	7.0	8.1	V
V_{DD_Reg1}	VDD Regulation Voltage	FB is floating	12.4	12.6	12.8	V
I_{VDD_st}	Start-up Current	No switching		100	300	μA
I_{VDD_Op}	Operation Current	Fsw=60kHz		800		μA
I_{VDD_Q}	Quiescent Current			200		μA
V_{DD_OVP}	VDD OVP Threshold			28		V
V_{DD_Clamp}	VDD Clamp Votage	IVDD=10mA		30		V
Feedback Section (FB Pin)						
V_{FB_REF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_OVP}	Output Over Voltage Protection (Output OVP) Threshold			2.4		V
V_{FB_OLP}	Output Over Load Protection (Output OLP) Threshold			1.7		V
T_{D_OLP}	Over Loading Debounce Time			50		ms
Current Sense Input Section (CS Pin)						
T_{LEB}	Leading Edge Blanking Time			350		ns
T_{D_OCP}	Over Current Detection and Control Delay			100		ns
V_{IPK}	Normal Peak Current Limit		0.50	0.55	0.60	V
V_{AOCP}	Abnormal Over Current Protection Threshold			0.9		V
Timer Section						
$T_{OFF\_min\_norm}$	Normal Minimum OFF time		14.5	16	17.5	μs
$T_{OFF\_max\_nom}$	Nominal Maximum OFF Time			1.4		ms
$T_{OFF\_max\_FDR}$	Maximum OFF Time in Fast Dynamic Response Mode			420		μs
T_{ON_max}	Maximum ON Time			12		μs
T_{ss}	Internal Soft Start Time			3		ms
$T_{Auto\_Recovery}$	Protection Auto Recovery Debounce Time			500		ms
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown Trigger Point (6)			150		˚C

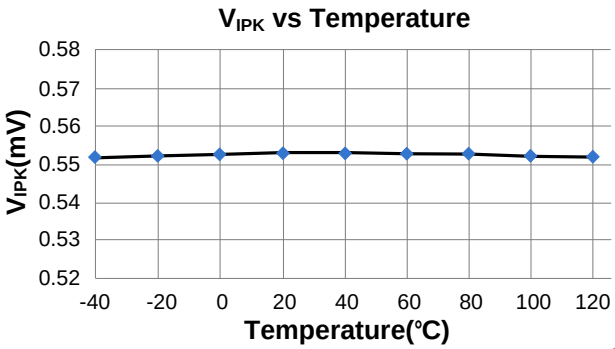
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
R_{dson}	Static Drain-Source on Resistance	KP3210		9.5		Ω
		KP3211		4		Ω
		KP3212		2.1		Ω

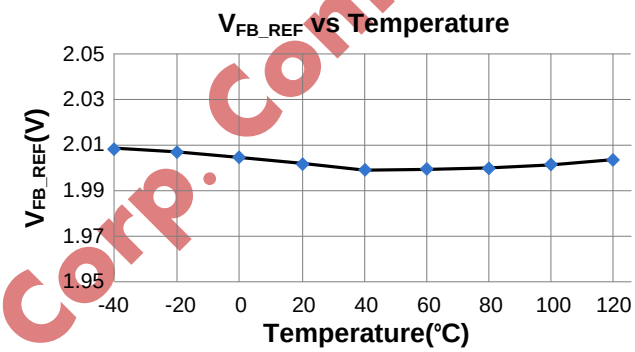
(6) Guaranteed by design.

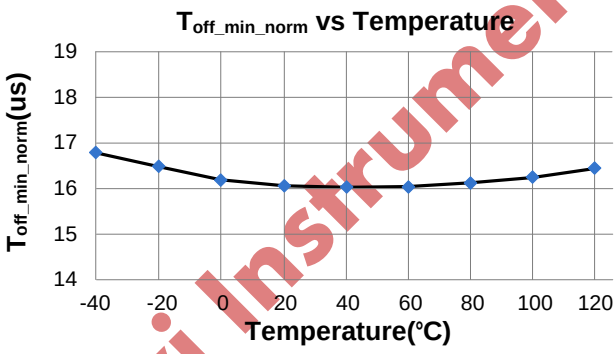
Characterization Plots











Operation Description

KP321X family integrates a high voltage power MOSFET switch and a multi mode PWM controller. It is optimized for off-line non-isolated buck or buck-boost applications in small home appliances and linear regulator replacement. The IC utilizes the multi mode PWM control to regulate output with high precision and lowest components count.

• Very Low Operation Current

The standby operating current in KP321X is as small as 200μA (typical). The small operating current results in higher efficiency and reduces the VCC hold-up capacitance requirement.

• High Voltage Start-Up Operation with Less than 50mW Standby Power

In KP321X, a 650V high voltage startup cell is integrated. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cvdd through Drain pin, as shown in “Block Diagram”. When VDD reaches UVLO turn-on voltage (7.5V typical), the IC begins switching and the IC current consumed increased to 0.8mA (typical). The VDD is charged by the output through the feedback diode in steady state, which result in less than 50mW standby power with the combination of high voltage startup cell.

• Current Limit and Leading Edge Blanking

There’s a programmable current limit for current sensing voltage from CS Pin, which is changed according to the system switching frequency. When the sampled voltage exceeds the internal threshold, the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (300ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

• Multi Mode PWM Control

To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP321X which is shown in the Fig 1.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 50mW.

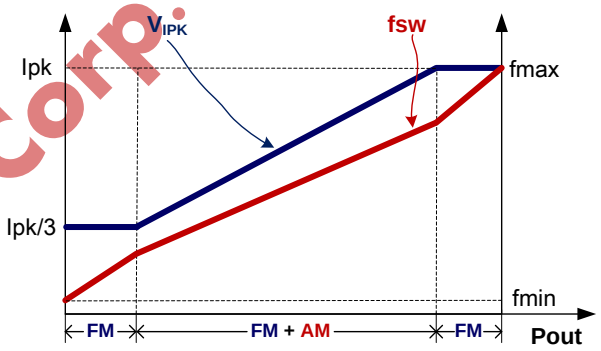


Fig.1

• Constant Voltage Control

During the power MOSFET off period, KP321X samples the FB pin signal which indicates the output voltage, then using the internal Sample & Hold circuit and constant voltage control circuit to guarantee FB pin voltage meet the internal reference V_{FB_REF} (typically 2.0V). So that constant output voltage is achieved.

Below equation approximately determines the output voltage:

$$Vo = 2.0V * \frac{Rup + Rdown}{Rdown}$$

Since the sampling of FB is affected by the isolation diode, it is necessary to adjust the FB voltage dividing resistance in practical application.

- **Soft Start**

KP321X features an internal 4ms (typical) soft start that slowly increases the switching frequency during startup sequence. Every restart attempt is followed by the soft start activation.

- **Output Over Voltage Protection (OVP)**

In KP321X, if the sampled FB voltage is larger than 2.4V and lasts for three continuous PWM cycles, the IC will enter into Output Over Voltage Protection (Output OVP) mode, in which auto recovery mode will be followed.

- **Over Load Protection (OLP) / Short Load Protection (SLP)**

If over load or short load condition occurs, the output and the feedback voltage drop down to be lower than V_{FB_OLP}. If this fault is present for more than 50ms (typical), the protection will be triggered, the IC will experience an auto-restart mode (as mentioned below).

- **Abnormal Over Current Protection (AOCP)**

When in heavy load or output short condition, the inductor current may be increased too large. To avoid system components damaged, there's a abnormal over current limit (typically 0.9V) for CS Pin. When the CS voltage is larger than this threshold, the internal power MOSFET is turned off immediately and is to be turned on again after 128μs.

- **On Chip Thermal Shutdown**

KP321X integrates thermal shutdown function. When the IC junction temperature is higher than 150 °C, IC shuts down and enters into auto-restart mode (as mentioned below).

- **Enhanced Dynamic Response**

In KP321X, the dynamic response performance is optimized to reduce output drop in load transient.

- **Audio Noise Free Operation**

In KP321X, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage higher than V_{DD_OVP}(typically 28V), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (typically 7V) and then the system will restart up again. An internal 30V (typical) zener clamp is integrated to prevent the IC from damage.

- **Protections with Auto-Restart**

In the event of protections, the IC enters into auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 500ms had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process.

- **Soft Totem-Pole Gate Driver**

KP321X has a soft totem-pole gate driver with optimized EMI performance.

- **PCB Layout Guide**

Good PCB layout is very important to KP321X's operation, which helps to improve system reliability, EMI and thermal performance. Follow below guidelines to optimize performance.

(1) Power Loop Routing:

As shown in fig.2, minimize the power loop area of

① and ② as small as possible. Power loop ① is formed by input capacitor – IC – inductor – output capacitor. Power loop ② is formed by inductor – output capacitor – freewheeling diode. Make sure these two loop area reduce to its minimum.

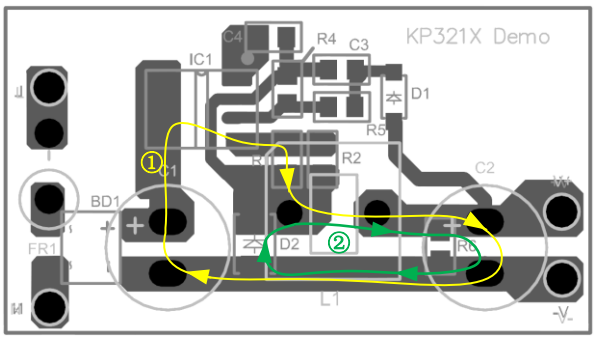


Fig.2

(2) Feedback Routing:

As shown in fig.3, the feedback loop ③ is formed by inductor – feedback diode – FB divided resistor//FB capacitor – IC. This loop is most important to system operation. Make sure these guidelines below been checked when layout: a) Put the feedback loop out of the main power loop ① and ②，and minimize this loop area as small as possible; b) Do not route FB pin line too long, and do not route this line beneath the IC, or system may not operation normally;

c) Put the components (FB divided resistor and FB capacitor) of this loop close to IC as much as possible, and far away from the power inductor; d) Place the output feedback point at the positive of the output capacitor, and do not route this line beneath the power inductor or freewheeling diode in case high-frequency noise coupled; e) Make sure signal ground of FB line and IC are connected first, then connect to power ground of inductor through a single point.

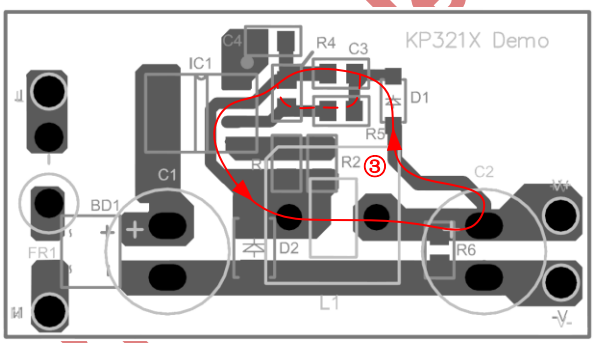


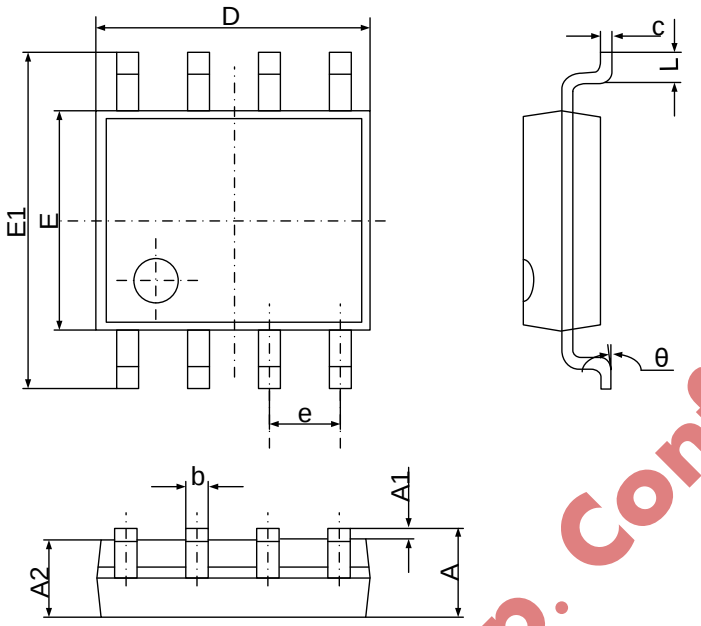
Fig.3

(3) Additional Notes:

a) When π filter circuit is added after the bridge, make sure power inductor far away from the π filter inductor; b) Connect the drain pin of KP321X to a large cooper area to improve thermal performance if possible.

Package Dimension

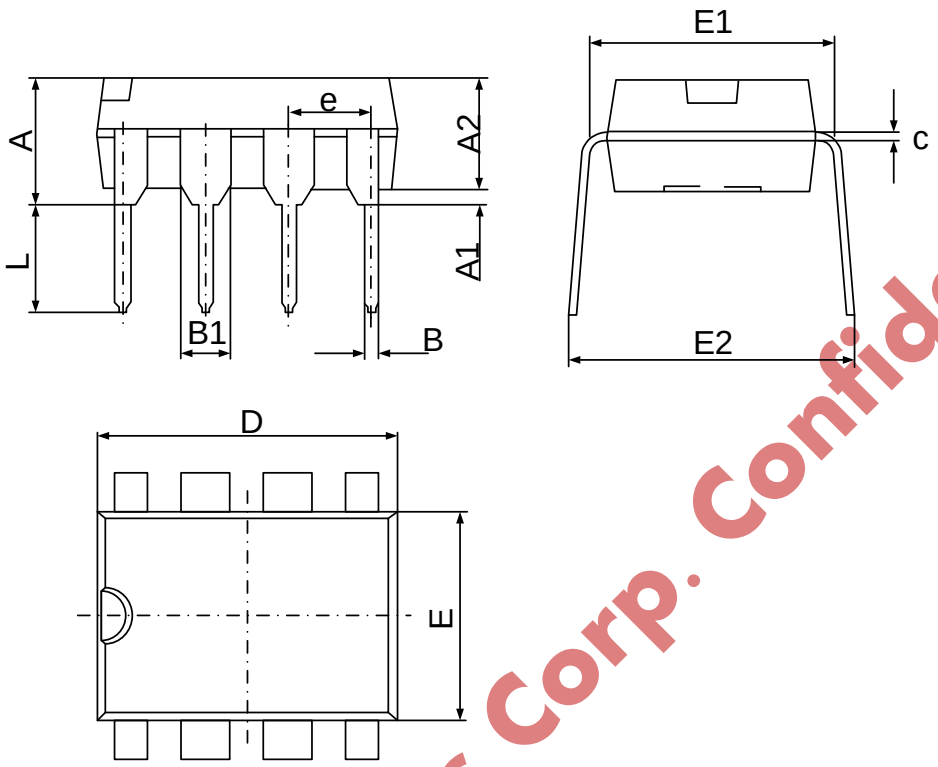
SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension (Continued)

DIP-8



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	3.600	4.150	0.142	0.163
A1	0.510	-	0.020	-
A2	3.150	3.400	0.124	0.134
B	0.380	0.560	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
c	0.200	0.350	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.500	0.244	0.256
E1	7.620 (REF)		0.300 (REF)	
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	7.620	9.300	0.300	0.366

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