Offline Inductor-less AC Linear Regulator

FEATURES

- **High Output Voltage Accuracy: 2%**
- **Programmable Output: 5V/3.3V/2.7V**
- **Smart Control to Maximize Efficiency**
- **Universal Input Range: 80~305VAC**
- **No Inductor Required**
- **No Bulk Capacitor Required**
- **Less Components and Low Cost**
- **Fast Line and Load Transient Response**
- **Short Load Protection**
- **Output Under Voltage Protection (UVP)**
- **Over Load Protection(OLP)**
- **On Chip Thermal Shutdown**
- **Available with SOP8 Package**

APPLICATIONS

- **Non Isolation AC/DC Converter**
- **Home Appliance**
- **Wall Switches and Dimmers**

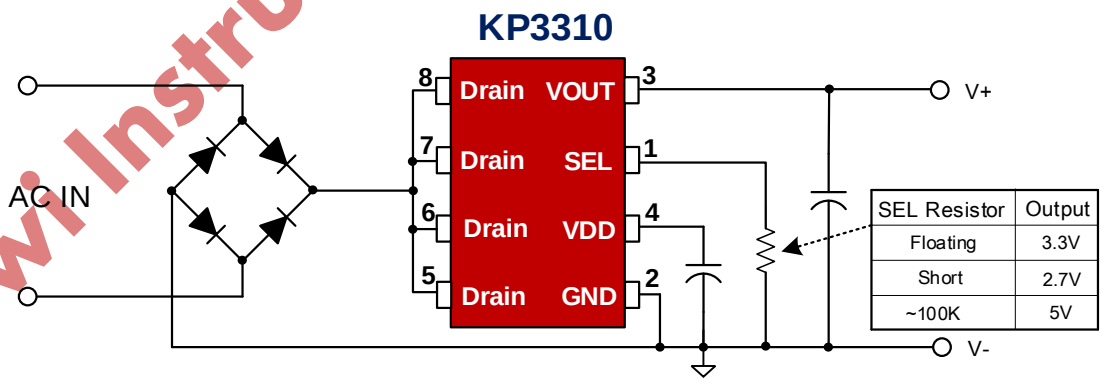
GENERAL DESCRIPTION

KP3310 is a compact, inductor-less, offline linear regulator. It steps down the AC line voltage to 5V/3.3V/2.7V based on SEL pin program. It is a simple solution to provide a bias voltage in offline applications.

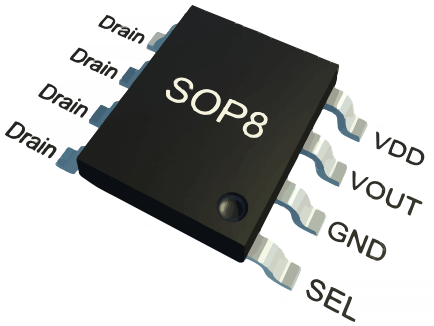
KP3310 integrates a 650V power MOSFET, startup controller, voltage control circuit, AC synchronous circuit, low dropout regulator, etc. The IC also integrates smart control system using AC line power when necessary, thus minimizing device losses to achieve good efficiency. The IC can help system designs meeting new standby power specifications.

KP3310 integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Over Load Protection (OLP), Output Under Voltage Protection (UVP), On-chip Thermal Shutdown, etc.

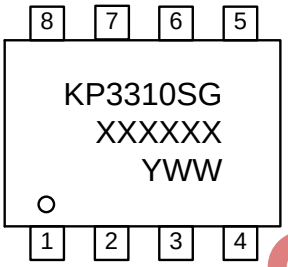
TYPICAL APPLICATION CIRCUIT



Pin Configuration



Marking Information



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YWW:Year & Week Code
Y: H-2018 WW:01-52

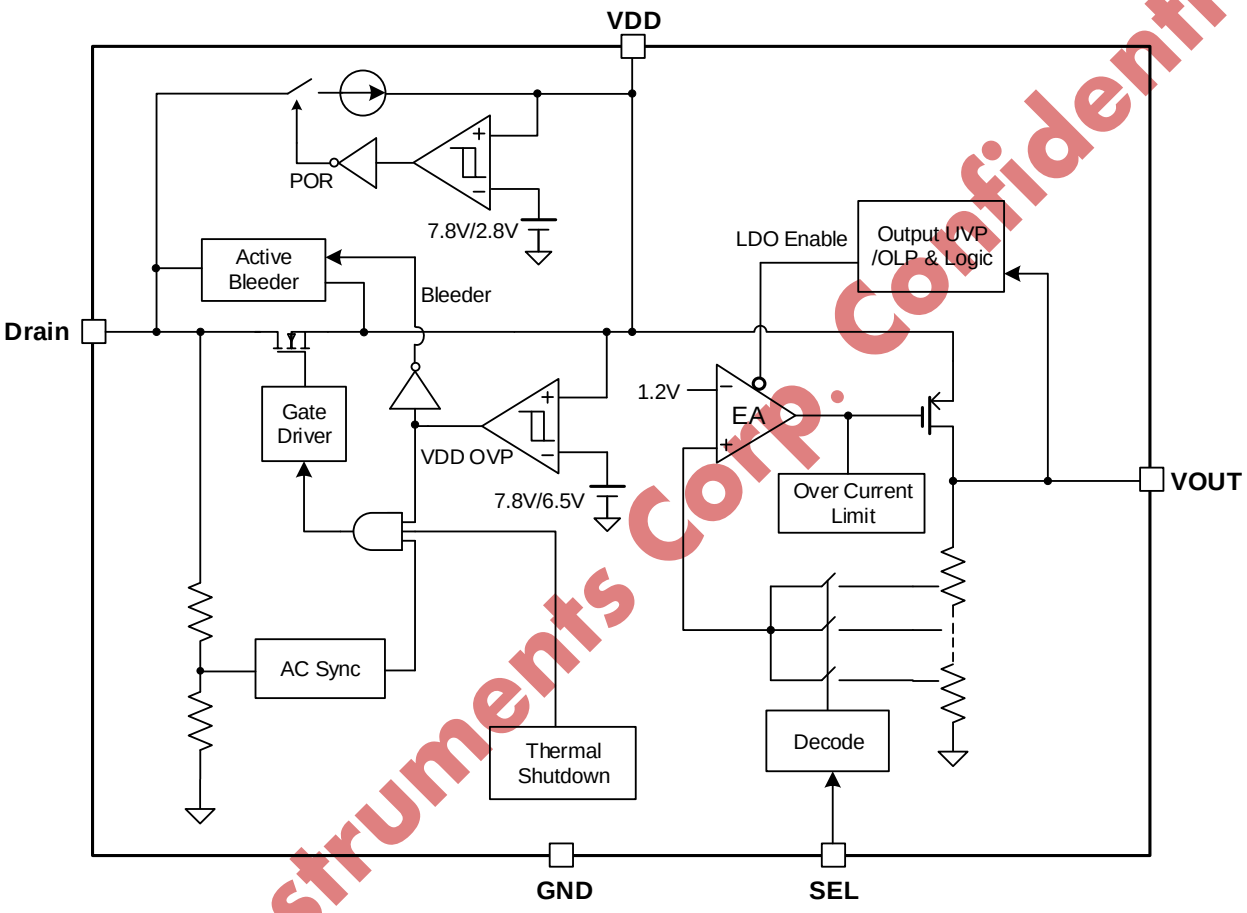
Pin Description

Pin Number	Pin Name	I/O	Description
1	SEL	I	Selection pin. If floating, the LDO outputs 3.3V. If short to GND, LDO outputs 2.7V. If connecting a 100K resistor to GND, LDO outputs 5V.
2	GND	P	The ground of the IC
3	VOUT	O	LDO output pin.
4	VDD	P	Energy storage. Connect to GND with a capacitor to buffer energy for the output LDO stage.
5,6,7,8	Drain	P	Internal power MOSFET drain pin. Provide energy when the voltage falls within the charging window.

Ordering Information

Part Number	Description
KP3310SGA	SOP-8，Halogen free, 4000Pcs/Reel

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
Drain Voltage	650	V
VDD DC Supply Voltage	9	V
VDD DC Clamp Current	10	mA
VOUT, SEL Voltage Range	-0.3 to 7	V
Package Thermal Resistance (SOP-8)	100	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
High Voltage Startup Section (Drain Pin)						
I_{HV}	HV Current Source	HV=600V, VDD=3V	5	10		mA
$I_{HV\_leakage}$	HV Leakage Current	HV=600V, VDD=8.5V			20	uA
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		650			V
$V_{AC\_sync\_OFF}$	AC Synchronization Turn OFF Voltage			50		V
Supply Voltage Section (VDD Pin)						
I_{VDD_Op}	Operation Current	Iout=1mA		1.4		mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		7.6	7.8	8	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			2.8		V
V_{DD_OVP}	VDD OVP Threshold		7.6	7.8	8	V
$V_{DD\_OVP\_hys}$	VDD OVP Threshold Hysteresis		6.3	6.5	6.7	V
VOUT Section (VOUT Pin)						

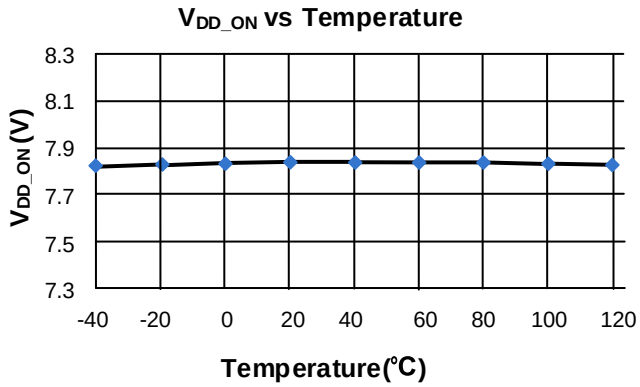
$V_{OUT\_3.3V}$	Output Voltage	SEL=Floating, Iout=2mA	3.2	3.3	3.4	V
$V_{OUT\_2.7V}$	Output Voltage	SEL=GND, Iout=2mA	2.65	2.7	2.75	V
V_{OUT_5V}	Output Voltage	SEL=100K to GND, Iout=2mA	4.9	5	5.1	V
I_{LIM}	Output Current Limit		100	138	160	mA
V_{UVP}	Output Under Voltage Protection		10	12.5	15	%
$\Delta V_{OUT(VIN)}$	Line Regulation dVout/dVin	Iout=100uA		0.2		%/V
PSRR	Power Supply Rejection Ratio	Iout=30mA, Cout=4.7uF, f=10Hz to 60KHz		60		dB
SEL Section (SEL Pin)						
I_{SEL}	SEL Pin Pull up Current			13		uA
$V_{SEL\_2.7V}$	Below the Threshold Voltage, the LDO outputs 2.7V			0.4		V
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown	(Note 3)	---	160	--	℃
T_{RC}	Thermal Recovery	(Note 3)		140	--	℃

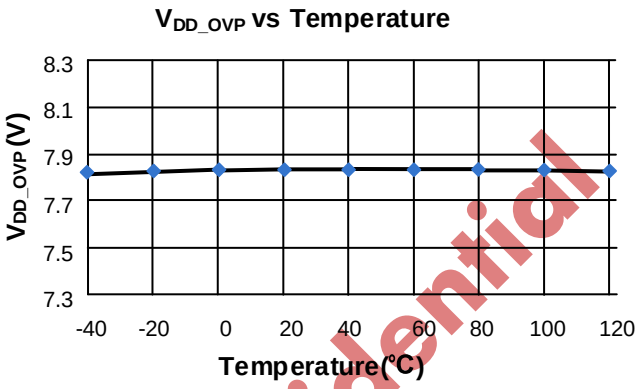
Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

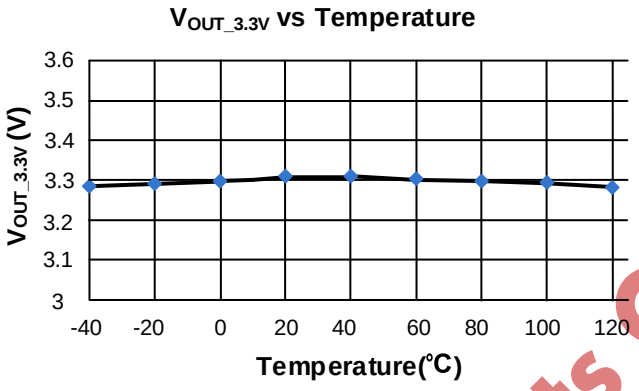
Note2. The device is not guaranteed to function outside its operating conditions.

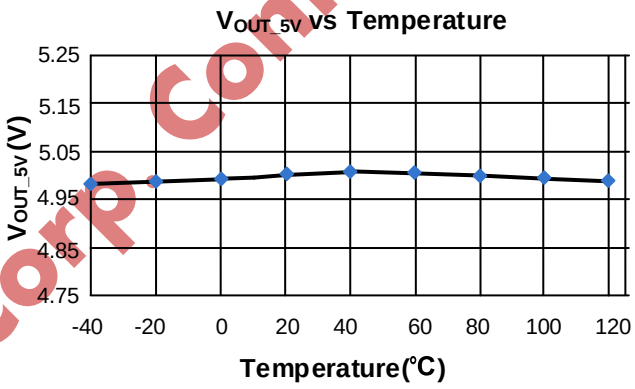
Note3. Guaranteed by the Design.

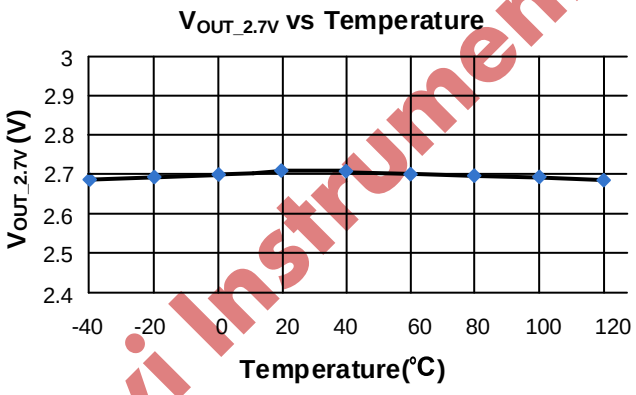
CHARACTERIZATION PLOT











OPERATION DESCRIPTION

KP3310 is a compact, inductor free, and highly monolithic AC/DC linear converter which is designed for non-isolated AC/DC converter and home appliances. The IC covers universal AC voltage input to provide programmable DC output voltage with current limit for the non-isolated AC/DC converter.

• Startup Current

During KP3310 startup, the internal high voltage current source (10mA) charges the VDD capacitor though the rectifier and Drain pin. The IC remains off until the VDD voltage is larger than V_{DD_ON} and the output voltage is built up at the same time. After the IC turns on, the internal high voltage current source is disabled by the control loop. The major energy path changes from the high voltage current source to the inner power MOSFET.

• AC Synchronization with Active Bleeder Circuit

KP3310 integrates AC synchronization block through an internal resistor divider from Drain to GND. The AC synchronous signal is used to open the power MOSFET when AC voltage is under $V_{AC\_sync\_OFF}$ to charge the VDD cap.

The Drain voltage may not enter its charging interval during normal operation due to the parasitic capacitance from Drain to GND. An active bleeder circuit is enabled to pull down the Drain voltage when VDD falls below $V_{DD\_OVP\_hys}$ and disabled when VDD reaches V_{DD_OVP}, so that enough energy from the input ports can be delivered. In addition, when protection (UVP, OLP or OTP) occurs, the active bleeder circuit discharges the energy stored in the parasitic capacitor to VDD Cap to ensure that the circuit can restart easily.

• Programmable Output: 2.7V/3.3V/5V

In KP3310, the output can be programmed by SEL pin. If SEL pin is floating, the internal LDO will output 3.3V. If SEL is short to GND, the internal LDO will output 2.7V. If 5V output is needed, a 100K resistor is to be connected between SEL and GND.

• Output Current Limit

KP3310 includes a current limiter for safe LDO operation. The limiter monitors the loading current and directly controls the output delivery current of LDO. The typical limited current set is 138mA to avoid the output shorted to ground for an indefinite amount of time without damaging the part if no protection is triggered. At over current operation, the current limiter limits the maximum output current and causes the unregulated output voltage to drop until UVP function occurs.

• Output Under Voltage Protection(UVP)

When the output power is larger than the maximum handling power of KP3310, the condition causes the output voltage to drop. Until the output voltage is less than the nominal voltage -12.5%, the UVP function disables the LDO stage and waits for two AC synchronous signal then restart the KP3310 automatically.

• Over Load Protection(OLP)

When the output voltage decreases due to heavy load, UVP is triggered. If KP3310 continues stay in UVP for 50ms, Over Load Protection is triggered, the power MOSFET and LDO is shut down for the following 640ms (Auto Recovery Delay), and VDD is charged to V_{DD_OVP} level by the internal high voltage bleeder circuit.

• VDD Over Voltage Protection (VDD OVP)

After startup, KP3310 turns on the OVP function. During conduction angle interval, the VDD voltage has two kinds of behavior. One is that if the VDD capacitor recharges to OVP trigger point (7.8V typical), KP3310 turns off the internal power MOSFET to limit the maximum VDD voltage. The other is that if the voltage of VDD cannot recharge to the OVP level during the conduction interval, the power MOSFET is turned off by AC synchronous signal and continuously recharges VDD capacitor at next duration. Using this technique, energy is drawn from the AC mains only during the low voltage portions of each half cycle. During the power MOSFET turn-on, the current provided by the commutated AC voltage is used to supply the loads and to charge the VDD capacitor. In this way, when the power MOSFET switches off, the loads receive the required currents by the capacitor discharge.

For the VDD capacitor selection, during the conduction angle interval, the energy is drawn from commutated AC bus, which not only meets the output load requirement but also recharges the VDD capacitor to OVP level. Outside of conduction angle, the VDD capacitor can is determined by the maximum loading current:

$$C_{VDD} \approx 0.01 \times I_{LOAD} \quad (\text{unit} = \text{F})$$

- **Surge Protection**

When Surge happens, AC voltage couples a very high spike voltage. If this spike voltage is higher than 100Vdc and occurs within the AC charging window, Surge Protection is triggered, the power MOSFET shuts down quickly and IC enters Auto-Restart progress.

- **On Chip Thermal Shutdown (OTP)**

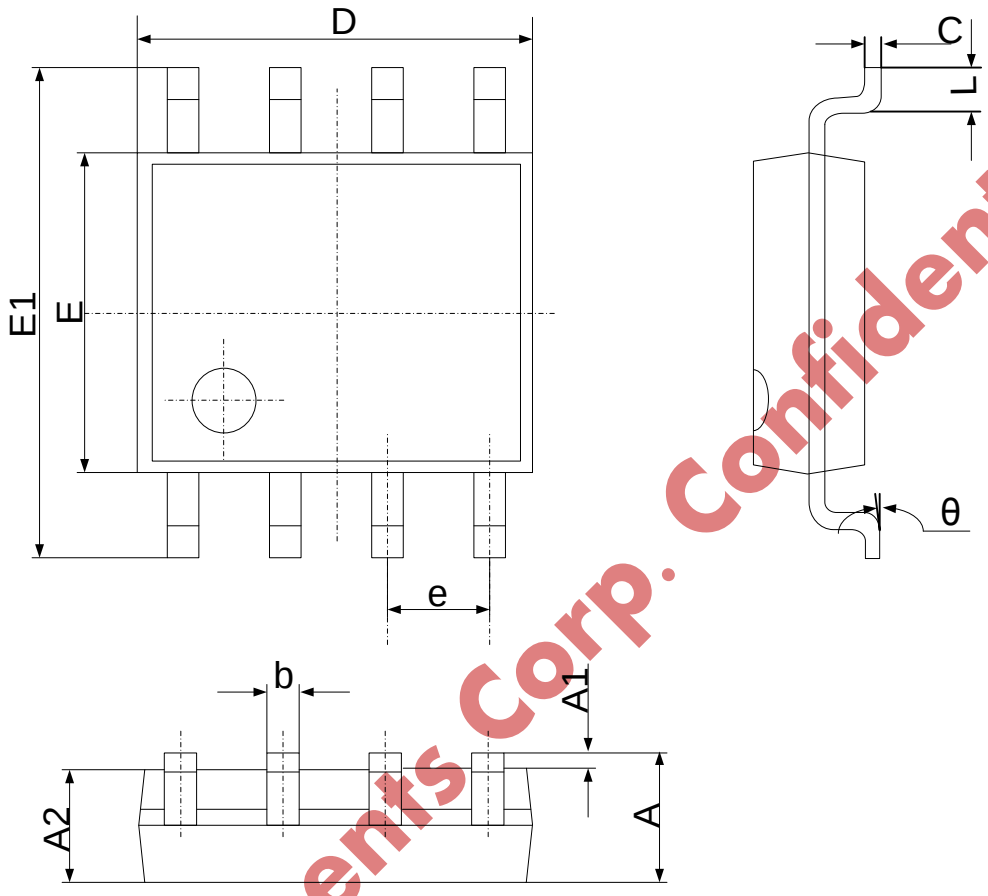
When the IC temperature is over 160 °C, the IC shuts down. Only when the IC temperature drops to 140 °C, IC will enter Auto-Restart progress.

- **Protections with Auto-Restart**

In the event of protections such as OTP, OLP, Surge Protection, the IC enters auto-restart and an internal timer begins counting, wherein the power MOSFET is disabled. When 640ms delay had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above-mentioned process.

Package Dimension

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

Revision History

DATE	REV.	DESCRIPTION
2018/03/23	1.0	First Release

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