

Secondary Side Synchronous Rectifier (SR)

FEATURES

- Secondary Side Synchronous Rectifier(SR) for Flyback converters
- Supports High-Side and Low-Side in DCM and Quasi-Resonant Topologies
- <math><300\mu\text{A}</math> Low Quiescent Current
- Built-in HV Supplies without Aux-Winding for VDD supply
- Integrated with 45V Power MOSFET
- Built-in Protections:
 - VDD UVLO
 - VDD Clamper by >5mA sink current
- Available with SOP-8 Package

APPLICATIONS

- Flyback converters
- Chargers

TYPICAL APPLICATION CIRCUIT

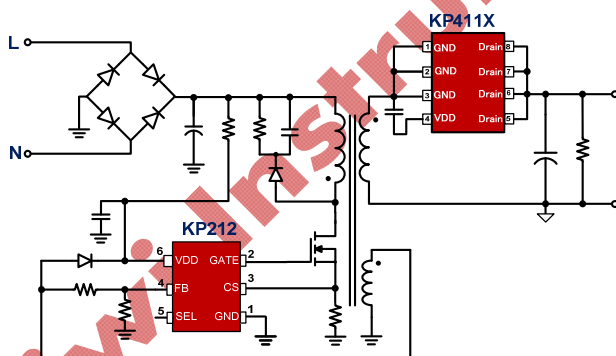
GENERAL DESCRIPTION

KP411X is a family of secondary side synchronous rectifier, that replaced Schottky diodes by combined with an ultra low on-state resistance power MOSFET for high-efficiency flyback converters. It supports High-Side and Low-Side in DCM and Quasi-Resonant Topologies.

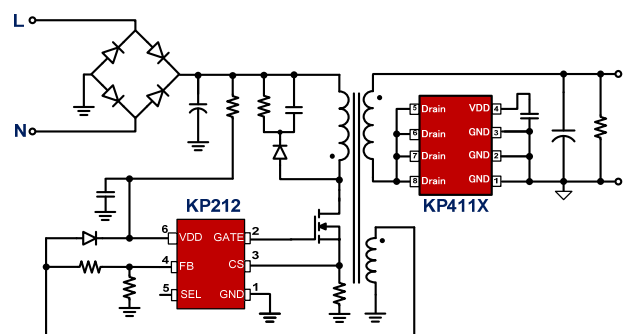
KP411X is built-in HV supplies for VDD capacitor, that can eliminate the aux-winding of VDD supply for cost saving.

KP411X integrates protections of Under Voltage Lockout (UVLO), VDD Clamper.

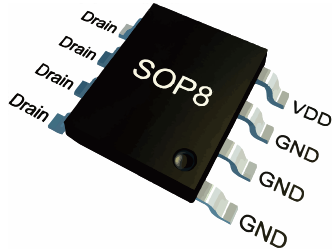
High Side SR



Low Side SR



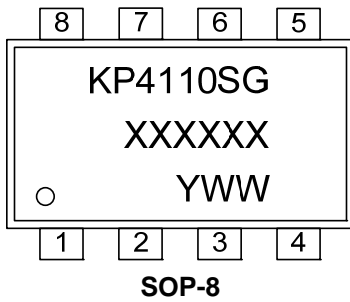
Pin Configuration



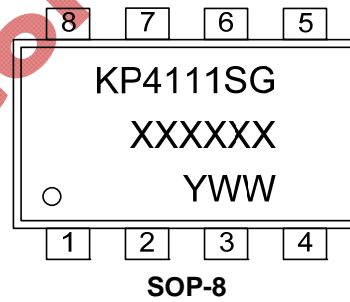
SOP-8

Marking Information

XXXXXX: Wafer Lot Code
Y: Year, G for 2017
WW: Working Week, 01-52



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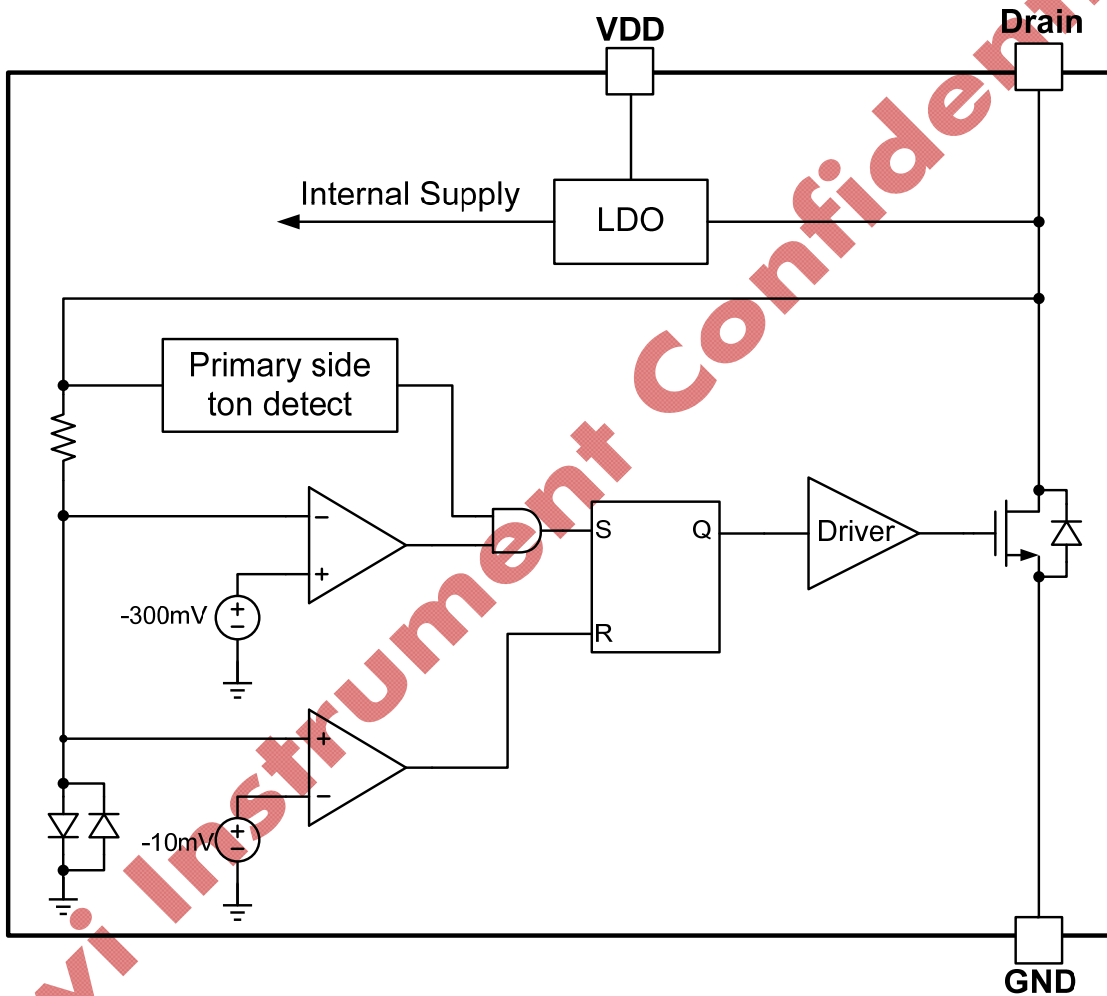
Pin Description

| Pin Number | Pin Name | I/O | Description |
|------------|----------|-----|--|
| 1,2,3 | GND | P | IC Ground Pin and also the internal Power MOSFET Source Pin |
| 4 | VDD | P | IC Power Supply Pin and 1uF Ceramic Capacitor is Recommended |
| 5,6,7,8 | Drain | I | Internal Power MOSFET Drain Pin |

Ordering Information

| Part Number | Description |
|-------------|--|
| KP4110SGA | SOP-8, Halogen free in T&R, 4000Pcs/Reel |
| KP4111SGA | SOP-8, Halogen free in T&R, 4000Pcs/Reel |

Block Diagram



Absolute Maximum Ratings (Note 1)

| Parameter | Value | Unit |
|---|------------|------|
| Drain Pin Voltage Range | -0.3 to 45 | V |
| VDD DC Supply Voltage | 7.4 | V |
| VDD DC Clamp Current | 5 | mA |
| Package Thermal Resistance----Junction to Ambient (SOP-8) | 165 | °C/W |
| Maximum Junction Temperature | 150 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | 260 | °C |
| ESD Capability, HBM (Human Body Model) | 3 | kV |
| ESD Capability, MM (Machine Model) | 250 | V |

Recommended Operation Conditions (Note 2)

| Parameter | Value | Unit |
|-------------------------------|------------|------|
| Operating Ambient Temperature | -40 to 125 | °C |

Electrical Characteristics (Ta = 25°C, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|--|----------------------------------|---------------------------|-----|------|-----|------|
| Supply Voltage Section(VDD Pin) | | | | | | |
| I _Q | Quiescent Operation Current | VDD=6V,Drain=0V | 50 | 150 | 200 | uA |
| V _{DD_reg} | HV supply VDD regulation Voltage | Drain=12V | 6.7 | 7.1 | 7.5 | V |
| I _{HV} | HV supply current | Drain=12V,VDD=5.5V | 15 | | 30 | mA |
| V _{DD_ON} | VDD Start-up Voltage | VDD rising | 3.7 | 4 | 4.3 | V |
| V _{DD_OFF} | VDD Under Voltage Lockout Enter | VDD falling | 2.8 | 3.1 | 3.4 | V |
| V _{DD_Clamp} | VDD Zener Clamp Voltage | I(V _{DD}) = 5mA | | 7.4 | | V |

| Internal MOSFET and Control Section(Drain Pin) | | | | | | |
|--|--|--------|-----|------|-----|----|
| Vth_off | Internal synchronous MOSFET turn off threshold voltage | | -15 | -10 | -5 | mV |
| Vth_on | Internal synchronous MOSFET turn on threshold voltage | | | -300 | | mV |
| Rds_on | Internal synchronous MOSFET on-state resistance | KP4110 | | 15 | 20 | mΩ |
| | | KP4111 | | 10 | 15 | mΩ |
| Td_on | Internal synchronous MOSFET turn on delay time | | | | 200 | ns |
| Td_off | Internal synchronous MOSFET turn off delay time | | | | 60 | ns |
| V _{BR} | Internal synchronous MOSFET Drain Source Breakdown Voltage | | 45 | | | V |

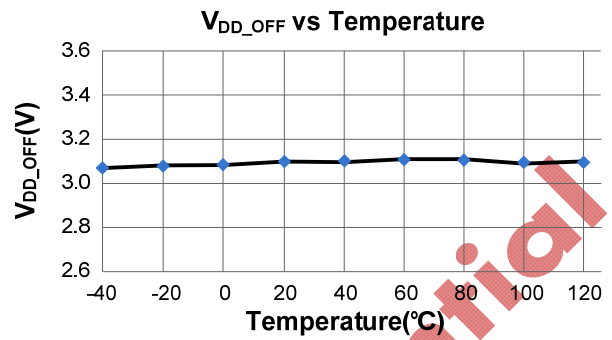
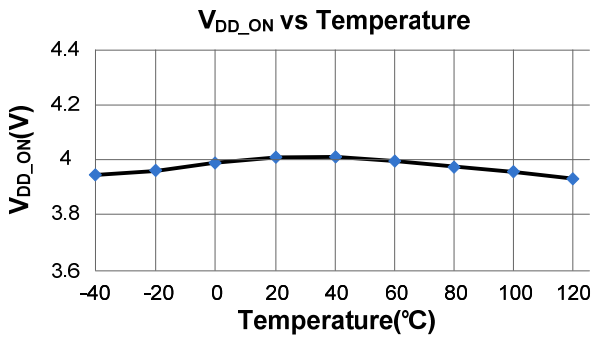
Note 1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. The device is not guaranteed to function outside its operating conditions.

Note 3. Guaranteed by the Design.

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Characterization Plots



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Operation Description

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- **7.1V Regulator**

In KP411X, the 7.1V regulator charges VDD hold-up capacitor to 7.1V by drawing a current from the Drain pin during the on state of primary side. A capacitor value about 1uF is sufficient for both high frequency decoupling and energy storage.

- **System Start-Up Operation**

After system power up, VDD hold up capacitor is charged by the internal LDO through Drain pin.

When VDD pin voltage is below UVLO threshold (3.1V typically), the IC is in sleep mode and the internal synchronous MOSFET is keeping off. The current flows through body diode of the internal synchronous MOSFET. When VDD pin voltage reaches the turn on threshold (4V typically), the IC begins working. The internal synchronous MOSFET can be only turned on during the demagnetization time of the transformer.

- **Turn-on Phase**

When the internal synchronous MOSFET is off, current will flow through its body diode which can generate a negative V_{ds} (<-500mV) across it. The body diode drop voltage V_{ds} is much smaller than

the turn on threshold of KP411X (-300mV typically), which will turn on the internal synchronous MOSFET after about 200ns turn on delay (T_{d_on}). (Shown in Fig 1)

- **Turn-off Phase**

During the turn-on period of the internal synchronous MOSFET, The KP411X senses the drop voltage V_{ds} across the on-state resistance of the MOSFET. When V_{ds} is higher than the turn off threshold (-10mV typically), the internal synchronous MOSFET will be turned off after about 60ns turn on delay (T_{d_off}). (Shown in Fig 1)

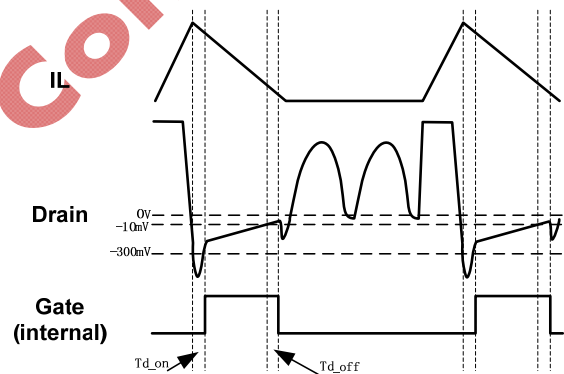
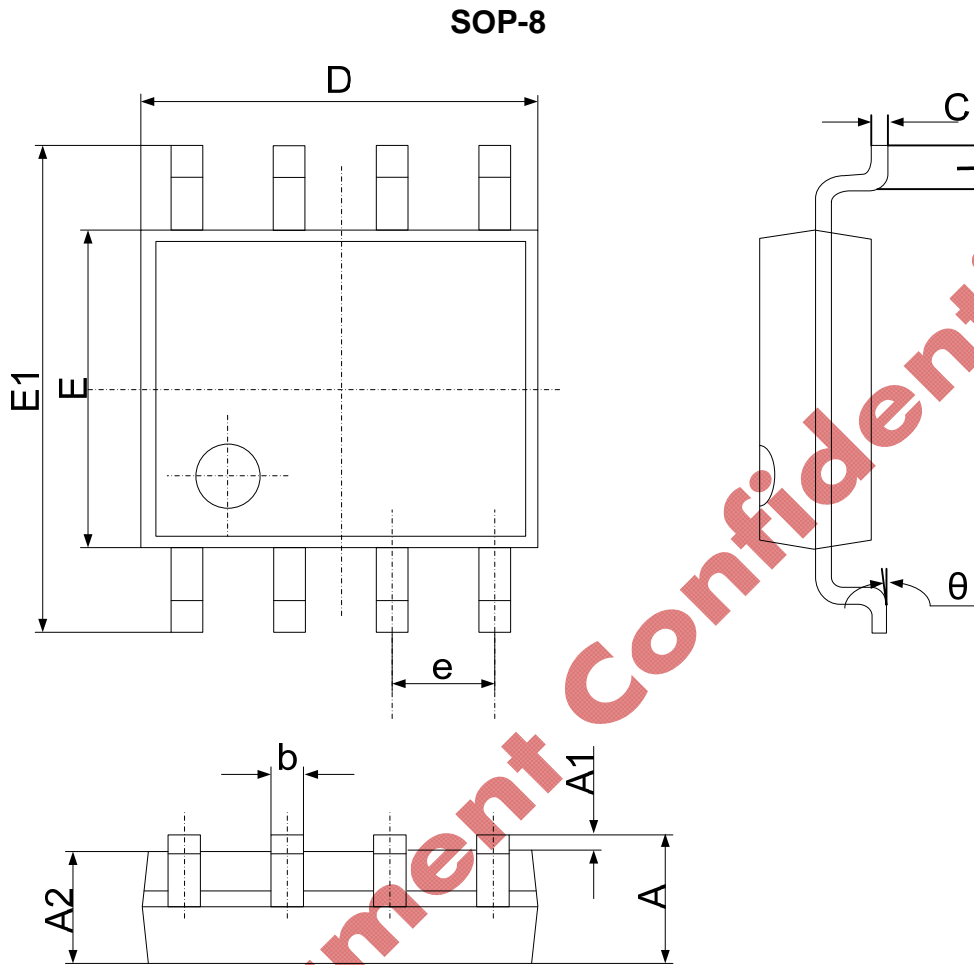


Fig 1

- **Leading Edge Blanking (LEB)**

Each time the internal synchronous MOSFET is switched on, a turn-on spike occurs across the Drain and GND. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (1us typically), the turn-off comparator is disabled and cannot switch off the internal synchronous MOSFET.

Package Dimension



| Symbol | Dimensions in Millimeters | | Dimensions in Inches | |
|----------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 (BSC) | | 0.050 (BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Revision History

| DATE | REV. | DESCRIPTION |
|------------|------|--|
| 2017/07/10 | 1.0 | First Release |
| 2017/08/09 | 1.01 | Modify “Absolute Maximum Ratings” and “Electrical Characteristics” table |

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