PST KP738

HIGH POWER PHASE CONTROL THYRISTOR
FOR PHASE CONTROL APPLICATIONS

Features :

- Blocking Capability up to 2200 V
- High dV/dt Capability
- All Diffused Structure
- Amplifying Gate Configuration
- Rugged Ceramic Hermetic Package

ELECTRICAL CHARACTERISTICS AND RATINGS

Blocking

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Repetitive peak reverse voltage	V_{RRM}		2200		V	Tj = -40 ℃ to 125 ℃
Repetitive peak off-state voltage	V_{DRM}		2200		V	Tj = -40 ℃ to 125 ℃
Non repetitive peak reverse voltage	V_{RSM}		2300		V	Tj = -40 ℃ to 125 ℃
Repetitive peak reverse current	I_{RRM}		200		mA	Tj = Tjmax , V = V_{RRM}
Repetitive peak off-state current	I_{DRM}		200		mA	Tj = Tjmax ,V = V_{DRM}

Conducting

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Average value of on-state current	$I_{T(AV)}$		3080		A	50 Hz sine wave,180° conduction, T_c = 85 ℃
RMS value of on-state current	$I_{T(RMS)}$		4836		A	50 Hz sine wave,180° conduction, T_c = 85 ℃
Surge non repetitive current	I_{TSM}		57		kA	50 Hz sine wave Half cycle V_R = 0 T_j = 125 ℃
I square t	I^2t		16245		kA^2s	
Peak on-state voltage	V_{TM}		1.15		V	On-state current 2000 A, Tj= Tjmax
Threshold voltage	$V_{T(TO)}$		0.94		V	$T_j = T_{jmax}$
On-state slope resistance	r_T		0.104		mΩ	$T_j = T_{jmax}$
Holding current	I_H			100	mA	V_D = 24 V; I_T = 2.5 A
Latching current	I_L			400	mA	V_D = 24 V; R_L = 12 Ω

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Triggering

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Gate current	I_{GT}		300		mA	V_D = 6 V; R_L = 3 Ω; Tj = - 40 ℃
			200		mA	V_D = 6 V; R_L = 3 Ω; Tj = 25 ℃
			125		mA	V_D = 6 V; R_L = 3 Ω; Tj = 25 ℃
Gate voltage	V_{GT}		5		V	V_D = 6 V; R_L = 3 Ω; Tj = - 40 ℃
			3		V	V_D = 6 V; R_L = 3 Ω; Tj = 0 ÷ 125 ℃
		0.3			V	V_D = V_{DRM}; R_L = 10 kΩ; Tj = 125 ℃
Peak gate current	I_{GM}		10		A	
Peak reverse gate voltage	V_{RGM}		5		V	
Peak gate power dissipation	P_{GM}		200		W	
Average gate power dissipation	$P_{G(AV)}$		5		W	

Switching

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Critical rate of rise of on-state current	**di/dt**	200			A/µs	Switching from V_{DRM} ≤ 1000 V
Critical rate of rise of on-state voltage	**dv/dt**	500			V/µs	Linear ramp up to 80% of V_{DRM}
Gate controlled delay time	t_d		3	2.5	µs	I_{TM} = 50 A; V_D = 1500 V; V_G = 20 V R_G = 20 Ω; t_r = 0.1 µs; t_p = 20 µs
Turn-off time	t_q		400	250	µs	I_{TM} = 500 A; di/dt = 25 A/µs;V_R ≥ 50 V dV/dt = 200 V/µs linear to 80% V_{DRM} V_G = 0 V;Tj = 125 ℃
Reverse recovery charge	Q_{rr}			2000	µC	I_T = 2000 A di/dt = 20 A/µs V_R ≥ 50 V T_j = T_{jmax}
Reverse recovery current	I_{rr}			250	A/µs	

Thermal and mechanical

Parameter	Symbol	Min	Max	Typ	Unit	Conditions
Operating temperature	T_j	-40	125		℃	
Storage temperature	T_{stg}	-40	125		℃	
Thermal resistance junction to case	$R_{th(j-c)}$		0.008		℃/W	Double side cooled , DC
Thermal resistance case to sink	$R_{th(c-s)}$		0.002		℃/W	Double side cooled, mounting surfaces smooth, flat and greased
Mounting force	**F**	40	50		kN	
Weight	**W**			1600	g	

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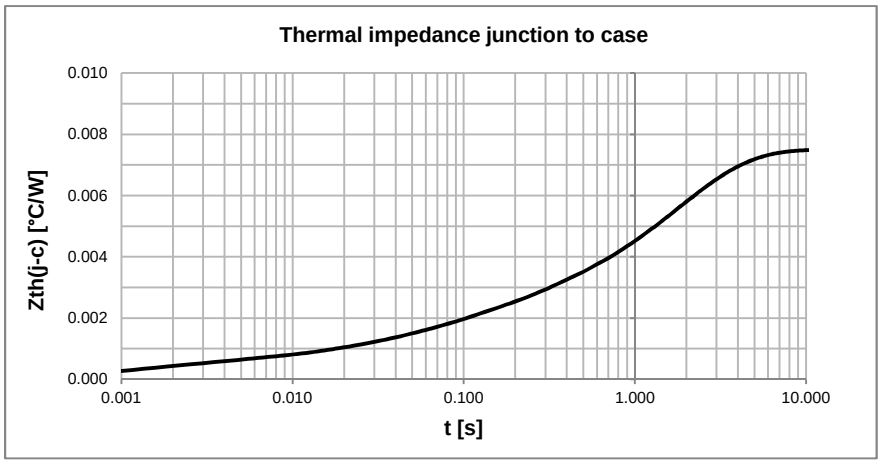
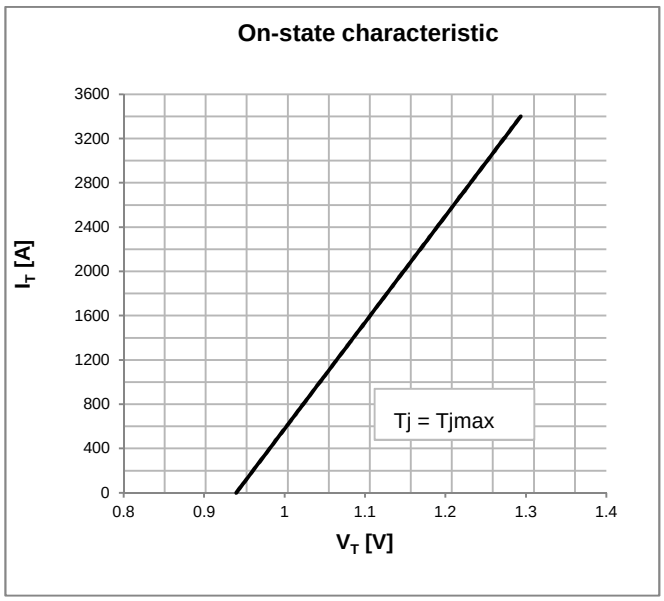
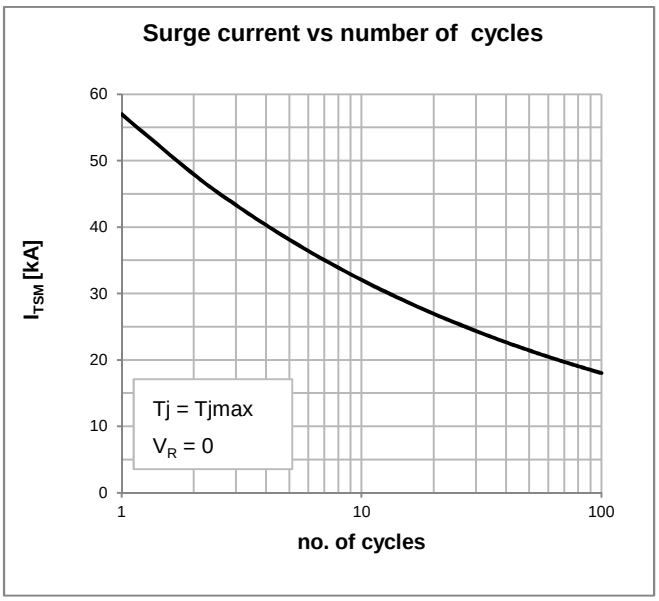
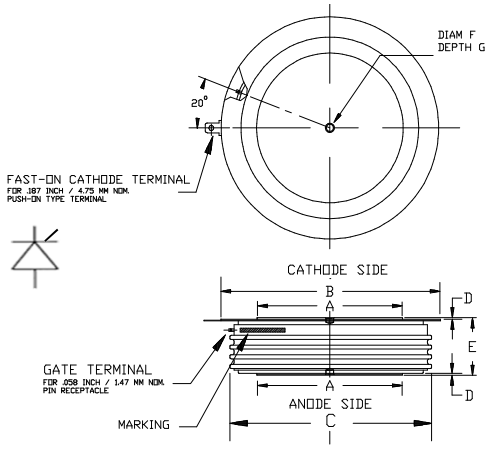






OUTLINE AND DIMENSIONS



	A	B	C	E
mm	34	59	53	26

- All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink surfaces with flatness < 0.03 mm and roughness < 2µm