650V/300mA,600mA Half Bridge Gate Driver with Integrated Bootstrap Diode

FEATURES

- **Fully Operational up to 650V**
- **Peak Output Current 0.3A Source, 0.6A Sink**
- **Integrated Fast Bootstrap Diode**
- **dV/dt Immunity of 50V/ns**
- **Logic Operational up to -7V on VS Pin**
- **Negative Voltage Tolerance on Inputs of -5V**
- **Independent UVLO for Both Channels**
- **Small Propagation Delay (175ns Typical)**
- **Delay Matching (15ns Typical)**
- **Dual Inputs with Output Interlock**
- **3.3V, 5V and 15V Input Logic Compatible**
- **Schmitt Trigger Input with Hysteresis**
- **Maximum Supply Voltage of 20V**
- **Package Type: SOP-8**

Applications

- **Power MOSFET Driver**
- **Motor Drive, Appliances, Refrigerator**
- **Lighting, LED Power Supply**
- **Induction Heating**
- **DC-to-AC Inverters**

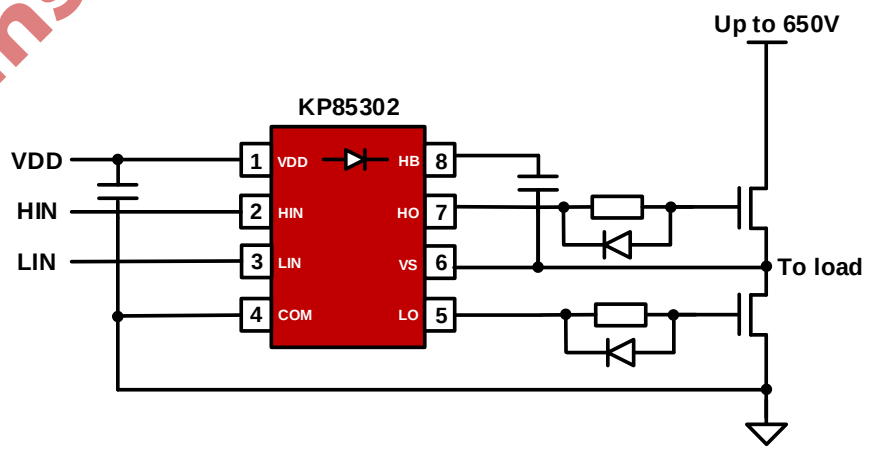
DESCRIPTION

The KP8530X is a 650V half bridge gate driver with integrated bootstrap diode. The typical source and sink current is 300mA and 600mA respectively. KP8530X targeted to drive power MOSFETS.

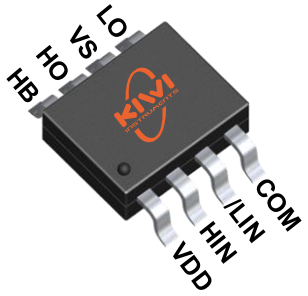
Developed with Kiwi's high-voltage device technology, KP8530X features robust drive with excellent noise and transient immunity including large negative voltage tolerance on its inputs, high dV/dt tolerance, wide negative transient voltage on switch node (VS).

KP8530X includes protection features where outputs are held low when the inputs are left open or when the minimum input pulse width specification is not met. Interlock and dead time functions prevent both outputs from being turned on simultaneously. In addition, the device accepts a wide range bias supply range from 10V to 20V, and offers UVLO protections for both high side and low side supply.

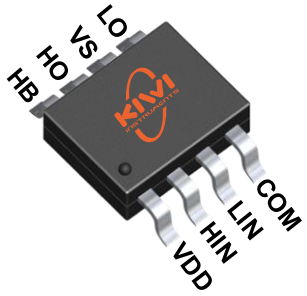
Typical Application Circuit



Pin Configuration



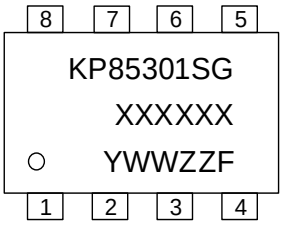
KP85301
SOP-8



KP85302
SOP-8

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ
F: Control Number 1-9 or A-Z，a-z



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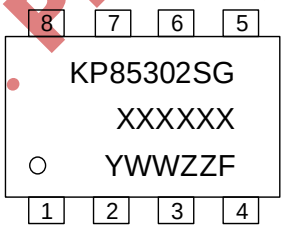


SOP-8

Pin Description

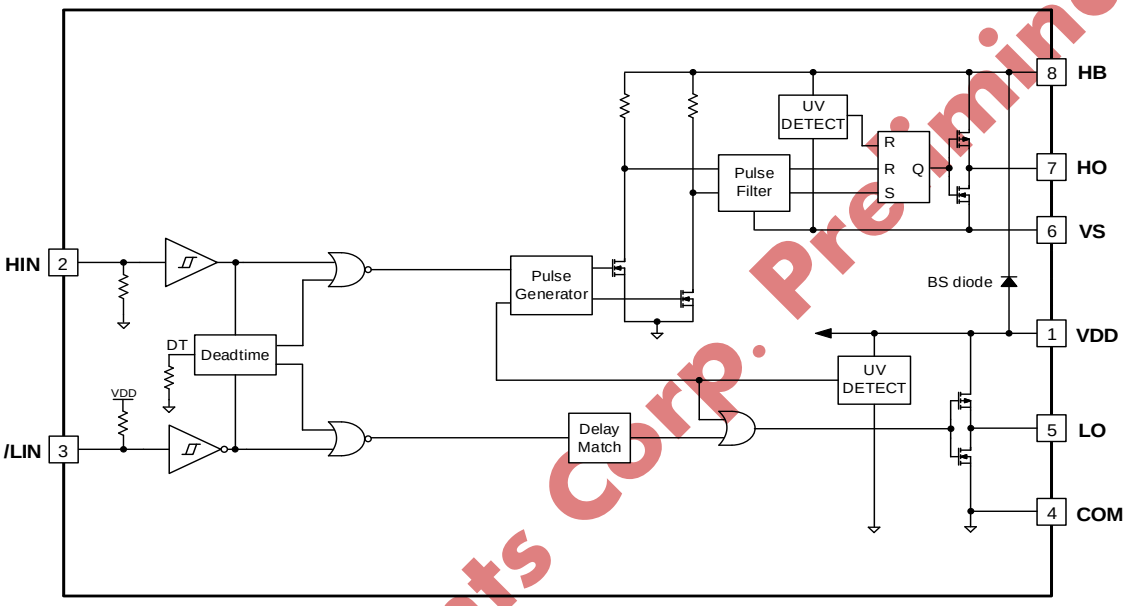
Pin Number	Pin Name		Description
	KP85301	KP85302	
1	VDD	VDD	Power supply for the input logic and low side driver. Bypass this pin to COM with a 0.1μF or larger value ceramic capacitor
2	HIN	HIN	Logic input for high side driver. If HIN is unbiased or floating, HO is held low
3	/LIN	LIN	Logic input for low side driver. If /LIN or LIN is unbiased or floating, LO is held low. For KP85301, pin 3 input is out of phase with LO, for KP85302, pin 3 input is in phase with LO.
4	COM	COM	Ground
5	LO	LO	Low Side Driver Output
6	VS	VS	Return for High Side Floating Supply
7	HO	HO	High Side Driver Output
8	HB	HB	High side floating supply. Bypass this pin to VS with a suitable capacitor to sustain boot-strap circuit operation, typical 10 times larger than the MOSFETs gate capacitance

Ordering Information

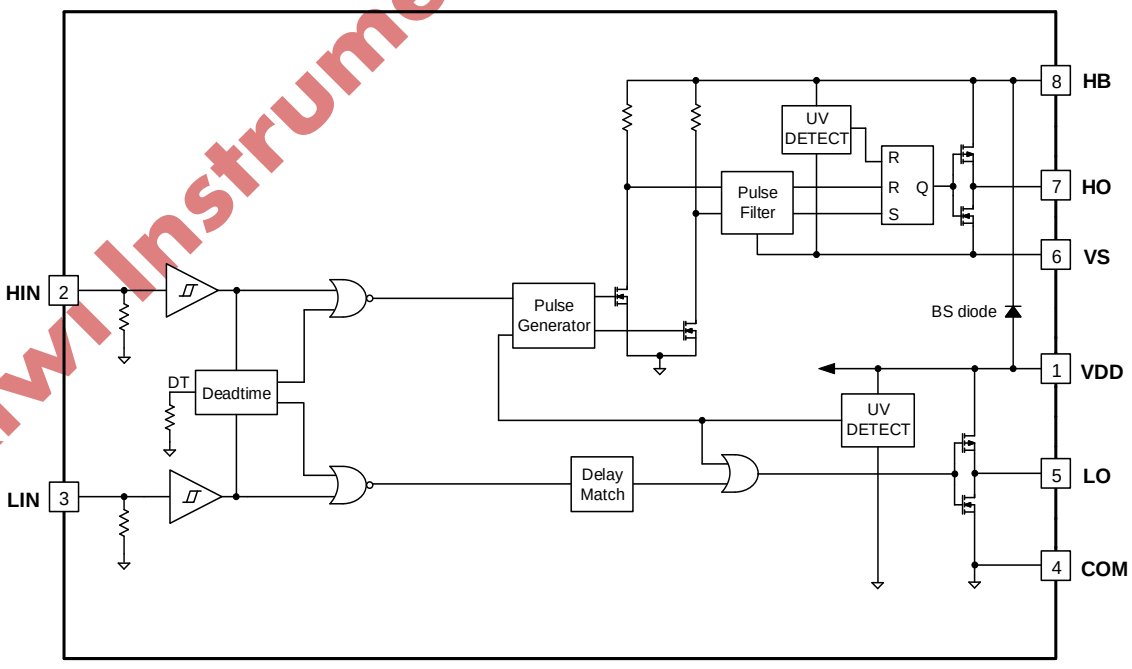
Part Number	Description
KP85301SGA	SOP-8, Halogen Free, Tape & Reel, 4000pcs/reel
KP85302SGA	SOP-8, Halogen Free, Tape & Reel, 4000pcs/reel

Note: Suffix "A" – Tape & Reel

Block Diagram



KP85301SGA internal block diagram



KP85302SGA internal block diagram

Absolute Maximum Ratings

Parameter	Min	Max	Unit
HIN, LIN, /LIN, Input Logic Pin	-5	20	V
VDD, Power Supply	-0.3	20	V
LO, Low Side Driver Output	-0.3	20	V
VS, High Side Return	-0.3	650	V
HO, High Side Driver Output	-0.3	670	V
HB, High Side Floating Supply	-0.3	670	V
dV_{VS}/dt	-50	50	V/ns
Operating Junction Temperature, T_J	-40	150	˚C
Storage Temperature, T_{stg}	-55	150	˚C
Electrostatic Discharge, HBM	±1.5		kV
Electrostatic Discharge, CDM	±500		V

Recommended Operation Conditions

Parameter	Min	Max	Unit
VDD, Power Supply	10	20	V
HIN, LIN, /LIN Logic Input	-3	20	V
VS, High Side Return	-0.3	650	V
Operating Ambient Temperature, T_A	-40	125	˚C

Thermal Information

Thermal Impedance	SOIC8	Unit
R_{th_JA}, Junction-to-Ambient Thermal Resistance	200	˚C/W

Electrical Characteristics

(T_A=25˚C, VDD=15V, unless otherwise noted)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Power Supply (VDD, VHB)						
V_{DD_ON}	Turn On Threshold of VDD		8	8.9	9.8	V
V_{DD_OFF}	Turn Off Threshold of VDD		7.5	8.4	9.3	V

V_{HB_ON}	Turn on Threshold of HB-VS		7.2	8.2	9.2	V
V_{HB_OFF}	Turn off Threshold of HB-VS		6.4	7.3	8.3	V
I_{QVDD}	Quiescent VDD-COM Supply Current			50		μA
I_{QBS}	Quiescent HB-VS Supply Current			20		μA
I_{OP}	Dynamic Operating Current	F=100kHz, duty=50%, CL=1nF		3.2	4.5	mA
Input block (HIN, LIN, /LIN)						
V_{IH}	Input Voltage High Threshold		2.0			V
V_{IL}	Input Voltage Low Threshold				1.2	V
I_{IH}	Input High Bias Current	HIN,LIN=5V, KP85302	1.7		70	μA
I_{IL}	Input Low Bias Current	HIN,LIN=0V, KP85302	-5	0	5	μA
Output block (HO, LO)						
Rpd	HO,LO Pull Down Resistance	IHO=ILO=20mA		8		Ω
Rpu	HO,LO Pull Up Resistance	IHO=ILO=-20mA		16		Ω
Bootstrap diode						
R_{BS_diode}	Bootstrap Diode Resistance			310		Ω
Dynamic Parameters						
t_{PDLH}	Turn on Propagation Delay, Without Deadtime	LIN to LO, HIN to HO, VS=COM=0V		170		ns
t_{PDHL}	Turn off Propagation Delay	LIN to LO, HIN to HO, VS=COM=0V		185		ns
t_{PDRM}	Low-to-High Delay Matching			10	30	ns
t_{PDFM}	High-to-Low Delay Matching			10	30	ns
t_{RISE}	Turn on Rise Time	10% to 90%, HO/LO with 1nF Load		50		ns
t_{FALL}	Turn off Fall Time	10% to 90%, HO/LO with 1nF Load		50		ns
t_{ON}	Minimum HIN, LIN, /LIN ON Pulse that Changes Output State	0 V to 5 V Input Signal on HIN, LIN and /LIN Pins		70		ns
t_{OFF}	Minimum HIN, LIN, /LIN OFF Pulse that Changes Output State	5V to 0V Input Signal on HIN, LIN and /LIN Pins		70		ns
DT	Dead Time	Internal Deadtime for Interlock	300	500	700	ns

Function Timing Diagram

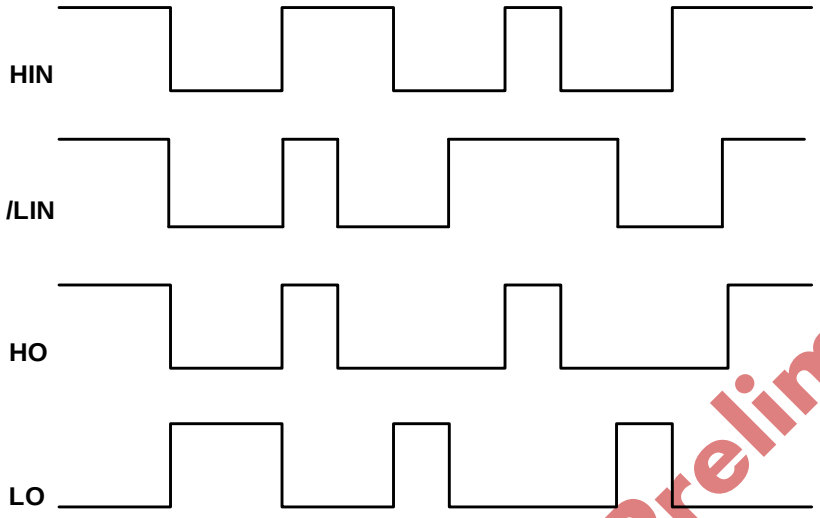


Figure 1 KP85301 Input and output timing waveform

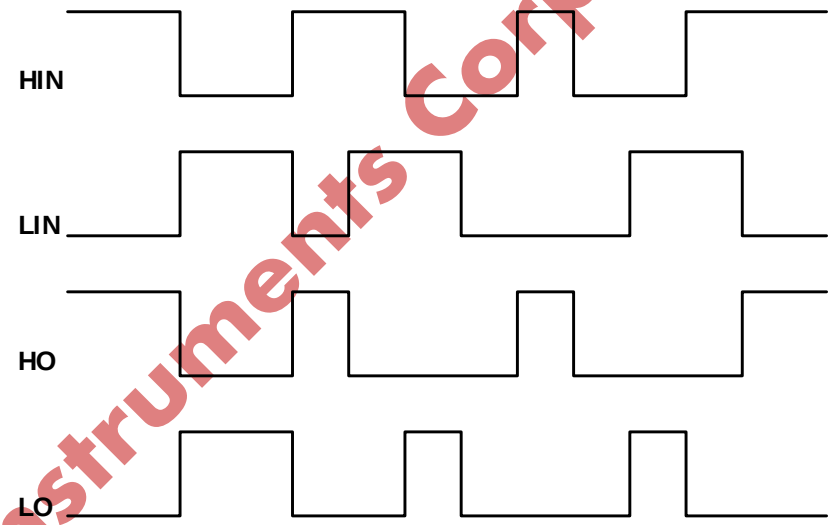


Figure 2 KP85302 Input and output timing waveform

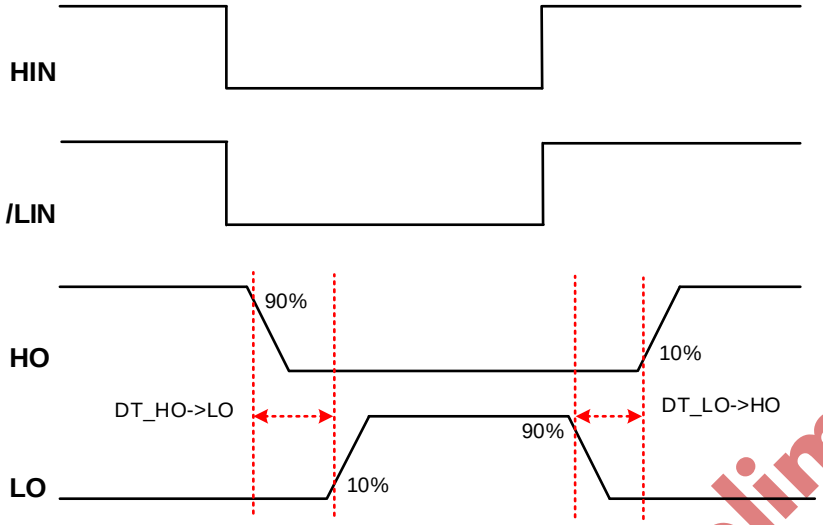


Figure 3 KP85301 Dead Time Definition

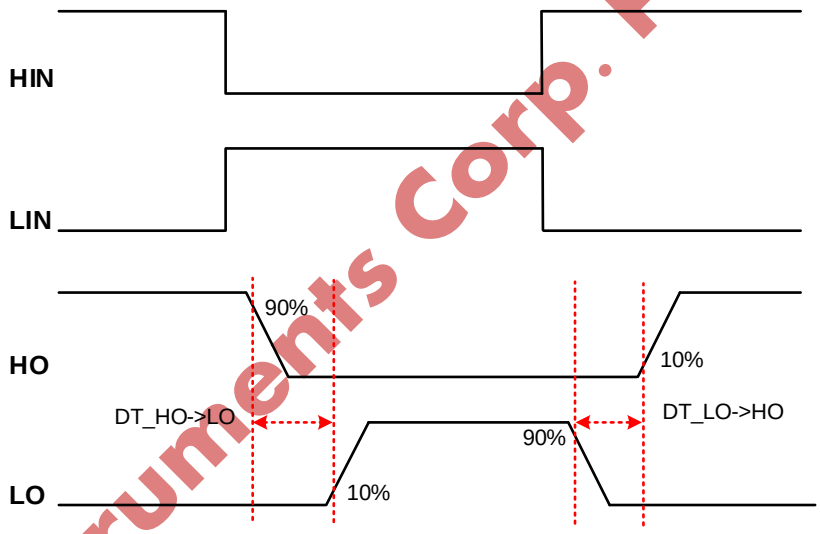


Figure 4 KP85302 Dead Time Definition

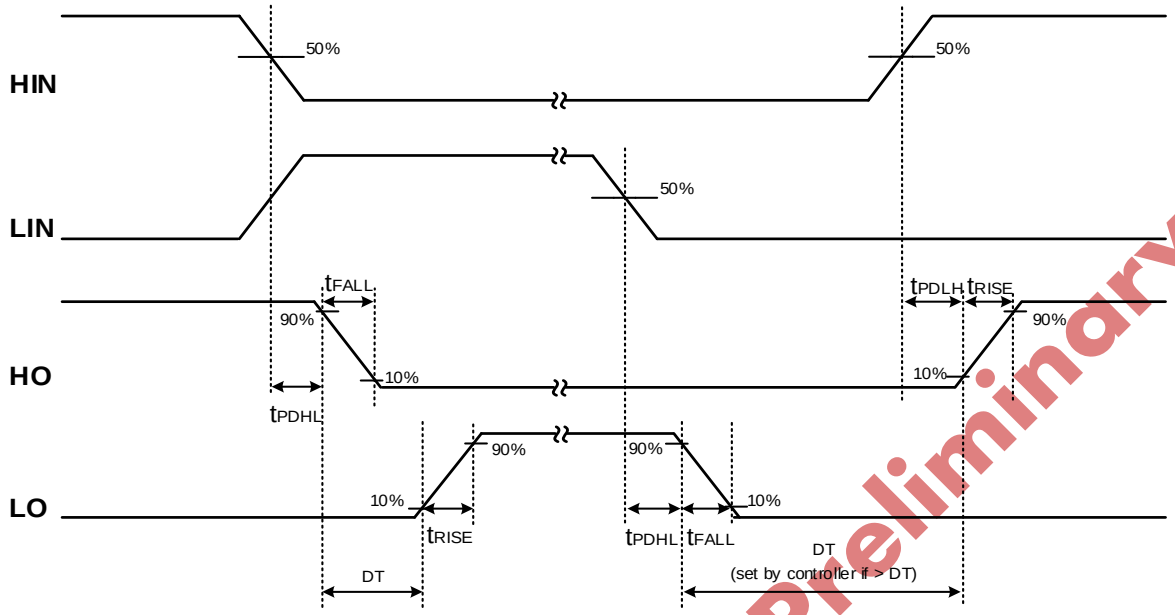


Figure 5 Typical Test Timing Diagram

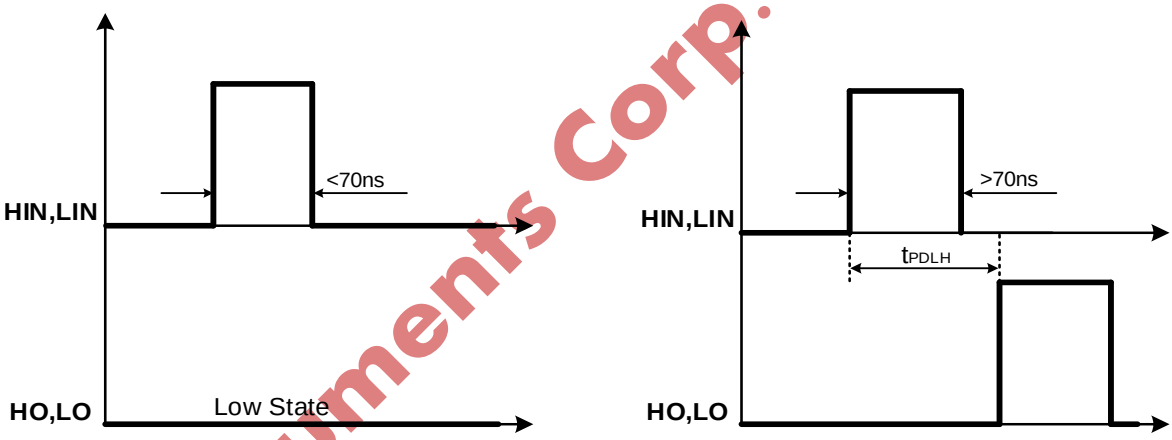


Figure 6 Minimum Turn-On Pulse

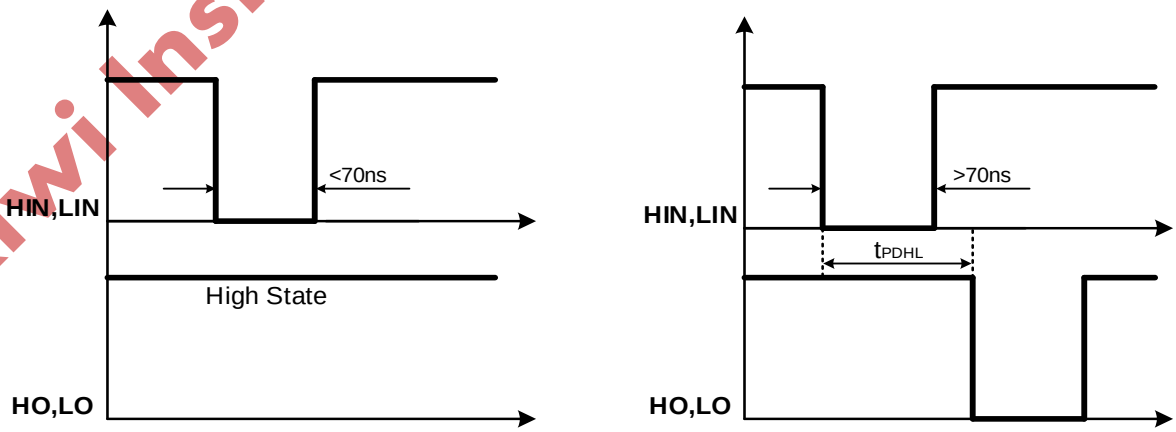


Figure 7 Minimum Turn-Off Pulse

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