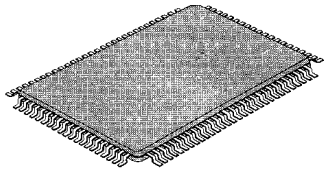
KS0063 80CH SEGMENT DRIVER FOR DOT MATRIX LCD

INTRODUCTION

The KSOO63 is a LCD driver LSl which is fabricated by low power CMOS technology. Basically this LSl consists of 40x2 bit bidrectional shift register, 40x2 bit data latch and 40x2 bit LCD driver (refer to Fig 1). This LSl can be used segment driver.

100 QFP



FUNCTION

- Dot matrix LCD driver with 80 channel output.
- Input/Output signal
  - Output : 40¡¿2channel waveform for LCD driving
  - Input : - Serial display data and control pulse from the controller LSl.
    - Bias voltage (V_1 - V_4)

FEATURES

- Display driving bias ; static-1/5
- Power supply voltage ; +5V±10%
- Supply voltage for display : 0 ~ - 5V(V_{EE})
- interface

driver (cascade connection)	controller
KS0065B, Other KS0063	KS0066/U

- CMOS Process
- l00QFP and bare chip available

BLOCK DIAGRAM

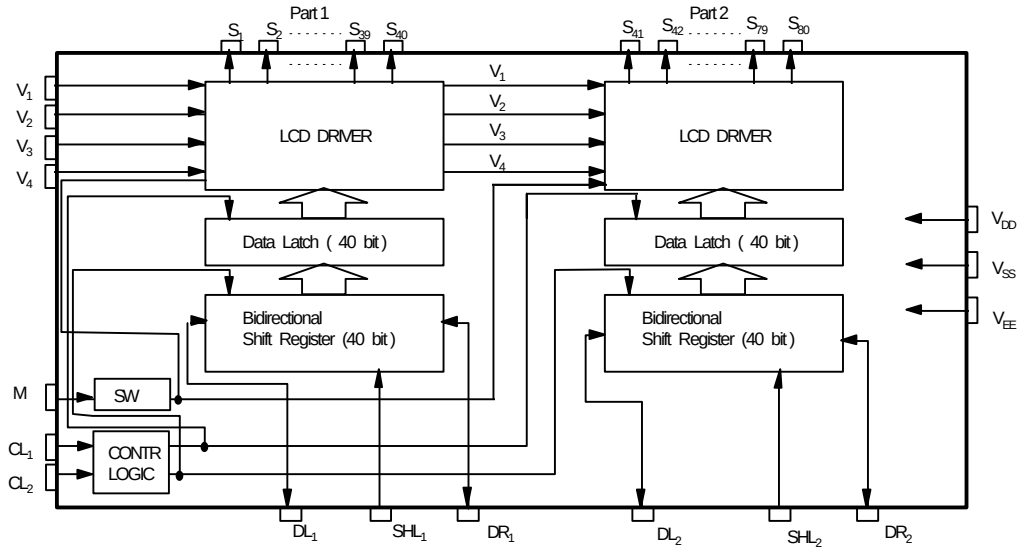


Fig. 1. KS0063 functional block diagram

PIN CONFIGURATION

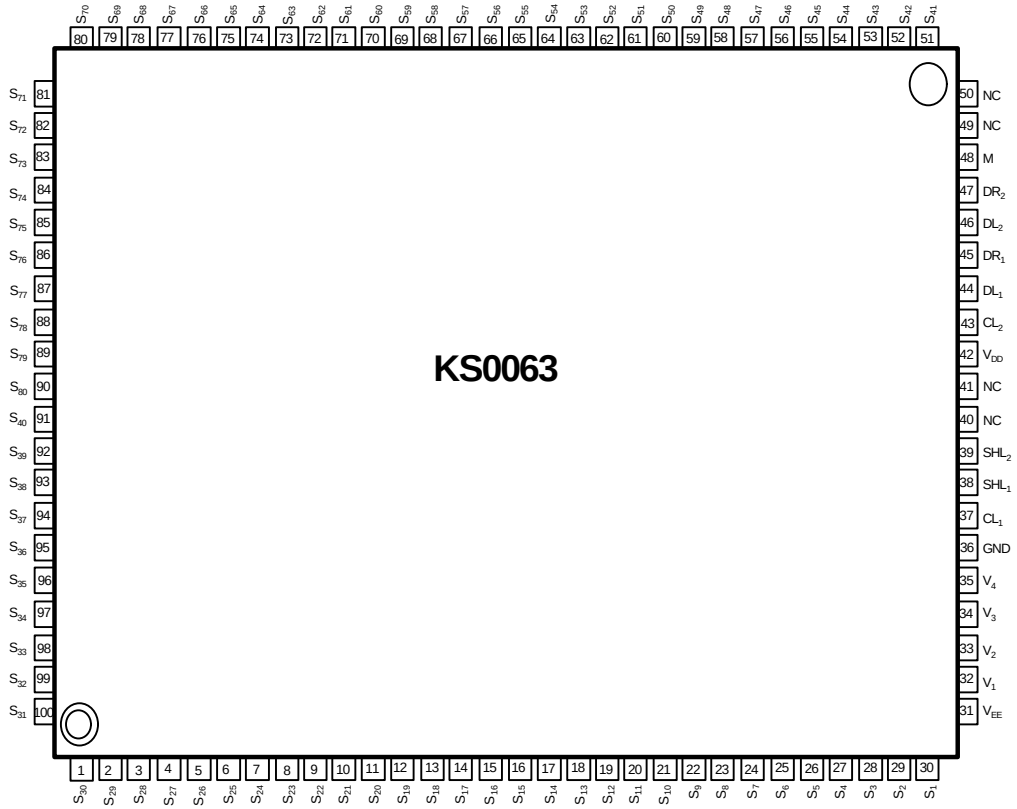


Fig. 2.100QFP Top View

PIN DESCRIPTION

<table>
<tr><th>PIN (NO.)</th><th>INPUT
OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(42)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (+5V±10%)</td><td rowspan="3">Power
Supply</td></tr>
<tr><td>V_{SS}(GND)(36)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit (- 5V)</td></tr>
<tr><td>V1, V2
(32,33)</td><td>Input</td><td colspan="2" rowspan="2">LCD driver
output voltage level</td><td>Bias voltage level for LCD drive (Select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V3, V4 (34,35)</td><td>Input</td><td>Bias voltage level for LCD drive (Nonselect level)</td></tr>
<tr><td>S1 - S40</td><td>Output</td><td rowspan="3">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL1(38)</td><td>Input</td><td>Data
Interface</td><td>Selection of the shift direction of shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>OUT</td><td>IN</td></tr><tr><td>V_{SS}</td><td>IN</td><td>OUT</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1
(44,45)</td><td>Input
Output</td><td colspan="2">Data Input/output of shift register (part 1)</td><td>Controller or
KS0063</td></tr>
<tr><td>S41 - S80</td><td>Output</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL2 (39)</td><td>Input</td><td>Data
Interface</td><td>Selection of the shift direction of shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>OUT</td><td>IN</td></tr><tr><td>V_{SS}</td><td>IN</td><td>OUT</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2, DR2
(46,47)</td><td>Input
Output</td><td colspan="2">Data Input/output of shift register (part 2)</td><td>Controller or
KS0063</td></tr>
<tr><td>M(48)</td><td>Input</td><td colspan="2">Alternated signal for
LCD driver output</td><td>The alternating signal to convert LCD drive
waveform to AC</td><td rowspan="2">Controller</td></tr>
<tr><td>CL1, CL2
(37,43)</td><td>Input</td><td colspan="2">Data shift/latch clock</td><td>CL1 : Data latch clock
CL2 : Data shift clock</td></tr>
<tr><td>NC
(40, 41, 49, 50)</td><td></td><td colspan="2"></td><td>No connection</td><td>NC</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (T_a=25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3~+7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD}-13.5~V_{DD}+0.3	V
Input Voltage 1	V_{IN1}	-0.3~V_{DD}+0.3	V
Input Voltage 2 (V_1~V_4)	V_{IN2}	V_{DD}+0.3~V_{EE}-0.3	V
Operating Temperature	T_{OPR}	-20~+75	°C
Storage Temperature	T_{STG}	-55~+125	°C

* Voltage greater than above may damage to the circuit
* V_{EE} : connect a protection resistor (220 kΩ ±5%)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}= +5V ±10% V_{EE}= -5 ±10% V_{SS}=0V, Ta=-20 ~ +75°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current	I_{DD}	f_{CL2} = 400KHz	-	1	mA	V_{DD}, V_{EE}
Supply Current	I_{EE}	f_{CL1} = 1KHz	-	10	µs	
Input High Voltage	V_{IH}	-	0.7V_{DD}	V_{DD}	V	CL1, CL2,DL1,
Input Low Voltage	V_{IL}		0	0.3V_{DD}		DL2, DR1, DR2,
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ V_{DD}	-5	5	µs	SHL1, SHL2, M
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	-		DL1, DL2,
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA		0.4	V	DR1, DR2
Voltage Descending	V_{D1}	I_{ON} = 0.1mA for one of S_1 - S_{80}	-	1.1		V(V_1-V_4)-S(S_1-S_{80})
	V_{D2}	I_{ON} = 0.05mA for each S_1 - S_{80}	-	1.5		
Leakage Current	I_V	V_{IN} = V_{DD} ~ V_{EE} (Output S_1 ~ S_{80} ; floating)	-10	10	µs	V_1 - V_4

AC CHARACTERISTICS (V_{DD} = +5V±10%, V_{EE} = -5V±10%, V_{SS}=0V, Ta = -20 ~ +75°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1,CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		
Data Set-up Time	t_{SU}	-	300	-		DL1,DL2,DR1,DR2
Data Hold Time	t_{DH}	-	300	-		DL1,DL2,DR1,DR2
Data Delay Time	t_D	C_L = 15pF	-	500		DL1,DL2,DR1,DR2

TIMING CHARACTERISTICS

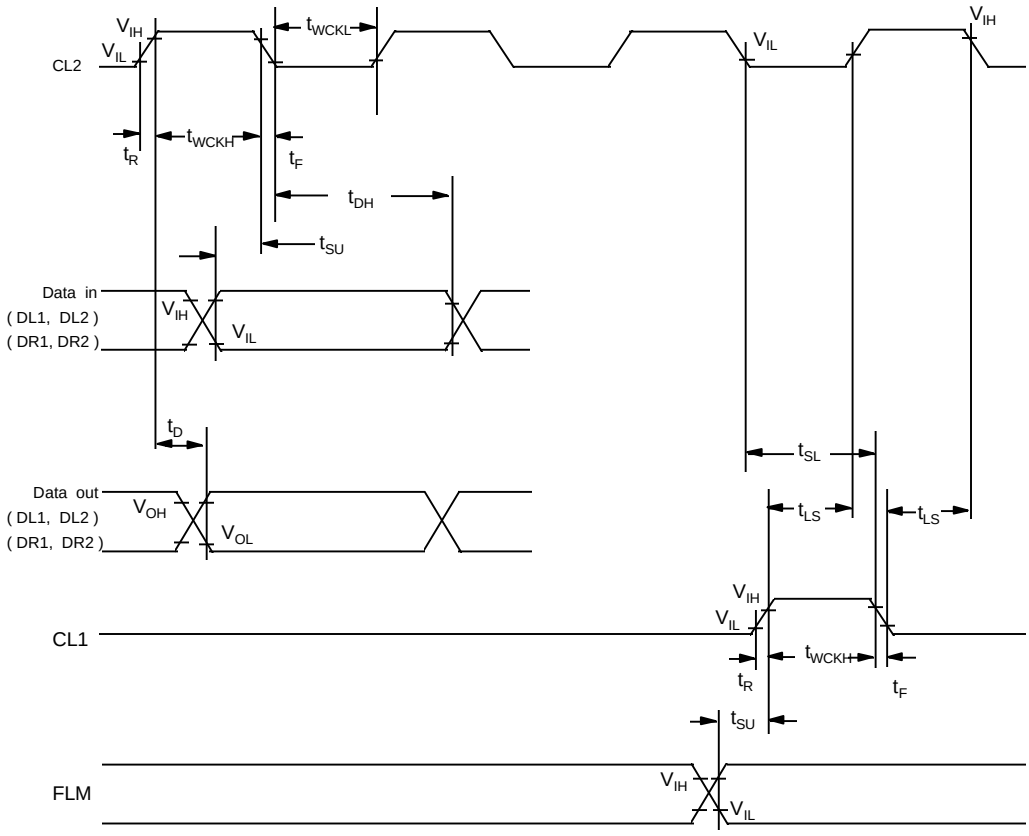
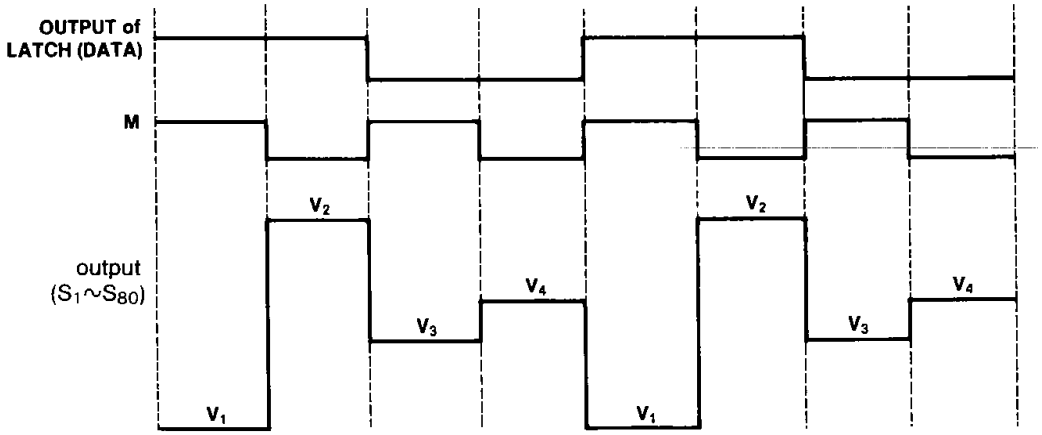
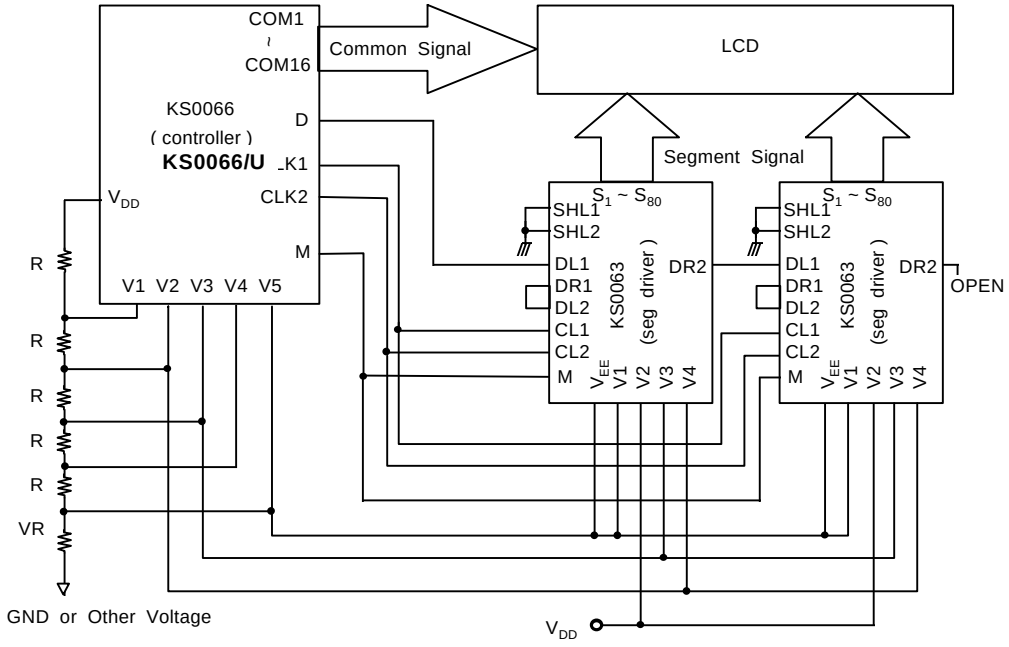


Fig 3.AC characteristics

LCD OUTPUT WAVEFORMS



APPLICATION CIRCUIT

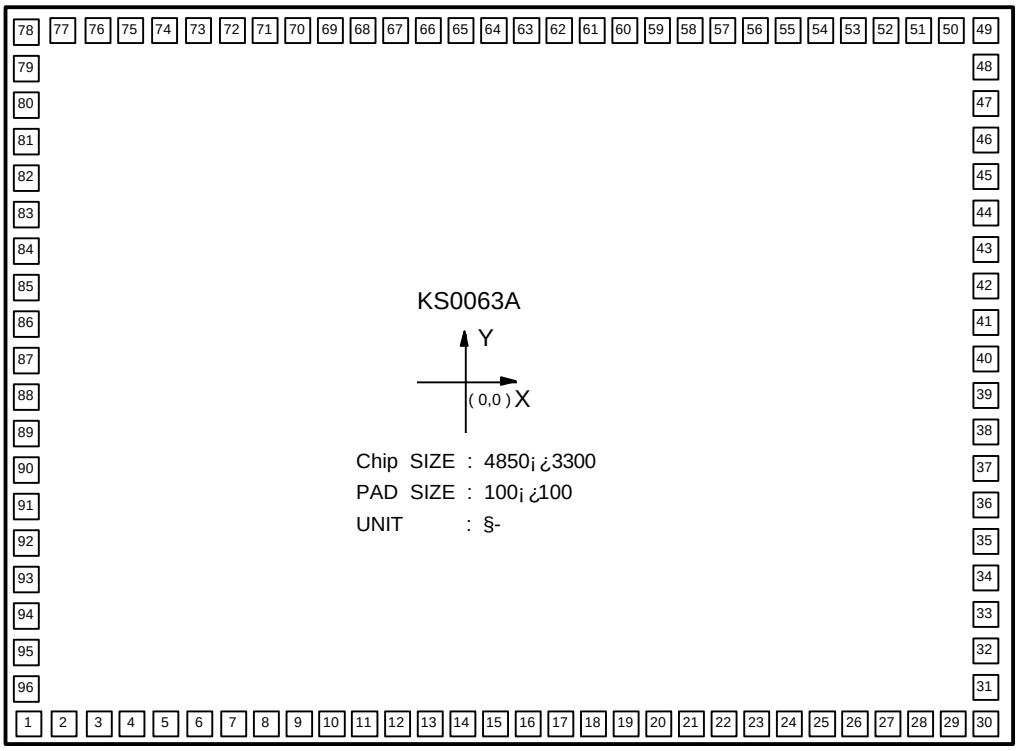


PAD LOCATION

UNIT (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	S42	-2247.5	-1472.5	33	S74	2247.5	-1007.5	65	S15	-232.5	1472.5
2	S43	-2092.5	-1472.5	34	S75	2247.5	-852.5	66	S14	-387.5	1472.5
3	S44	-1937.5	-1472.5	35	S76	2247.5	-697.5	67	S13	-542.5	1472.5
4	S45	-1782.5	-1472.5	36	S77	2247.5	-542.5	68	S12	-697.5	1472.5
5	S46	-1627.5	-1472.5	37	S78	2247.5	-387.5	69	S11	-852.5	1472.5
6	S47	-1472.5	-1472.5	38	S79	2247.5	-232.5	70	S10	-1007.5	1472.5
7	S48	-1317.5	-1472.5	39	S80	2247.5	-77.5	71	S9	-1162.5	1472.5
8	S49	-1162.5	-1472.5	40	S40	2247.5	77.5	72	S8	-1317.5	1472.5
9	S50	-1007.5	-1472.5	41	S39	2247.5	232.5	73	S7	-1472.5	1472.5
10	S51	-852.5	-1472.5	42	S38	2247.5	387.5	74	S6	-1627.5	1472.5
11	S52	-697.5	-1472.5	43	S37	2247.5	542.5	75	S5	-1782.5	1472.5
12	S53	-542.5	-1472.5	44	S36	2247.5	697.5	76	S4	-1937.5	1472.5
13	S54	-387.5	-1472.5	45	S35	2247.5	852.5	77	S3	-2092.5	1472.5
14	S55	-232.5	-1472.5	46	S34	2247.5	1007.5	78	S2	-2247.5	1472.5
15	S56	-77.5	-1472.5	47	S33	2247.5	1162.5	79	S1	-2247.5	1317.5
16	S57	77.5	-1472.5	48	S32	2247.5	1317.5	80	VEE	-2247.5	1162.5
17	S58	232.5	-1472.5	49	S31	2247.5	1472.5	81	V1	-2247.5	1007.5
18	S59	387.5	-1472.5	50	S30	2092.5	1472.5	82	V2	-2247.5	852.5
19	S60	542.5	-1472.5	51	S29	1937.5	1472.5	83	V3	-2247.5	697.5
20	S61	697.5	-1472.5	52	S28	1782.5	1472.5	84	V4	-2247.5	542.5
21	S62	852.5	-1472.5	53	S27	1627.5	1472.5	85	GND	-2247.5	387.5
22	S63	1007.5	-1472.5	54	S26	1472.5	1472.5	86	CL1	-2247.5	232.5
23	S64	1162.5	-1472.5	55	S25	1317.5	1472.5	87	SHL1	-2247.5	77.5
24	S65	1317.5	-1472.5	56	S24	1162.5	1472.5	88	SHL2	-2247.5	-77.5
25	S66	1472.5	-1472.5	57	S23	1007.5	1472.5	89	VDD	-2247.5	-232.5
26	S67	1627.5	-1472.5	58	S22	852.5	1472.5	90	CL2	-2247.5	-387.5
27	S68	1782.5	-1472.5	59	S21	697.5	1472.5	91	DL1	-2247.5	-542.5
28	S69	1937.5	-1472.5	60	S20	542.5	1472.5	92	DR1	-2247.5	-697.5
29	S70	2092.5	-1472.5	61	S19	387.5	1472.5	93	DL2	-2247.5	-852.5
30	S71	2247.5	-1472.5	62	S18	232.5	1472.5	94	DR2	-2247.5	-1007.5
31	S72	2247.5	-1317.5	63	S17	77.5	1472.5	95	M	-2247.5	-1162.5
32	S73	2247.5	-1162.5	64	S16	-77.5	1472.5	96	S41	-2247.5	-1317.5

PAD DIAGRAM



* There is mark of KS0063A on the center in chip.