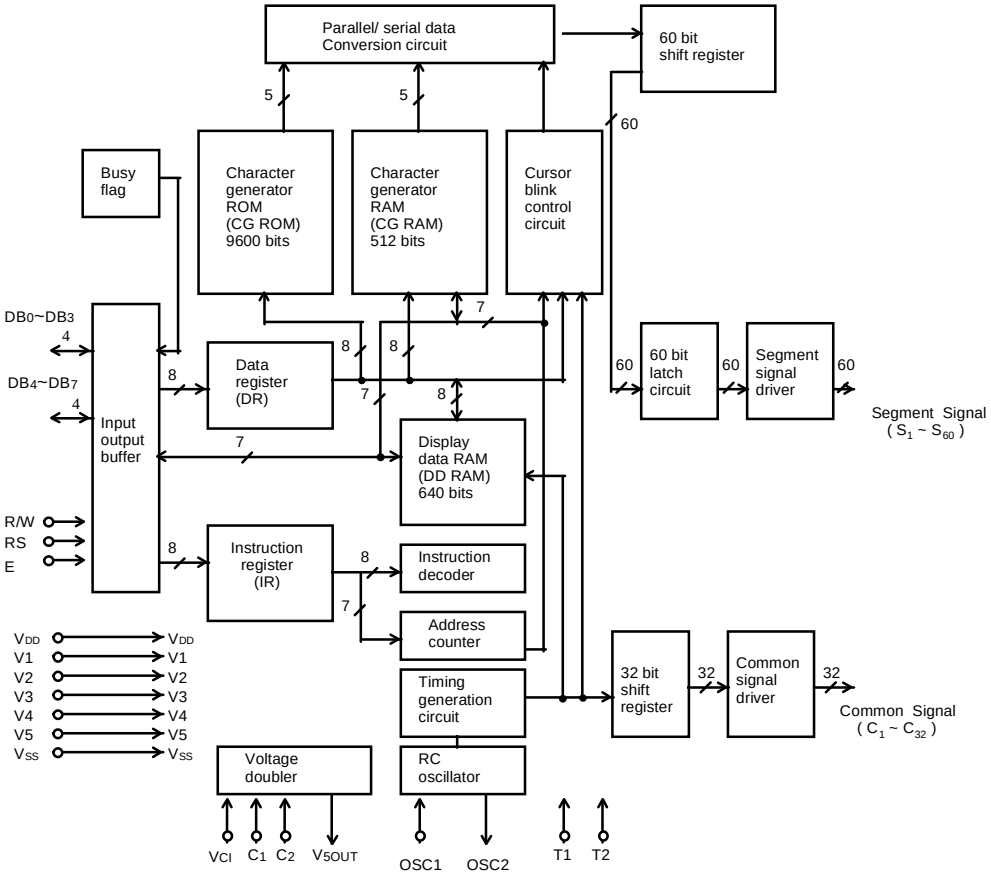
INTRODUCTION

The KS0071B is a dot matrix LCD controller & driver LSI which is fabricated by low power CMOS technology, designed to drive a split screen dot matrix LCD display of 1 line × 24 characters or 2 line × 24 characters with 5×7 dots format.

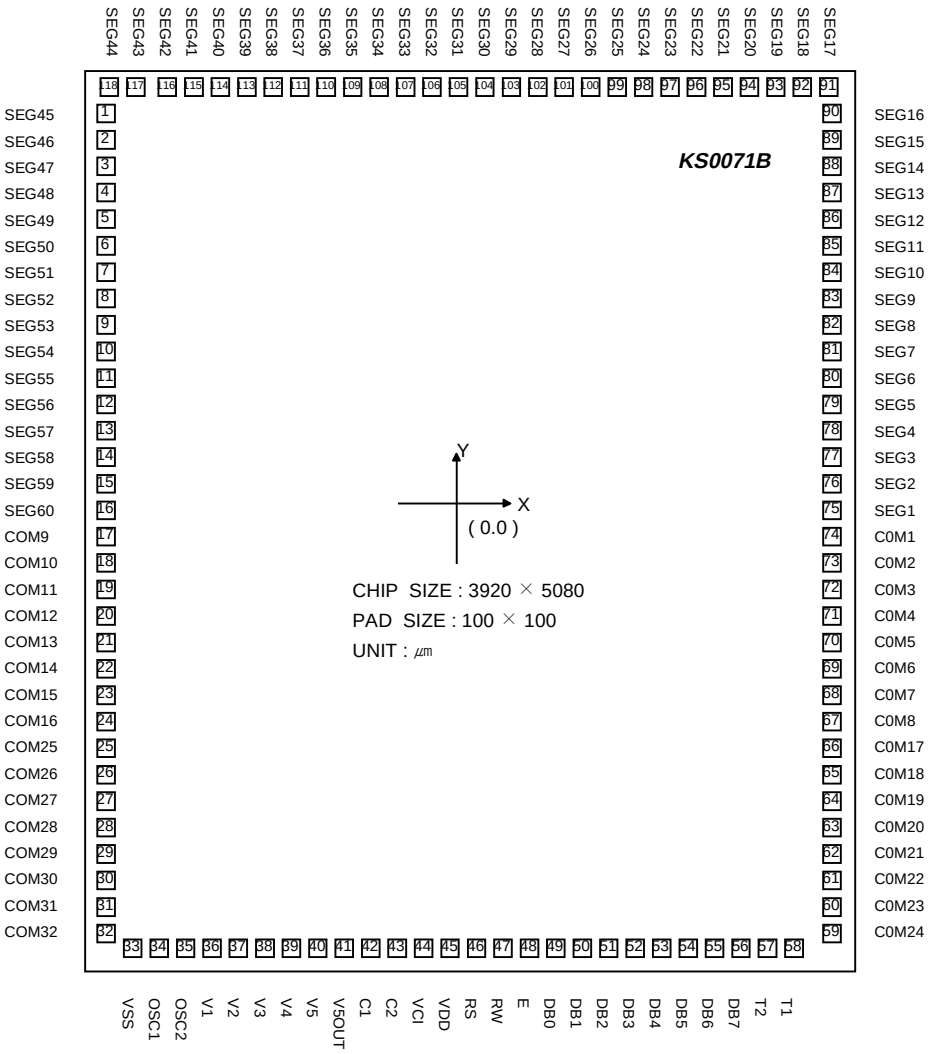
FEATURES

- Character type dot matrix single chip LCD controller & driver
- High voltage LCD driver 32 common and 60 segment signal output.
- Easy interface with a 4 bit or 8 bit MPU.
- Internal memory
  - -. Character generator ROM : 8400bits (240 characters for 5×7 dots)
  - -. Character generator RAM : 512 bits (8 patterns for 5×7 dots)
  - -. Display data RAM : 640 bits (80×8 bits for 80 characters)
- Maximum display characters
  - -. 1 line, 1/16 duty, 5×7 dots + cursor, 24 characters.
  - -. 2 line, 1/32 duty, 5×7 dots + cursor, 24 characters .
- A customer character pattern can be programmable by mask option.
- . The special character pattern can be programmable by character generator RAM directly.
- It is possible to read both character generator and display data RAM from MPU.
- Useful 11 code instruction set
- Automatic power on reset function
- On chip generation of LCD supply voltage from voltage doubler (external supply also possible)
- .Voltage doubler generates about double from single power supply (5V)
- High contrast display can be performed though the simple power supply circuits.
- On chip oscillator requires external resistor (external clock also possible)
- Power supply voltage: +5V±10%, +3V±20%
- Supply voltage for display: -5V
- Package outline: 118 TAB or bare chip available.

BLOCK DIAGRAM



PAD DIAGRAM



* “KS0071B” Marking : easy to find PAD No. 95

PAD LOCATION

UNIT :(㎛)

PAD NO.	PAD Name	Coordinate		PAD NO.	PAD Name	Coordinate		PAD NO.	PAD Name	Coordinate		PAD NO.	PAD Name	Coordinate	
		X	Y			X	Y			X	Y			X	Y
1	SEG45	-1794	2170	33	VSS	-1564.5	-2374	65	COM18	1794	-1330	97	SEG23	936	2374
2	SEG46	-1794	2030	34	OSC1	-1437.5	-2374	66	COM17	1794	-1190	98	SEG24	811	2374
3	SEG47	-1794	1890	35	OSC2	-1312.5	-2374	67	COM8	1794	-1050	99	SEG25	686	2374
4	SEG48	-1794	1750	36	V1	-1187.5	-2374	68	COM7	1794	-910	100	SEG26	561	2374
5	SEG49	-1794	1610	37	V2	-1062.5	-2374	69	COM6	1794	-770	101	SEG27	436	2374
6	SEG50	-1794	1470	38	V3	-937.5	-2374	70	COM5	1794	-630	102	SEG28	311	2374
7	SEG51	-1794	1330	39	V4	-812.5	-2374	71	COM4	1794	-490	103	SEG29	186	2374
8	SEG52	-1794	1190	40	V5	-687.5	-2374	72	COM3	1794	-350	104	SEG30	61	2374
9	SEG53	-1794	1050	41	V5OUT	-562.5	-2374	73	COM2	1794	-210	105	SEG31	-64	2374
10	SEG54	-1794	910	42	C1	-437.5	-2374	74	COM1	1794	-70	106	SEG32	-189	2374
11	SEG55	-1794	770	43	C2	-312.5	-2374	75	SEG1	1794	70	107	SEG33	-314	2374
12	SEG56	-1794	630	44	VCI	-187.5	-2374	76	SEG2	1794	210	108	SEG34	-439	2374
13	SEG57	-1794	490	45	VDD	-62.5	-2374	77	SEG3	1794	350	109	SEG35	-564	2374
14	SEG58	-1794	350	46	RS	62.5	-2374	78	SEG4	1794	490	110	SEG36	-689	2374
15	SEG59	-1794	210	47	RW	187.5	-2374	79	SEG5	1794	630	111	SEG37	-814	2374
16	SEG60	-1794	70	48	E	312.5	-2374	80	SEG6	1794	770	112	SEG38	- 939	2374
17	COM9	-1794	-70	49	DB0	437.5	-2374	81	SEG7	1794	910	113	SEG39	-1064	2374
18	COM10	-1794	-210	50	DB1	562.5	-2374	82	SEG8	1794	1050	114	SEG40	-1189	2374
19	COM11	-1794	-350	51	DB2	687.5	-2374	83	SEG9	1794	1190	115	SEG41	-1314	2374
20	COM12	-1794	-490	52	DB3	812.5	-2374	84	SEG10	1794	1330	116	SEG42	-1439	2374
21	COM13	-1794	-630	53	DB4	937.5	-2374	85	SEG11	1794	1470	117	SEG43	-1564	2374
22	COM14	-1794	-770	54	DB5	1062.5	-2374	86	SEG12	1794	1610	118	SEG44	-1689	2374
23	COM15	-1794	-910	55	DB6	1187.5	-2374	87	SEG13	1794	1750				
24	COM16	-1794	-1050	56	DB7	1312.5	-2374	88	SEG14	1794	1890				
25	COM25	-1794	-1190	57	T2	1437.5	-2374	89	SEG15	1794	2030				
26	COM26	-1794	-1330	58	T1	1562.5	-2374	90	SEG16	1794	2170				
27	COM27	-1794	-1470	59	COM24	1794	-2170	91	SEG17	1686	2374				
28	COM28	-1794	-1610	60	COM23	1794	-2030	92	SEG18	1561	2374				
29	COM29	-1794	-1750	61	COM22	1794	-1890	93	SEG19	1436	2374				
30	COM30	-1794	-1890	62	COM21	1794	-1750	94	SEG20	1311	2374				
31	COM31	-1794	-2030	63	COM20	1794	-1610	95	SEG21	1186	2374				
32	COM32	-1794	-2170	64	COM19	1794	-1470	96	SEG22	1061	2374				

PAD DESCRIPTION

PAD (No.)	NAME	I/O	Description	Interface
V_{DD} (45)	Power Supply	Input	For logical circuit (+5V±10%,+3V±20%)	Power supply
V_{SS} (33)			0V (GND)	
OSC1 (34) OSC2 (35)	Oscillator	Input output	OSC1 and OSC2 pin should be connected to external Rf resistor for internal oscillator. External clock can be input to OSC1.	Resistor or external clock
E (48)	Enable	Input	Start enable signal to read or write the data	MPU
R/W (47)	Read / write	Input	R/W signal input is used to select the read/write mode High: Read mode Low: Write mode	MPU
RS (46)	Register select	Input	Register select input. High: Data register (for read and write) Low: Instruction register (for write) busy flag, address counter (for read)	MPU
DB_0 ~ DB_7 (49 ~ 56)	Data interface	Input/ output	Used for data transfer between the MPU and KS0071B, These terminals are for data bus with bidirectional three-state. lower 4 bit (DB_0 ~ DB_3) are not used during 4 bit operation (DB_7 can be used as a busy flag.)	MPU
V_{CI} (44)	Voltage doubler output	Input	Input terminal for voltage doubler. (normally V_{CI}=V_{DD})	Power supply
C1 (42) C2 (43)	Capacitor	Input	Capacitor for voltage doubler connecting terminal (+). Capacitor for voltage doubler connecting terminal(-).	Capacitor
V_{5OUT} (41)	Voltage doubler output	Output	Voltage doubler output terminal connected to LCD supply voltage	V5
V1,V2,V3,V4,V5 (36 ~ 40)	LCD supply Voltage	Input	Bias voltage level for LCD driving	Divide resistor
S_1 ~ S_{44} (75~118) S_{45} ~ S_{60} (1 ~ 16)	Segment output	Output	Segment signal output for LCD driving	LCD
C_1 ~ C_8 (74 ~ 67) C_9 ~ C_{16} (17~24) C_{17} ~ C_{24} (66~59) C_{25} ~ C_{32} (25~32)	Common output	Output	Common signal output for LCD driving	LCD
T1(58),T2(57)	Test pin	Input	Maker testing terminal (normally open)	

MAXIMUM ABSOLUTE LIMIT

Description	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 ~ + 7.0	-
Driver Supply Voltage	V1 ~ V5	V_{DD}- 13.5 ~ V_{DD} + 0.3	-
Input Voltage	V_{IN}	- 0.3 ~ V_{DD} + 0.3	-
Power Dissipation	P_D	500	mW
Operating Temperature	T_{OPR}	- 30 ~ + 85	℃
Storage Temperature	T_{STG}	- 55 ~ + 125	℃

. Voltage greater than above may damage the circuit
. The voltage relation : $V_{DD} \geq V_{CI} \geq V_5 \geq V_{5OUT}$, $V_{DD} \geq V_{SS} \geq V_{5OUT}$, V_{SS} = 0V

ELECTRICAL CHARACTERISTICS

DC Characteristics

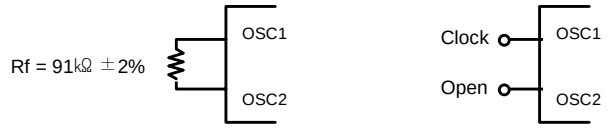
(V_{DD} = +5V±10%, V_{SS} = 0V, Ta = -30℃ ~ +85℃)

Characteristic		Symbol	Condition	Min	Typ	Max	Unit	Applicable pin
Operating voltage		V_{DD}	-	4.5	5.0	5.5	V	-
Supply current (*1)		I_{DD}	Internal oscillation or external clock V_{DD}=5V f_{OSC}=270KHz	-	0.6	1.0	mA	-
Input voltage 1	High	V_{IH1}	-	2.3	-	V_{DD}	V	E, DB_0 ~ DB_7, R/W, RS
	Low	V_{IL1}	-	-	-	0.8		
Input voltage 2	High	V_{IH2}	-	V_{DD}-1	-	V_{DD}		OSC1
	Low	V_{IL2}	-	-	-	1.0		
Output voltage 1	High	V_{OH1}	I_{OH}=-0.205mA	2.4	-	-	V	DB_0 ~ DB_7
	Low	V_{OL1}	I_{OL}=1.6mA	-	-	0.4		
Output voltage 2	High	V_{OH2}	I_O=-40uA	0.9V_{DD}	-	-		OSC2
	Low	V_{OL2}	I_O=40uA	-	-	0.1V_{DD}		
Voltage drop (*2)	COM	Vd_{COM}	I_O=±0.1mA	-	-	1	V	COM1 ~ COM32
	SEG	Vd_{SEG}		-	-	1		SEG1 ~ SEG60
Input Leakage Current		I_{IL1}	V_{IN}=0V or V_{DD}	-1	-	1	uA	E
		I_{IL2}	V_{IN}=V_{DD}	-5	-	5		RS, R/W, DB_0~DB_7
Low Input Current		I_{IN}	V_{IN}=0V, V_{DD}=5V (Test pull up R)	-50	-125	-250		
Internal Frequency (*3)		f_{lc}	Rf=91kΩ±2%	190	270	350	KHz	OSC1,OSC2
External clock (*4)	Frequency	f_{EC}	-	160	250	350		OSC1
	Duty	duty		45	50	55	%	
	Rise, Fall	tr, tf		-	-	0.2	μs	
Voltage doubler (*5)	Output Voltage	V_{5OUT}	I_{OUT}=5mA, Ta=25℃	-2.8	-3.9	-	V	V_{5OUT}
	Voltage		I_{OUT}=1mA, Ta=25℃	-4.5	-4.7	-		
	conv. rate	V_{EF}	RL=∞	95	99.9	-	%	
	Input Voltage	V_{CI}	-	2.5	-	5.5	V	V_{CI}
LCD driving voltage(*6)		V_{LCD}	V_{LCD}-V5 1/5 bias	3.0	-	13.5	V	V_1~V_5
			1/6.7 bias	3.0	-	13.5		

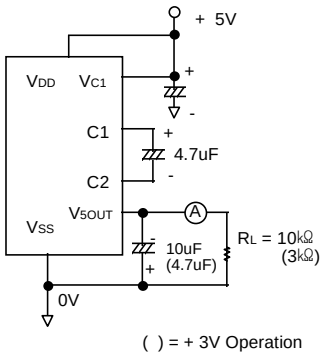
DC Characteristics (continued) (V_{DD} = +3V±20%, V_{SS} = 0V, Ta = -30℃ ~ +85℃)

Characteristic		Symbol	Condition	Min	Typ	Max	Unit	Applicable pin
Operating Voltage		V_{DD}	-	2.4	3.0	3.6	V	
Supply Current (*1)		I_{DD}	Internal oscillation or external clock V_{DD}=3V f_{OSC}=240 KHz	-	0.2	0.3	mA	
Input Voltage 1	High	V_{IH1}	-	0.8V_{DD}	-	V_{DD}	V	E, DB_0 ~ DB_7, R/W, RS
	Low	V_{IL1}	-	-	-	0.2V_{DD}		
Input Voltage 2	High	V_{IH2}	-	V_{DD}-1	-	V_{DD}		OSC1
	Low	V_{IL2}	-	-	-	1.0		
Output Voltage 1	High	V_{OH1}	I_{OH}=-0.205mA	2.0	-	-	V	DB_0 ~ DB_7
	Low	V_{OL1}	I_{OL}=1.6mA	-	-	0.5		
Output Voltage 2	High	V_{OH2}	I_O=-40uA	0.9V_{DD}	-	-		OSC2
	Low	V_{OL2}	I_O=40uA	-	-	0.1V_{DD}		
Voltage Drop (*2)	COM	Vd_{COM}	I_O=±0.1mA	-	-	1	V	COM_1 ~ COM_{32}
	SEG	Vd_{SEG}		-	-	1		SEG_1 ~ SEG_{60}
Input Leakage Current		I_{IL1}	V_{IN}=0V or V_{DD}	-1	-	1	uA	E
		I_{IL2}	V_{IN}=V_{DD}	-5	-	5		RS, R/W, DB_0~DB_7
Input Low Current		I_{IN}	V_{IN}=0V, V_{DD}=3V (Test pull up R)	-10	-25	-50		
Internal Clock Frequency (*3)		f_{ic}	Rf=91kΩ±2%	160	240	320	KHz	OSC1,OSC2
Voltage doubler (*5)	Output Voltage	V_{5OUT}	I_{OUT}=1mA, Ta=25℃	-2.5	-2.75	-	V	V_{5OUT}
	Voltage conv. rate	V_{EF}	RL=∞	95	99.9	-	%	
	Input voltage	V_{CI}	-	1.8	-	V_{DD}	V	V_{CI}
LCD driving voltage(*6)		V_{LCD}	V_{DD} - V5	3.0	-	12		V_1~V_5

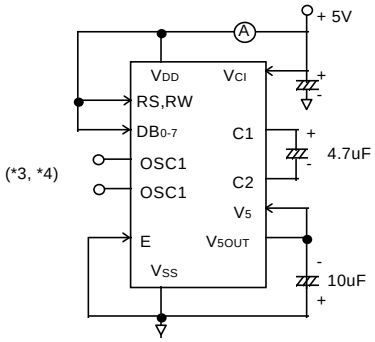
NOTE: *1) Applies to the current value flowing through VDD under the following conditions
(all input level must be fixed to 'H' or 'L')
* 2) Applies to COM voltage DROP (Vdcom) occurring from terminals V_{DD}, V_1,V_4 and V_5 to each common terminal (COM_1 ~ COM_{32}), and also to SEG voltage drop (Vd_{SEG}) occurring from terminals V_{DD}, V_2,V_3 and V_5 to each segment terminal (SEG1 ~ SEG60).
* 3) Internal clock * 4) External clock



* 4) Voltage doubler measuring circuit



* 5) Supply current measuring circuit



* 6) LCD driving voltage V_1, V_2, V_3,V_4, V_5 ($V_{LCD} = V_{DD} - V_5$)

Power	Duty	1/16 duty	1/32 duty
	Bias	1/5 bias	1/6.7 bias
V_{DD} (COM / SEG select voltage)		V_{DD}	V_{DD}
V_1 (COM non select voltage)		V_{DD}-(1/5) V_{LCD}	V_{DD}-(1/6.7) V_{LCD}
V_2 (SEG non select voltage)		V_{DD}-(2/5) V_{LCD}	V_{DD}-(2/6.7) V_{LCD}
V_3 (SEG non select voltage)		V_{DD}-(3/5) V_{LCD}	V_{DD}-(4.7/6.7) V_{LCD}
V_4 (COM non select voltage)		V_{DD}-(4/5) V_{LCD}	V_{DD}-(5.7/6.7) V_{LCD}
V_5 (COM / SEG select voltage)		V_{DD}-V_{LCD}	V_{DD}-V_{LCD}

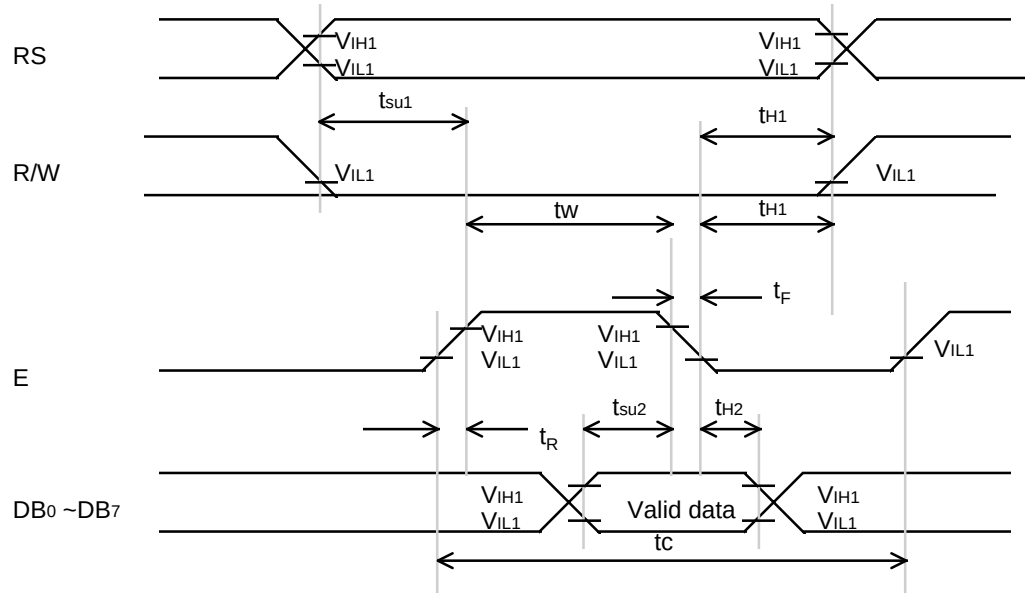
AC Characteristics

(1) Write mode (V_{DD} = 5V±10%, V_{SS} = 0V , Ta = -30℃ ~ +85℃)

Description	Symbol	Min	Typ	Max	Unit	Test Pin
Cycle Time	tc	500	-	-	ns	E
Rise Time / Fall Time	t_R, t_F	-	-	20	ns	E
Pulse Width (High, Low)	t_W	220	-	-	ns	E
R/W and RS Set-Up Time	t_{SU1}	40	-	-	ns	R/W, RS
R/W and RS Hold Time	t_{H1}	10	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	60	-	-	ns	DB_0 ~ DB_7
Data Hold Time	t_{H2}	10	-	-	ns	DB_0 ~ DB_7

(V_{DD} = 3V±20%, V_{SS} = 0V , Ta = -30℃ ~ +85℃)

Description	Symbol	Min	Typ	Max	Unit	Test Pin
Cycle Time	t_C	1400	-	-	ns	E
Rise Time / Fall Time	t_R, t_F	-	-	20	ns	E
Pulse Width (High, Low)	t_W	500	-	-	ns	E
R/W And RS Set-Up Time	t_{SU1}	70	-	-	ns	R/W, RS
R/W And RS Hold Time	t_{H1}	10	-	-	ns	R/W, RS
Data Set-Up Time	t_{SU2}	195	-	-	ns	DB_0 ~ DB_7
Data Hold Time	t_{H2}	10	-	-	ns	DB_0 ~ DB_7

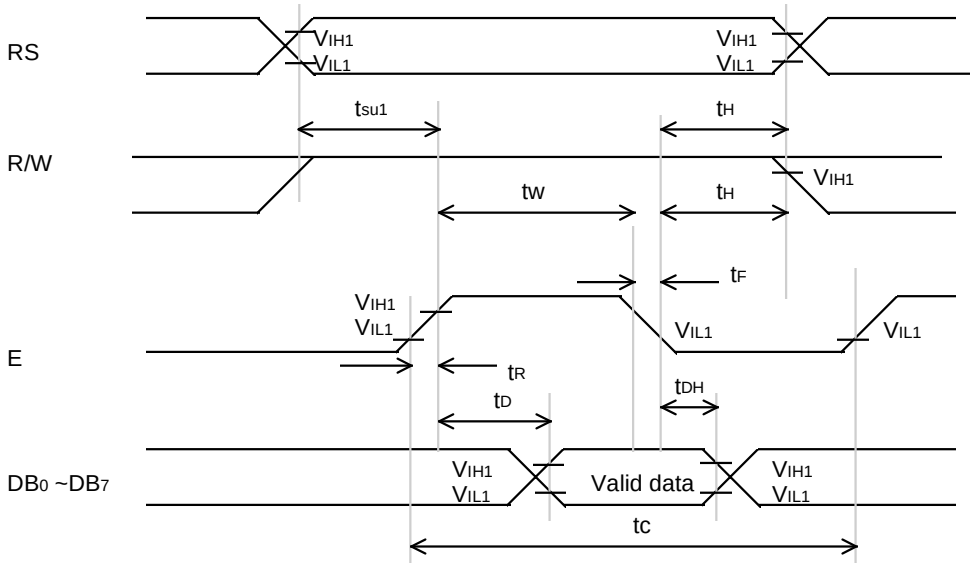


(2) Read mode (V_{DD} = 5V±10%, V_{SS} = 0V , Ta = -30℃ ~ +85℃)

Description	Symbol	Min	Typ	Max	Unit	Test Pin
E Cycle Time	t_C	500	-	-	ns	E
Rise Time / Fall Time	t_R, t_F	-	-	20	ns	E
E Pulse Width	t_W	220	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	40	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	10	-	-	ns	R/W, RS
Data Output Delay Time	t_D	-	-	120	ns	DB_0 ~ DB_7
Data Hold Time	t_{DH}	10	-	-	ns	DB_0 ~ DB_7

(V_{DD} = 3V±20%, V_{SS} = 0V , Ta = -30℃ ~ +85℃)

Description	Symbol	Min	Typ	Max	Unit	Test Pin
E Cycle Time	t_C	1400	-	-	ns	E
Rise Time / Fall Time	t_R, t_F	-	-	20	ns	E
E Pulse Width	t_W	500	-	-	ns	E
R/W And RS Set-Up Time	t_{SU}	70	-	-	ns	R/W, RS
R/W And RS Hold Time	t_H	10	-	-	ns	R/W, RS
Data output Delay Time	t_D	-	-	600	ns	DB_0 ~ DB_7
Data Hold Time	t_{DH}	20	-	-	ns	DB_0 ~ DB_7



CONTROL and DISPLAY COMMAND

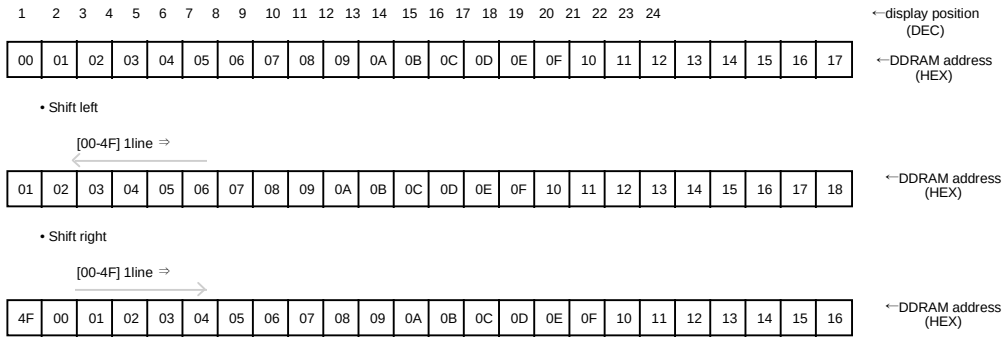
Command	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Execution time f_{OSC}=250KHz	Remark
Display clear	L	L	L	L	L	L	L	L	L	H	1.64mS	
Return home	L	L	L	L	L	L	L	L	H	X	1.64mS	Cursor move to first digit
Entry mode set	L	L	L	L	L	L	L	H	I/D	SH	40uS	I/D: Set cursor move direction I/D H Increase I/D L Decrease SH: Specifies shift of display SH H Display is shifted SH L Display is not shifted
Display on/off	L	L	L	L	L	L	H	D	C	B	40uS	Display D H Display on D L Display off Cursor C H Cursor on C L Cursor off Blinking B H Blinking on B L Blinking off
Shift	L	L	L	L	L	H	S/C	R/L	X	X	40uS	S/C H Display shift S/C L Cursor move R/L H Right shift R/L L Left shift
Set function	L	L	L	L	H	DL	N	X	X	X	40uS	DL H 8 bits interface DL L 4 bits interface N H 2 line display N L 1line display
Set CG RAM address	L	L	L	H	CG RAM address (corresponds to cursor address)						40uS	CG RAM data is sent and received after this setting
Set DD RAM address	L	L	H	DD RAM address							40uS	DD RAM data is sent and received after this setting
Read busy flag & address	L	H	BF	Address counter used for both DD & CG RAM address							0uS	BF H Busy BF L Ready - Reads BF indication internal operating performed - Reads address counter contents
Write data	H	L	Write data								46uS	Write data into DD or CG RAM
Read data	H	H	Read data								46uS	Read data into DD or CG RAM

X : don't care

DISPLAY MODE DESCRIPTION

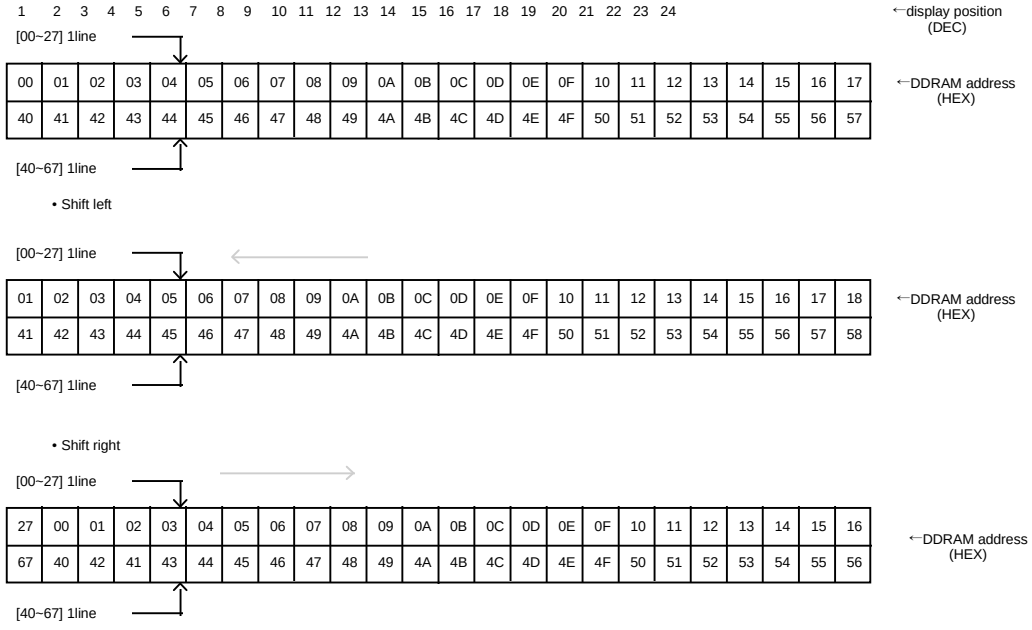
1) 1 Line Max. 24 character display (function set N=L)

• Normal DDRAM(HEX) line



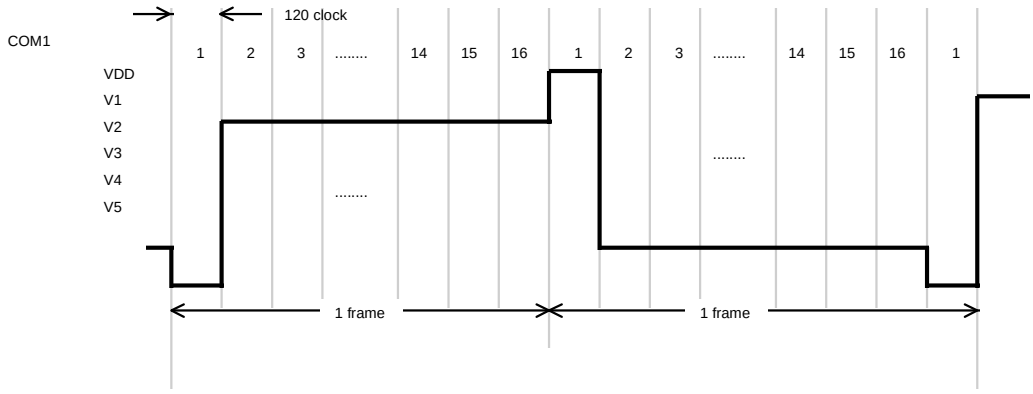
2) 2 Line Max. 24 character display (function set N=H)

• Normal DDRAM(HEX) line



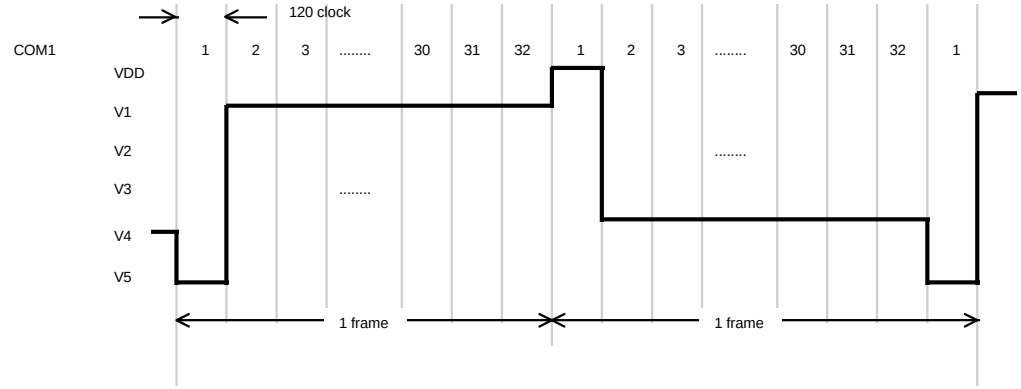
3) RELATION BETWEEN OSCILLATION FREQUENCY and LCD FRAME FREQUENCY

a) 1/16 duty



* One clock = 4 μs (Fosc = 250 kHz)
* Latch clock = 120 clock = 4 μs × 120 = 480μs , Frequency = 2.08 kHz
* One frame = 4 μs × 120 × 16 = 7,680μs = 7.68 ms
* Frame frequency = 1/7.68ms = 130.2 Hz

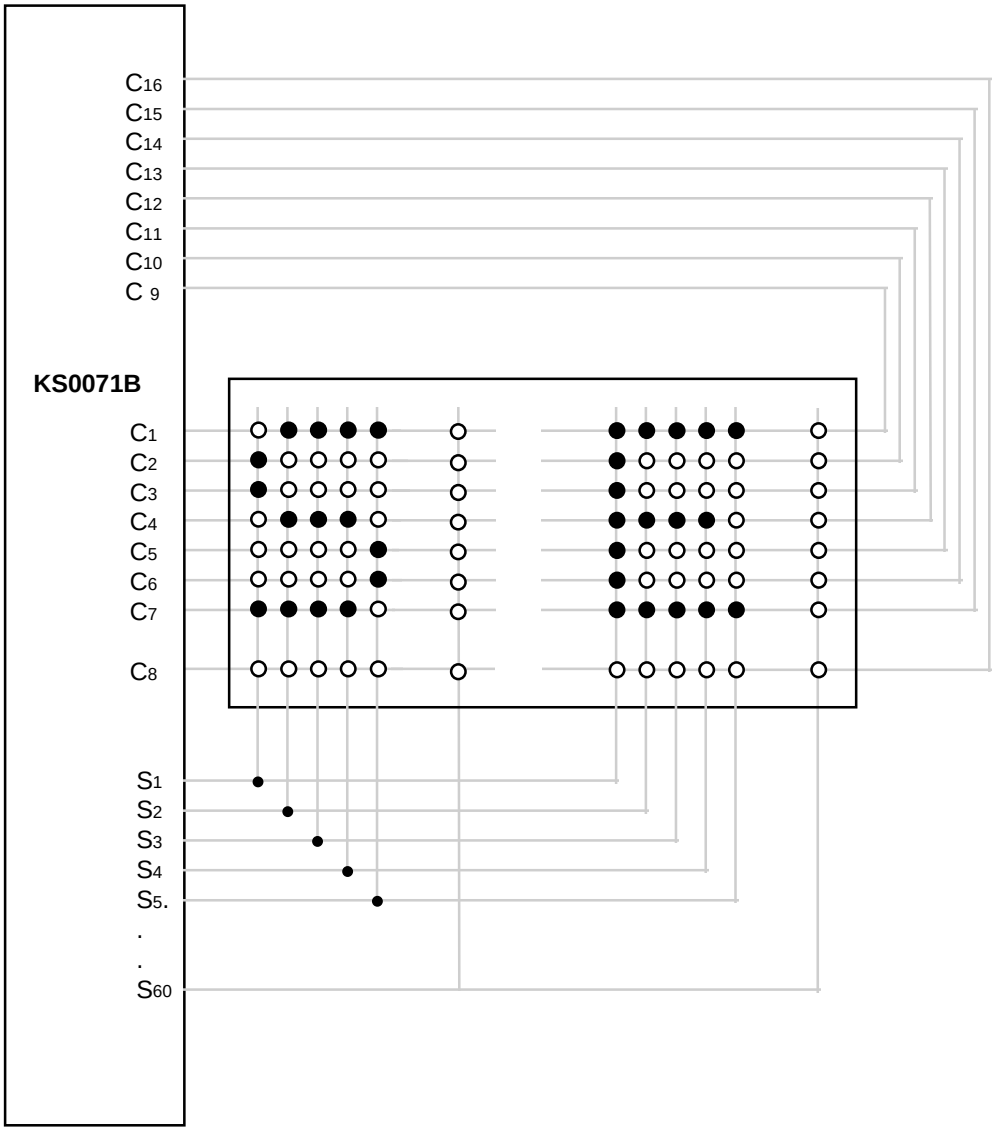
b) 1/32 duty



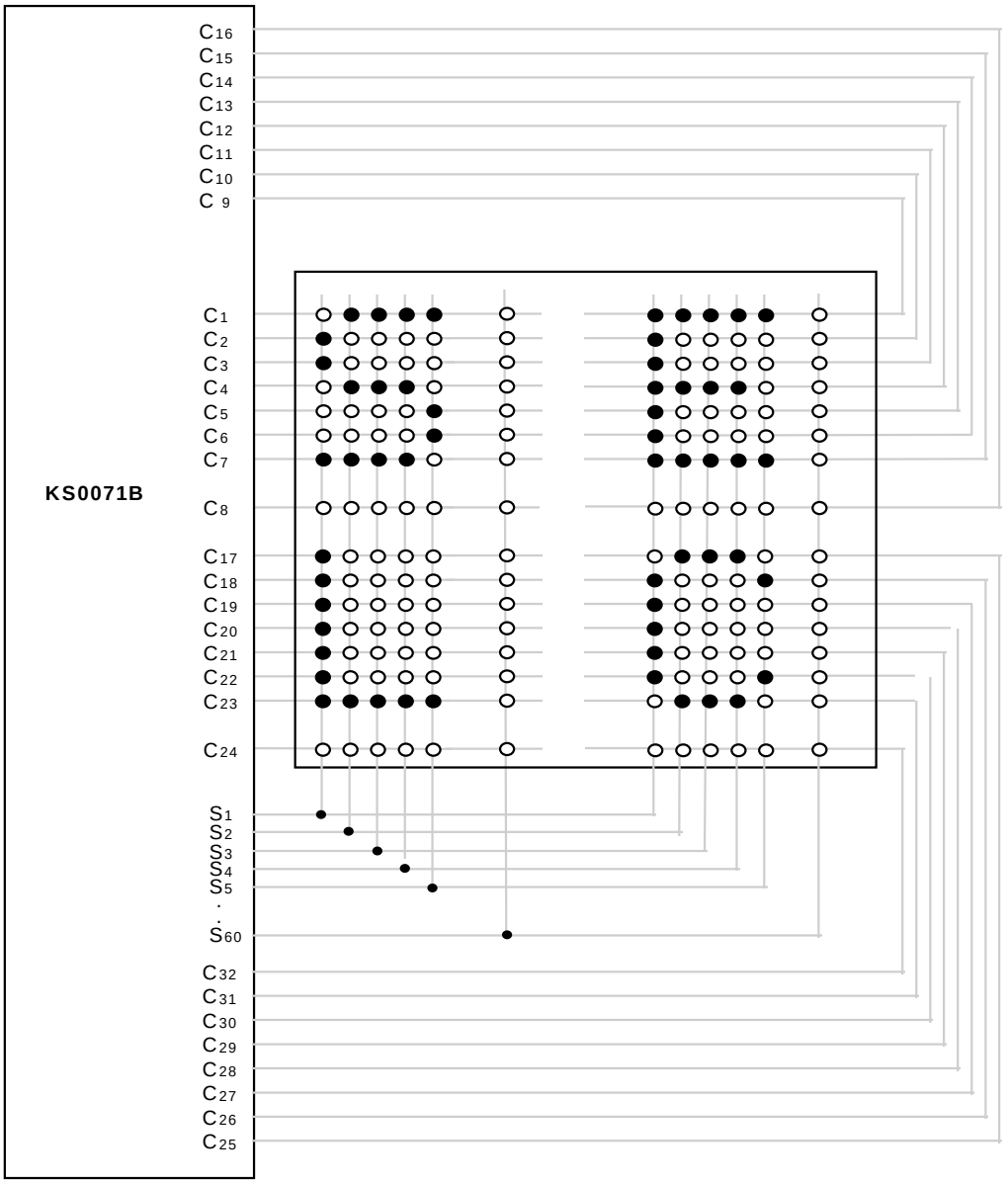
* One clock = 4 μs (Fosc = 250 kHz)
* Latch clock = 120 clock = 4 μs × 120 = 480 μs, Frequency = 2.08 kHz
* One frame = 4 μs × 120 × 32 = 15,360 μs = 15.36 ms
* Frame frequency = 1/15.36 ms = 65.1 Hz

APPLICATION INFORMATION

1) LCD panel: 24 character ×1 line character format: 5×7 dots + cursor line (1/5 bias, 1/16 duty)

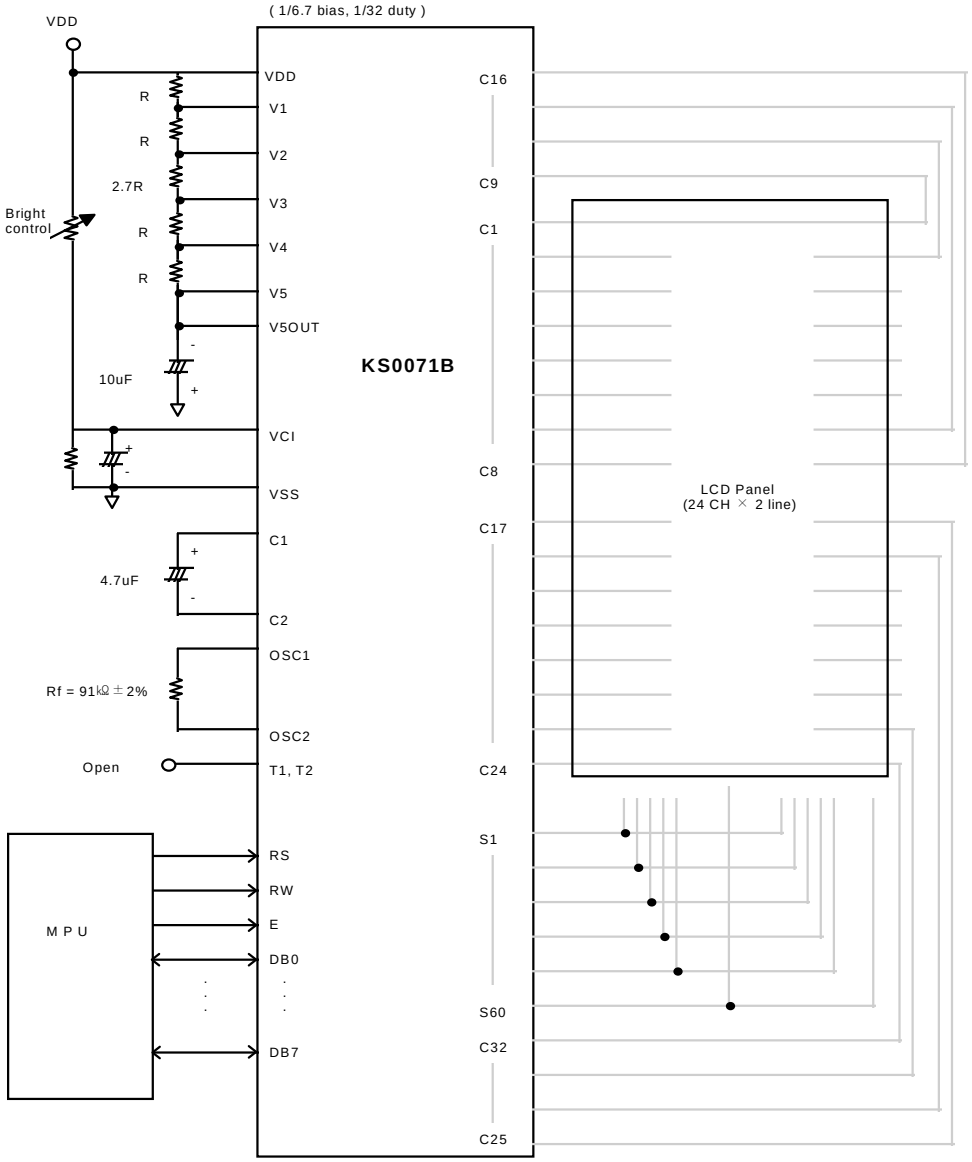


2) LCD panel: 24 character × 2 line character format: 5×7 dots + cursor line (1/6.7 bias, 1/32 duty)

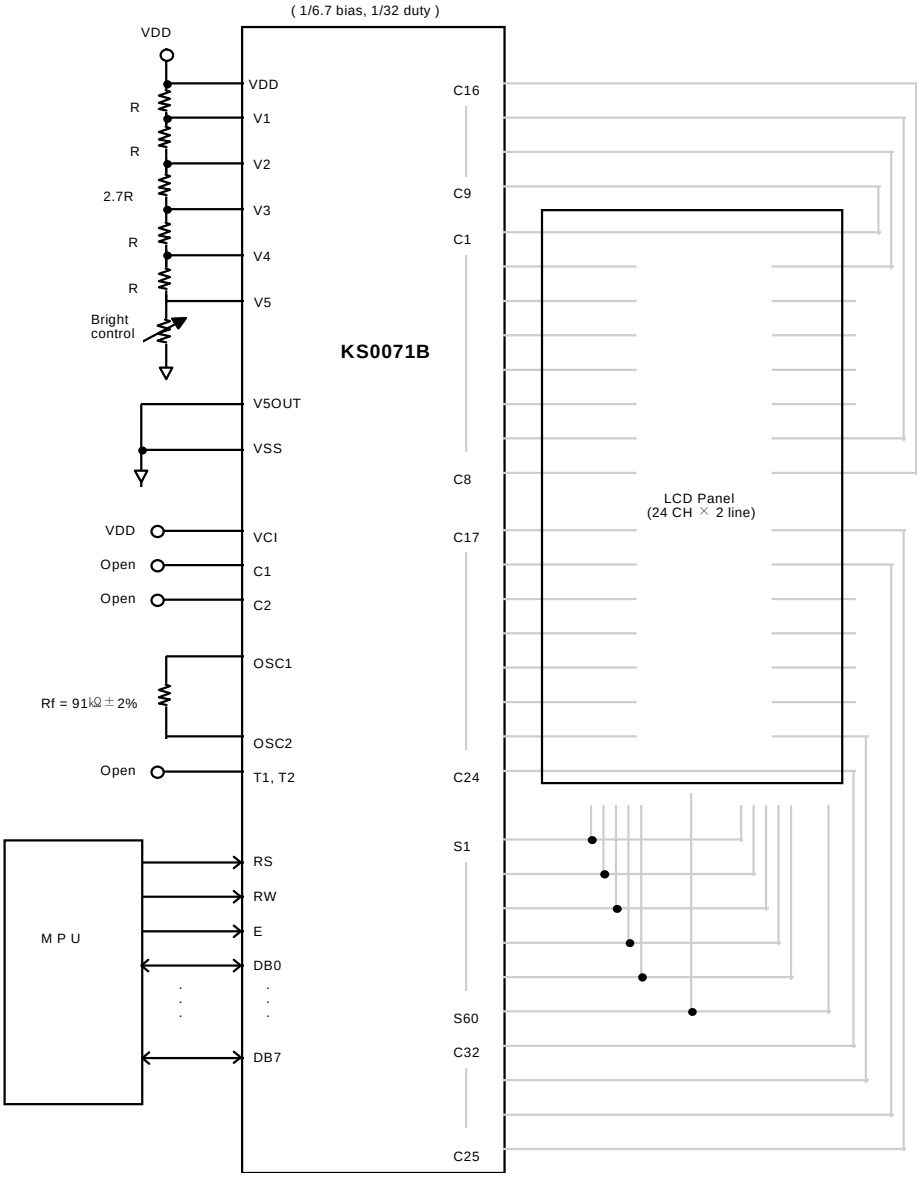


APPLICATION CIRCUIT

1) LCD driving voltage is generated by KS0071B (voltage doubler)



2) LCD driving voltage is supplied from external power supply



Standard Character Pattern (KS0071B-00)