KS0711

65 COM / 132 SEG DRIVER & CONTROLLER FOR 4G/S STN LCD

March. 1999.

KS0711 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	
1.0	Only FRC Method(For 4-level Gray Scale) → 3/4 FRC + 15/12/9 PWM(For 4-level Gray Scale) TEST0 Pin → REF Pin (For Reference Voltage Select) BSTS Pin → OSCCK Pin(Oscillator Clock) TEST3 Pin → VEXT Pin(External Reference Voltage) TEST4 Pin → REXT1 Pin(Resistor Pin For Oscillation) TEST5 Pin → REXT2 Pin(Resistor Pin For Oscillation) TEST6 Pin → TEST3 Pin TEST7 Pin → TEST4 Pin TEST8 Pin → TEST5 Pin	1998.
1.1	Vref & fosc: TBD → fixed Value(page27,47) IDDS2 : 10uA → 20uA(page48) Bumped Pad Height : 18um → 17um(page6) VDD : 2.7V → 2.4V(page47)	1998.7
2.0	Vref temperature coefficient : -0.05%,0.1%,0.15%,0.2% selectable by TEMPS0/1 pin status → -0.05%,0.2% selectable by product code Modify COMS output signal : COM[32],COM[48],COM[64] → COMS Voltage regulator (1+Rb/Ra) ratio : 5.5 → 5.4 Instruction description for LCD bias select : When bias=0, 1/9 bias(1/65 duty), 1/8 bias(1/49 duty), 1/6 bias(1/33 duty), → 1/7 bias(1/65 duty), 1/6 bias(1/49 duty), 1/5 bias(1/33 duty), When bias=1, 1/7 bias(1/65 duty), 1/6 bias(1/49 duty), 1/5 bias(1/33 duty), → 1/9 bias(1/65 duty), 1/8 bias(1/49 duty), 1/6 bias(1/33 duty) HPM Pin → HPMB Pin	1999.3

CONTENTS

INTRODUCTION

The KS0711 is an LCD driver LSI for liquid crystal dot-matrix graphic display systems. It incorporates 198 driver circuit for 132 segments, 64 commons and a common to drive icons, 65¡ 1 32¡ 2-bit bit-map RAM, and 4-level gray scale controller for enhanced graphics. It is capable of interfacing the microprocessor, accepting serial or 8-bit parallel display data directly from microprocessor, and storing data in an on-chip display data RAM. In addition, the KS0711 can read and write Display Data RAM with minimum current consumption as it does not require any external operation clocks, it also has an LCD driving voltage generation circuits such as the voltage converter, voltage regulator and voltage follower to save power consumption.

FEATURES

4-level (white, light gray, dark gray, black) gray scale display 9/12/15 PWM and 3/4 FRC method

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

(Accessible Column Address, n = 0, 1, 2, …..., 129, 130,131)

Driver output circuits

– 65 common outputs / 132 segment outputs

On-chip display data RAM

– Capacity: 65 x 132 x 2 = 17,160 bits

Multi-chip operation (Master, Slave) available

Applicable duty-ratios

Duty Ratio	Applicable LCD Bias	Maximum Display Area
1/65	1/9 or 1/7	65 × 132
1/49	1/8 or 1/6	49 × 132
1/33	1/6 or 1/5	33 × 132

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

On-chip oscillator circuit

On-chip low power supply for LCD driving voltage generation

– Voltage converter (x2, x3, x4, x5)
– Voltage regulator (temperature coefficient: -0.05%/°C, -0.2%/°C)
– Voltage follower
– Electronic contrast control functions (64 steps)

Operating voltage range

– Supply voltage (V_{DD}): 2.4 to 5.5 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low power consumption

– 150 ㎂ max. (Operation)
– 20 ㎂ max. (Standby Mode)

Wide operating temperature range

– Ta = -40°C to 85 °C

Package Type

– Slim chip for COG, and TCP available

Series Specifications

COG product code	TCP product code	Temp. Coefficient	REMARKS
KS0711UM-L0CC	KS0711TB-XX-L0TF	-0.05%/°C	BSG = 675 µm
KS0711UM-L4CC	KS0711TB-XX-L4TF		BSG = 475 µm
KS0711UM-H0CC	KS0711TB-XX-H0TF	-0.2%/°C	BSG = 675 µm
KS0711UM-H4CC	KS0711TB-XX-H4TF		BSG = 475 µm

* XX: TCP ordering

BLOCK DIAGRAM

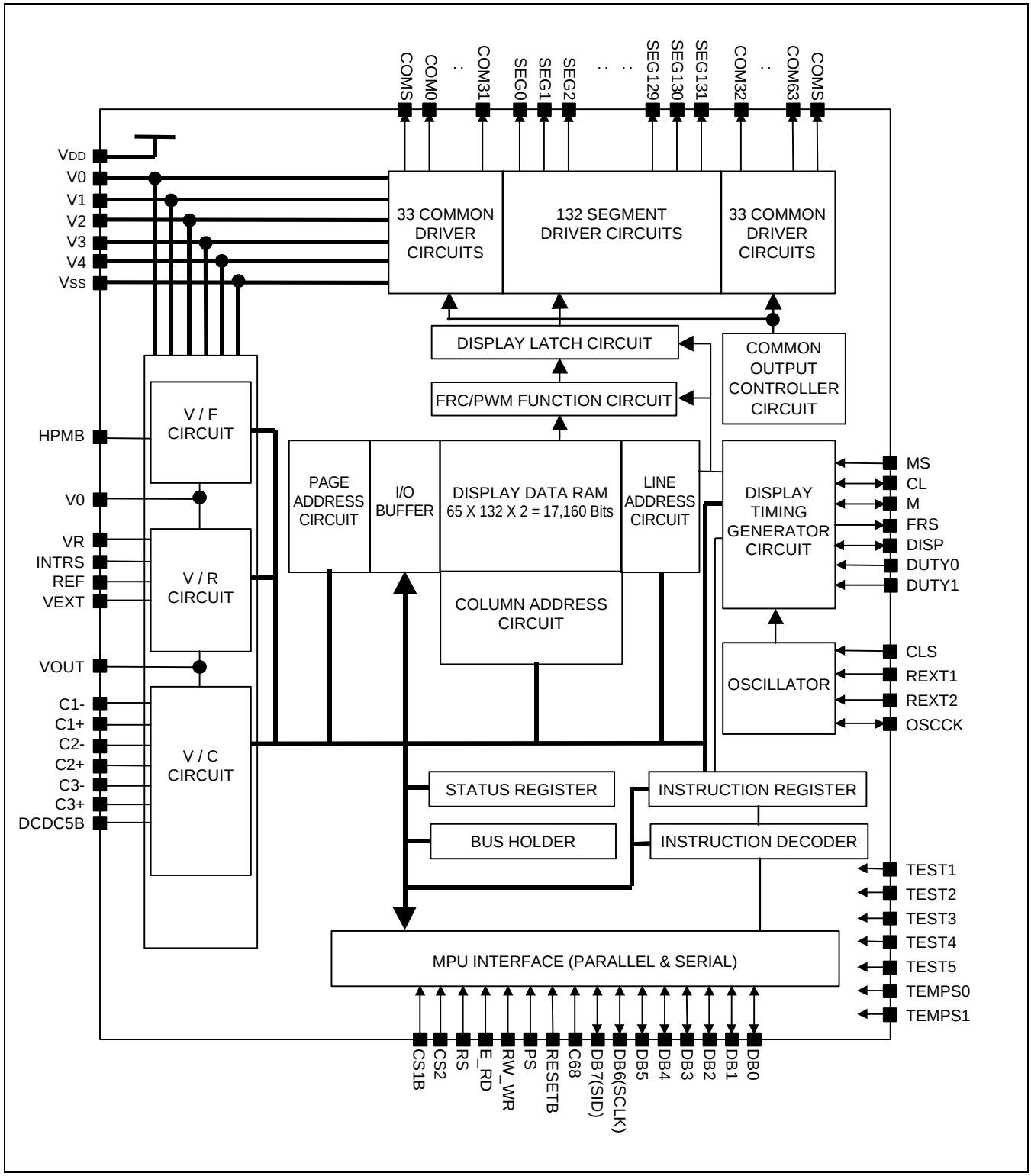


Figure 1. Block Diagram

PAD CONFIGURATION

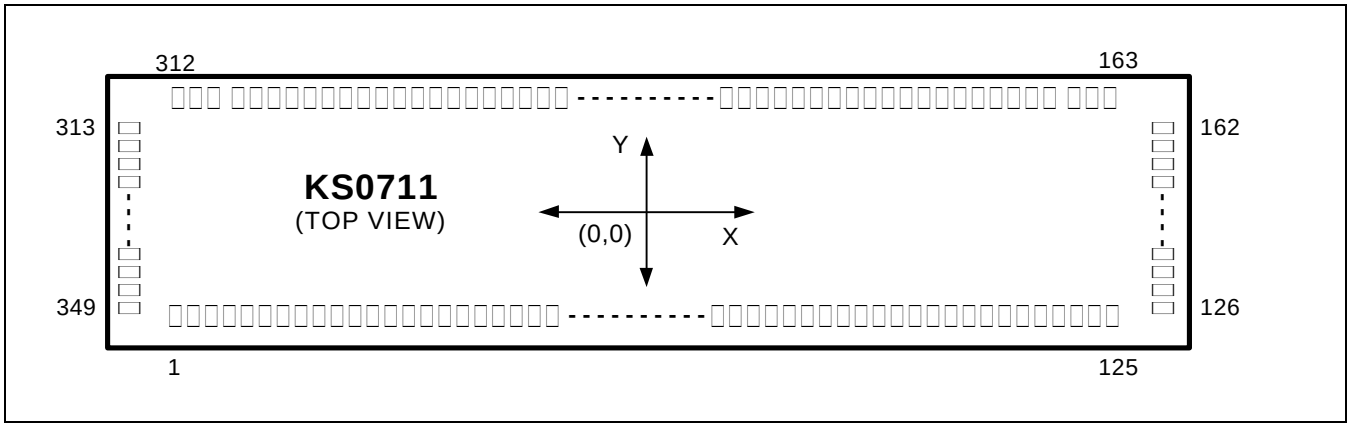


Figure 2. KS0711 Chip Configuration

Table 1. KS0711 Pad Dimensions

ITEM	PAD NO.	SIZE		UNIT
		X	Y	
CHIP SIZE	-	11690	3420	㎛
PAD PITCH	1 to 125	90		
	126 to 349	70		
BUMPED PAD SIZE	1 to 125	56	114	
	126 to 162	108	50	
	163 to 312	50	108	
	313 to 349	108	50	
BUMPED PAD HEIGHT	1 to 349	17 (TYP)		

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[unit: ㎛]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-5580	-1586	51	V_{SS}	-1080	-1586	101	V3	3420	-1586
2	DUMMY	-5490	-1586	52	V_{SS}	-990	-1586	102	V3	3510	-1586
3	DUMMY	-5400	-1586	53	V_{DD}	-900	-1586	103	V4	3600	-1586
4	DUMMY	-5310	-1586	54	V_{DD}	-810	-1586	104	V4	3690	-1586
5	FRS	-5220	-1586	55	V_{DD}	-720	-1586	105	V_{SS}	3780	-1586
6	M	-5130	-1586	56	V_{DD}	-630	-1586	106	V_{SS}	3870	-1586
7	CL	-5040	-1586	57	V_{DD}	-540	-1586	107	OSCCK	3960	-1586
8	DISP	-4950	-1586	58	V_{DD}	-450	-1586	108	DCDC5B	4050	-1586
9	V_{SS}	-4860	-1586	59	V_{DD}	-360	-1586	109	V_{DD}	4140	-1586
10	CS1B	-4770	-1586	60	V_{DD}	-270	-1586	110	HPMB	4230	-1586
11	CS2	-4680	-1586	61	VOUT	-180	-1586	111	INTRS	4320	-1586
12	V_{DD}	-4590	-1586	62	VOUT	-90	-1586	112	V_{SS}	4410	-1586
13	RESETB	-4500	-1586	63	VOUT	0	-1586	113	TEMP0	4500	-1586
14	RS	-4410	-1586	64	VOUT	90	-1586	114	TEMP1	4590	-1586
15	V_{SS}	-4320	-1586	65	C3+	180	-1586	115	V_{DD}	4680	-1586
16	RW_WR	-4230	-1586	66	C3+	270	-1586	116	REXT1	4770	-1586
17	E_RD	-4140	-1586	67	C3+	360	-1586	117	REXT2	4860	-1586
18	V_{DD}	-4050	-1586	68	C3+	450	-1586	118	V_{SS}	4950	-1586
19	C68	-3960	-1586	69	C3-	540	-1586	119	TEST3	5040	-1586
20	PS	-3870	-1586	70	C3-	630	-1586	120	TEST4	5130	-1586
21	V_{SS}	-3780	-1586	71	C3-	720	-1586	121	TEST5	5220	-1586
22	REF	-3690	-1586	72	C3-	810	-1586	122	DUMMY	5310	-1586
23	DUMMY	-3600	-1586	73	C1+	900	-1586	123	DUMMY	5400	-1586
24	DUMMY	-3510	-1586	74	C1+	990	-1586	124	DUMMY	5490	-1586
25	V_{DD}	-3420	-1586	75	C1+	1080	-1586	125	DUMMY	5580	-1586
26	DB0	-3330	-1586	76	C1+	1170	-1586	126	DUMMY	5669	-1330
27	DB1	-3240	-1586	77	C1-	1260	-1586	127	DUMMY	5669	-1260
28	DB2	-3150	-1586	78	C1-	1350	-1586	128	DUMMY	5669	-1190
29	DB3	-3060	-1586	79	C1-	1440	-1586	129	COMS	5669	-1120
30	DB4	-2970	-1586	80	C1-	1530	-1586	130	COM0	5669	-1050
31	DB5	-2880	-1586	81	C2+	1620	-1586	131	COM1	5669	-980
32	DB6	-2790	-1586	82	C2+	1710	-1586	132	COM2	5669	-910
33	DB7	-2700	-1586	83	C2+	1800	-1586	133	COM3	5669	-840
34	V_{SS}	-2610	-1586	84	C2+	1890	-1586	134	COM4	5669	-770
35	TEST1	-2520	-1586	85	C2-	1980	-1586	135	COM5	5669	-700
36	TEST2	-2430	-1586	86	C2-	2070	-1586	136	COM6	5669	-630
37	V_{DD}	-2340	-1586	87	C2-	2160	-1586	137	COM7	5669	-560
38	DUTY0	-2250	-1586	88	C2-	2250	-1586	138	COM8	5669	-490
39	DUTY1	-2160	-1586	89	V_{SS}	2340	-1586	139	COM9	5669	-420
40	V_{SS}	-2070	-1586	90	V_{SS}	2430	-1586	140	COM10	5669	-350
41	MS	-1980	-1586	91	VR	2520	-1586	141	COM11	5669	-280
42	CLS	-1890	-1586	92	VR	2610	-1586	142	COM12	5669	-210
43	V_{DD}	-1800	-1586	93	V0	2700	-1586	143	COM13	5669	-140
44	VEXT	-1710	-1586	94	V0	2790	-1586	144	COM14	5669	-70
45	V_{SS}	-1620	-1586	95	V0	2880	-1586	145	COM15	5669	0
46	V_{SS}	-1530	-1586	96	V0	2970	-1586	146	COM16	5669	70
47	V_{SS}	-1440	-1586	97	V1	3060	-1586	147	COM17	5669	140
48	V_{SS}	-1350	-1586	98	V1	3150	-1586	148	COM18	5669	1301
49	V_{SS}	-1260	-1586	99	V2	3240	-1586	149	COM19	5669	1301
50	V_{SS}	-1170	-1586	100	V2	3330	-1586	150	COM20	5669	1301

Table 2. Pad Center Coordinates (Continued)

[unit: mm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	COM21	5669	420	201	SEG29	2555	1534	251	SEG79	-945	1534
152	COM22	5669	490	202	SEG30	2485	1534	252	SEG80	-1015	1534
153	COM23	5669	560	203	SEG31	2415	1534	253	SEG81	-1085	1534
154	COM24	5669	630	204	SEG32	2345	1534	254	SEG82	-1155	1534
155	COM25	5669	700	205	SEG33	2275	1534	255	SEG83	-1225	1534
156	COM26	5669	770	206	SEG34	2205	1534	256	SEG84	-1295	1534
157	COM27	5669	840	207	SEG35	2135	1534	257	SEG85	-1365	1534
158	COM28	5669	910	208	SEG36	2065	1534	258	SEG86	-1435	1534
159	COM29	5669	980	209	SEG37	1995	1534	259	SEG87	-1505	1534
160	COM30	5669	1050	210	SEG38	1925	1534	260	SEG88	-1575	1534
161	COM31	5669	1120	211	SEG39	1855	1534	261	SEG89	-1645	1534
162	DUMMY	5669	1190	212	SEG40	1785	1534	262	SEG90	-1715	1534
163	DUMMY	5215	1534	213	SEG41	1715	1534	263	SEG91	-1785	1534
164	DUMMY	5145	1534	214	SEG42	1645	1534	264	SEG92	-1855	1534
165	DUMMY	5075	1534	215	SEG43	1575	1534	265	SEG93	-1925	1534
166	DUMMY	5005	1534	216	SEG44	1505	1534	266	SEG94	-1995	1534
167	DUMMY	4935	1534	217	SEG45	1435	1534	267	SEG95	-2065	1534
168	DUMMY	4865	1534	218	SEG46	1365	1534	268	SEG96	-2135	1534
169	DUMMY	4795	1534	219	SEG47	1295	1534	269	SEG97	-2205	1534
170	DUMMY	4725	1534	220	SEG48	1225	1534	270	SEG98	-2275	1534
171	DUMMY	4655	1534	221	SEG49	1155	1534	271	SEG99	-2345	1534
172	SEG0	4585	1534	222	SEG50	1085	1534	272	SEG100	-2415	1534
173	SEG1	4515	1534	223	SEG51	1015	1534	273	SEG101	-2485	1534
174	SEG2	4445	1534	224	SEG52	945	1534	274	SEG102	-2555	1534
175	SEG3	4375	1534	225	SEG53	875	1534	275	SEG103	-2625	1534
176	SEG4	4305	1534	226	SEG54	805	1534	276	SEG104	-2695	1534
177	SEG5	4235	1534	227	SEG55	735	1534	277	SEG105	-2765	1534
178	SEG6	4165	1534	228	SEG56	665	1534	278	SEG106	-2835	1534
179	SEG7	4095	1534	229	SEG57	595	1534	279	SEG107	-2905	1534
180	SEG8	4025	1534	230	SEG58	525	1534	280	SEG108	-2975	1534
181	SEG9	3955	1534	231	SEG59	455	1534	281	SEG109	-3045	1534
182	SEG10	3885	1534	232	SEG60	385	1534	282	SEG110	-3115	1534
183	SEG11	3815	1534	233	SEG61	315	1534	283	SEG111	-3185	1534
184	SEG12	3745	1534	234	SEG62	245	1534	284	SEG112	-3255	1534
185	SEG13	3675	1534	235	SEG63	175	1534	285	SEG113	-3325	1534
186	SEG14	3605	1534	236	SEG64	105	1534	286	SEG114	-3395	1534
187	SEG15	3535	1534	237	SEG65	35	1534	287	SEG115	-3465	1534
188	SEG16	3465	1534	238	SEG66	-35	1534	288	SEG116	-3535	1534
189	SEG17	3395	1534	239	SEG67	-105	1534	289	SEG117	-3605	1534
190	SEG18	3325	1534	240	SEG68	-175	1534	290	SEG118	-3675	1534
191	SEG19	3255	1534	241	SEG69	-245	1534	291	SEG119	-3745	1534
192	SEG20	3185	1534	242	SEG70	-315	1534	292	SEG120	-3815	1534
193	SEG21	3115	1534	243	SEG71	-385	1534	293	SEG121	-3885	1534
194	SEG22	3045	1534	244	SEG72	-455	1534	294	SEG122	-3955	1534
195	SEG23	2975	1534	245	SEG73	-525	1534	295	SEG123	-4025	1534
196	SEG24	2905	1534	246	SEG74	-595	1534	296	SEG124	-4095	1534
197	SEG25	2835	1534	247	SEG75	-665	1534	297	SEG125	-4165	1534
198	SEG26	2765	1534	248	SEG76	-735	1534	298	SEG126	-4235	1534
199	SEG27	2695	1534	249	SEG77	-805	1534	299	SEG127	-4305	1534
200	SEG28	2625	1534	250	SEG78	-875	1534	300	SEG128	-4375	1534

Table 2. Pad Center Coordinates (Continued)

[unit: mm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SEG129	-4445	1534								
302	SEG130	-4515	1534								
303	SEG131	-4585	1534								
304	DUMMY	-4655	1534								
305	DUMMY	-4725	1534								
306	DUMMY	-4795	1534								
307	DUMMY	-4865	1534								
308	DUMMY	-4935	1534								
309	DUMMY	-5005	1534								
310	DUMMY	-5075	1534								
311	DUMMY	-5145	1534								
312	DUMMY	-5215	1534								
313	DUMMY	-5669	1190								
314	COMS	-5669	1120								
315	COM63	-5669	1050								
316	COM62	-5669	980								
317	COM61	-5669	910								
318	COM60	-5669	840								
319	COM59	-5669	770								
320	COM58	-5669	700								
321	COM57	-5669	630								
322	COM56	-5669	560								
323	COM55	-5669	490								
324	COM54	-5669	420								
325	COM53	-5669	350								
326	COM52	-5669	280								
327	COM51	-5669	210								
328	COM50	-5669	140								
329	COM49	-5669	70								
330	COM48	-5669	0								
331	COM47	-5669	-70								
332	COM46	-5669	-140								
333	COM45	-5669	-210								
334	COM44	-5669	-280								
335	COM43	-5669	-350								
336	COM42	-5669	-420								
337	COM41	-5669	-490								
338	COM40	-5669	-560								
339	COM39	-5669	-630								
340	COM38	-5669	-700								
341	COM37	-5669	-770								
342	COM36	-5669	-840								
343	COM35	-5669	-910								
344	COM34	-5669	-980								
345	COM33	-5669	-1050								
346	COM32	-5669	-1120								
347	DUMMY	-5669	-1190								
348	DUMMY	-5669	-1260								
349	DUMMY	-5669	-1330								

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power Supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="9">V0
V1
V2
V3
V4</td><td rowspan="9">I/O</td><td colspan="5">LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias.</td></tr>
<tr><td>LCD Bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/9 Bias</td><td>8/9 x V0</td><td>7/9 x V0</td><td>2/9 x V0</td><td>1/9 x V0</td></tr>
<tr><td>1/8 Bias</td><td>7/8 x V0</td><td>6/8 x V0</td><td>2/8 x V0</td><td>1/8 x V0</td></tr>
<tr><td>1/7 Bias</td><td>6/7 x V0</td><td>5/7 x V0</td><td>2/7 x V0</td><td>1/7 x V0</td></tr>
<tr><td>1/6 Bias</td><td>5/6 x V0</td><td>4/6 x V0</td><td>2/6x V0</td><td>1/6 x V0</td></tr>
<tr><td>1/5 Bias</td><td>4/5 x V0</td><td>3/5 x V0</td><td>2/5 x V0</td><td>1/5 x V0</td></tr>
<tr><td colspan="5"></td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3-	O	Capacitor 3 negative connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input/output pin
VR	I	V0 voltage adjustment pin. It is valid only when on-chip resistors are not used (INTRS = “L”)
DCDC5B	I	5-times boosting circuit enable input pin. When this pin is low in 4-times boosting circuit, the 5-times boosting voltage appears at VOUT
REXT1 REXT2	I	When using an internal clock oscillator, connect a resistor between REXT1 and REXT2.
VEXT	I	External VREF input terminal for the LCD power supply voltage regulator.

SYSTEM CONTROL

Table 5. System Control Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">MS</td><td rowspan="5">I</td><td>Master/slave operation select pin.
– MS = "H": Master operation
– MS = "L": Slave operation
The following table depends on the MS status.</td></tr>
<tr><td>
<table>
<tr><th>MS</th><th>OSC Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>M</th><th>DISP</th><th>OSCCK</th></tr>
<tr><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable/disable select pin.
– CLS = “H”: Enable
– CLS = “L”: Disable (External display clock input to OSCCK pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
When the KS0711 is used in master/slave mode (multi-chip), the CL pins must be connected each other.
– MS = “H”: Output
– MS = “L”: Input</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input/output pin.
When the KS0711 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = “H”: Output
– MS = “L”: Input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin.
This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input/output. When KS0711 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
– MS = “H”: Output
– MS = “L”: Input</td></tr>
<tr><td>REF</td><td>I</td><td>Selects the external VREF voltage via the VEXT terminal.
– REF = “H”: Using the internal VREF
– REF = “L”: Using the external VREF</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor select pin.
This pin selects the resistors for adjusting V0 voltage level and is available only in master mode.
– INTRS = "H": Use the internal resistors.
– INTRS = "L": Use the external resistors. V0 voltage is controlled by VR pin and external resistive divider.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver.
– HPMB = "L": High power mode
– HPMB = "H": Normal mode
This pin is valid in master operation.</td></tr>
</table>

Table 5. System Control Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">DUTY0
DUTY1</td><td rowspan="6">I</td><td colspan="3">The LCD driver duty ratio depends on the following table.</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty Ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L/H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td rowspan="5">OSCCK</td><td rowspan="5">I/O</td><td colspan="3">Oscillator clock input/output</td></tr>
<tr><td>MS</td><td>CLS</td><td>OSCCK</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td></tr>
<tr><td>L</td><td>Input</td></tr>
<tr><td>L</td><td>-</td><td>Input</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin.
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface Mode</td><td>Chip Select</td><td>Data/ Instruction</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID(DB7)</td><td>Write only</td><td>SCLK(DB6)</td></tr>
</table></td></tr>
<tr><td>*Note: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input pin in parallel mode
– C68 = "H": 6800-series MPU interface
– C68 = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins.
Data/instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin.
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="3">RW_WR</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
– RW = “H” : Read
– RW = “L” : Write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>MI</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: High impedance
– DB6: Serial input clock (SCLK)
– DB7: Serial input data (SID).
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Output Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG131</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs.
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM63</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs.
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons. The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master/slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

TEST PINS

Table 8. Test Pins Description

Name	I/O	Description
TEST1 to TEST5	I	IC test pins – TEST1 to TEST2 pins: High – TEST3 to TEST5 pins: Open
TEMPS0 to TEMPS1	I	– TEMPS0 to TEMPS1 pins: High or Low

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip select input

There are CS1B and CS2 pins for chip selection. The KS0711 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / serial interface

KS0711 has three types of interface with an MPU, which are one serial and two parallel interface. This parallel or serial interface is determined by PS pin as shown in **Table 9.**

Table 9. Parallel / Serial Interface Mode.

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*× : don't care

Parallel interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in **Table 10**. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in **Table 11**.

Table 10. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 11. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register(Instruction)

Serial interface (PS = "L")

When the KS0711 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

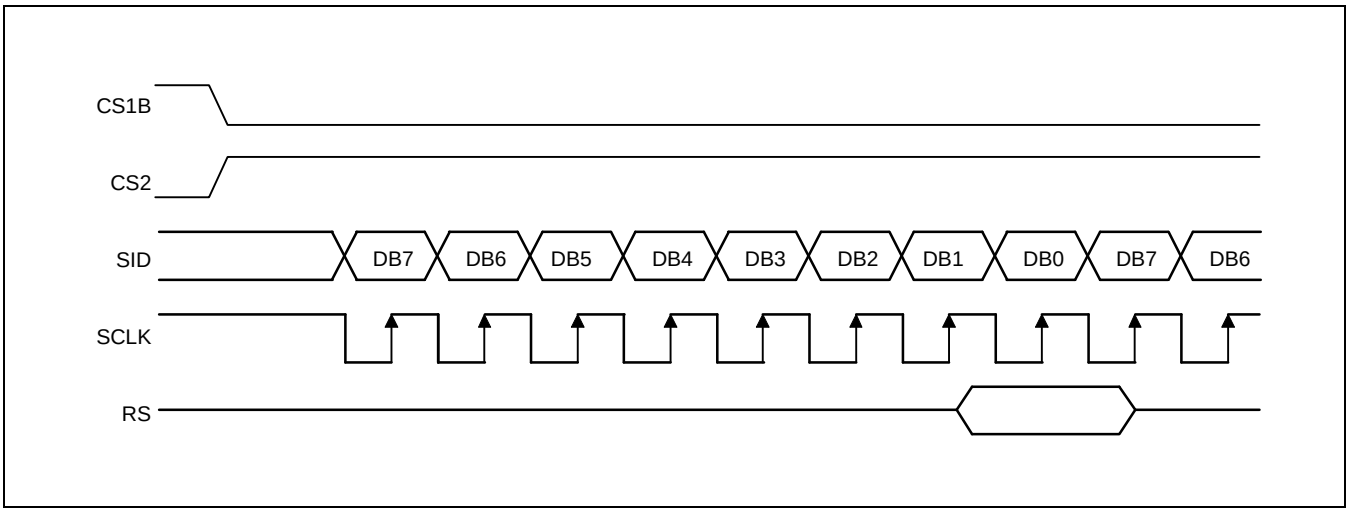


Figure 3. Serial Interface Timing

Busy Flag

The busy flag indicates whether the KS0711 is operating or not. When DB7 is "H" in Read Status operation, this device is in busy status and will accept only Read Status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The KS0711 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in **Figure 4**. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in **Figure 5**. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the Read Display Data instruction right after the address sets, but can be output at the second read of data.

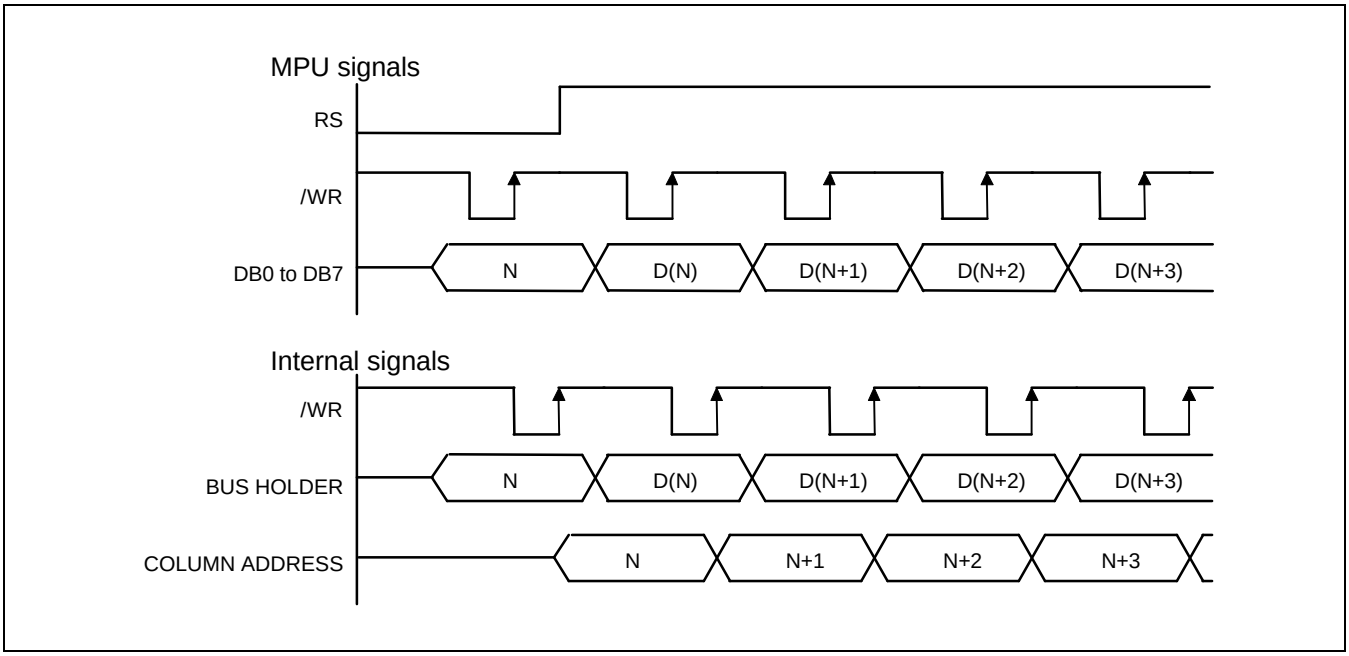


Figure 4. Write Timing

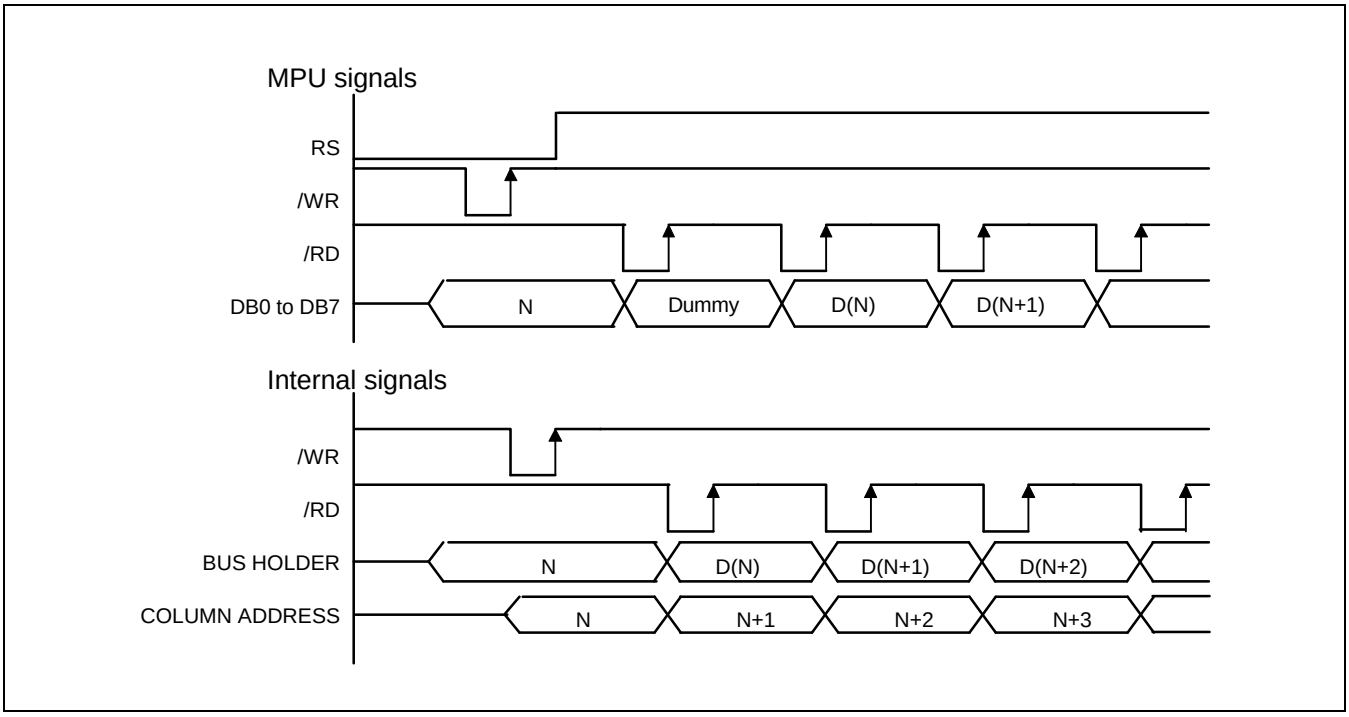


Figure 5. Read Timing

DISPLAY-DATA-RAM (DDRAM)

The DISPLAY-DATA-RAM stores pixel data for the LCD. It is 65-row ((8 page by 8 bits) + 1) by 264-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page address Circuit

This circuit is for providing a page address to DISPLAY-DATA-RAM shown in **Figure 7**. It incorporates 4-bit page address register changed by only the "Set Page" instruction. Page address 8(DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line address Circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in **Figure 7**. It incorporates 6-bit line address register changed by only the Initial Display Line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access line address of icons.

Column Address Circuit

Column address circuit has a 9-bit preset counter that provides column address to the DISPLAY-DATA-RAM as shown in **Figure 7**. When Set Column Address MSB/LSB instruction is issued, 8-bits [Y8:Y1] are set and lowest bit, Y0 is set to "0". Since this address is increased by 1 each a Read or Write Data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 108H. It is unlocked if a column address is set again by Set Column Address MSB/LSB instruction. And the column address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following **Figure 6**.

SEG Output	SEG 0		SEG 1		SEG 2		SEG 3		... ...	SEG 129		SEG 130		SEG 131		SEG 131	
Column Address [Y8:Y1]	00H		01H		02H		03H		... ...	80H		81H		82H		83H	
Internal Column Address [Y8:Y1]	000 HEX	001 HEX	002 HEX	003 HEX	004 HEX	005 HEX	006 HEX	007 HEX	... ...	100 HEX	101 HEX	102 HEX	103 HEX	104 HEX	105 HEX	106 HEX	107 HEX
Display data(ADC = 0)	1	1	1	0	0	0	0	1	... ...	1	0	1	1	0	0	0	1
LCD Panel Display									... ...								
Display data(ADC = 1)	0	1	0	0	1	1	1	0	... ...	0	1	0	0	1	0	1	1
LCD Panel Display									... ...								

Figure 6. The Relationship between the Column Address and The Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display On/Off, Reverse Display On/Off and Entire Display On/Off instructions without changing the data in the display data RAM.

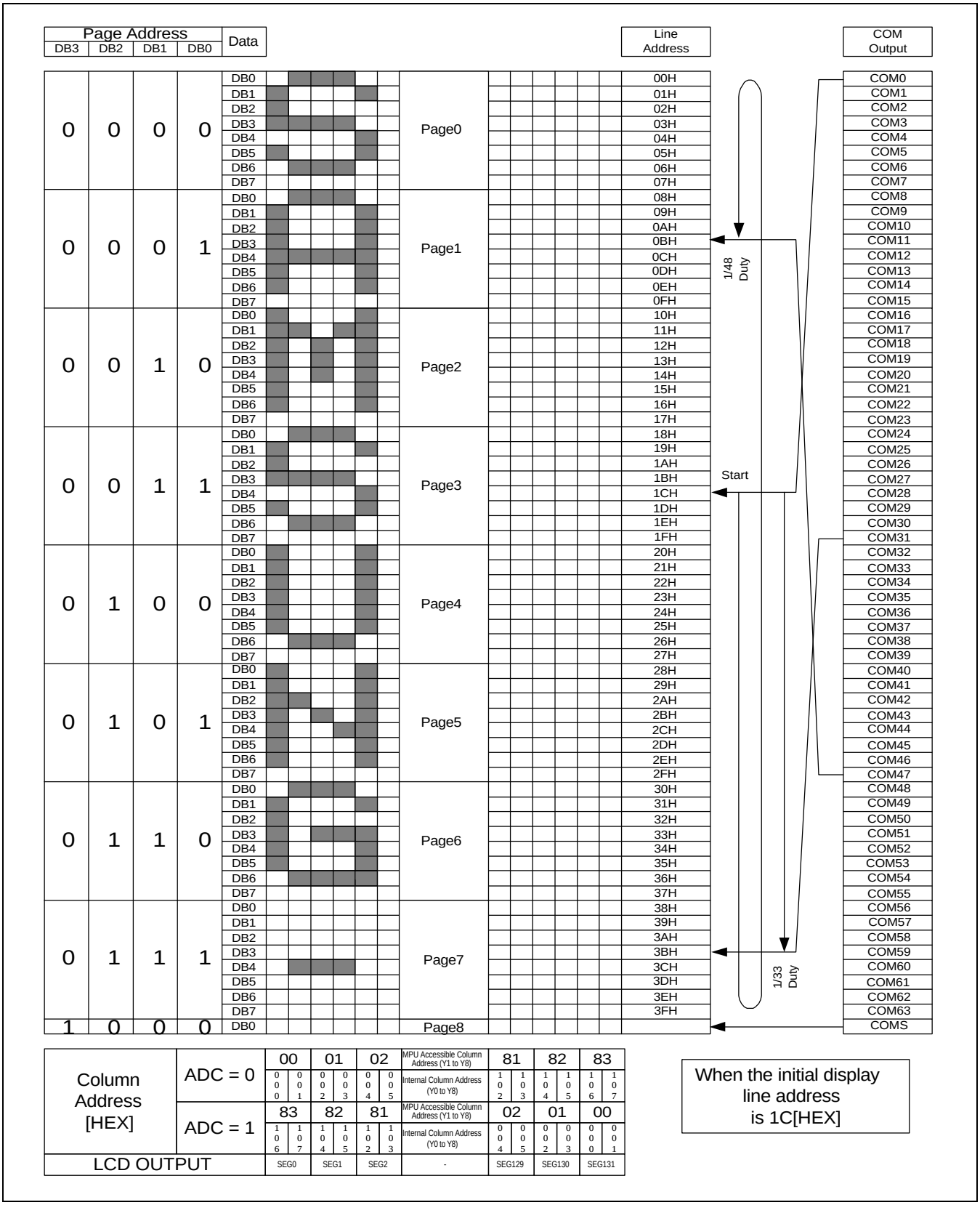


Figure 7. Display-Data-RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

* Test condition: Temperature: 25°C & 85°C, REXT=250 kΩ, No load

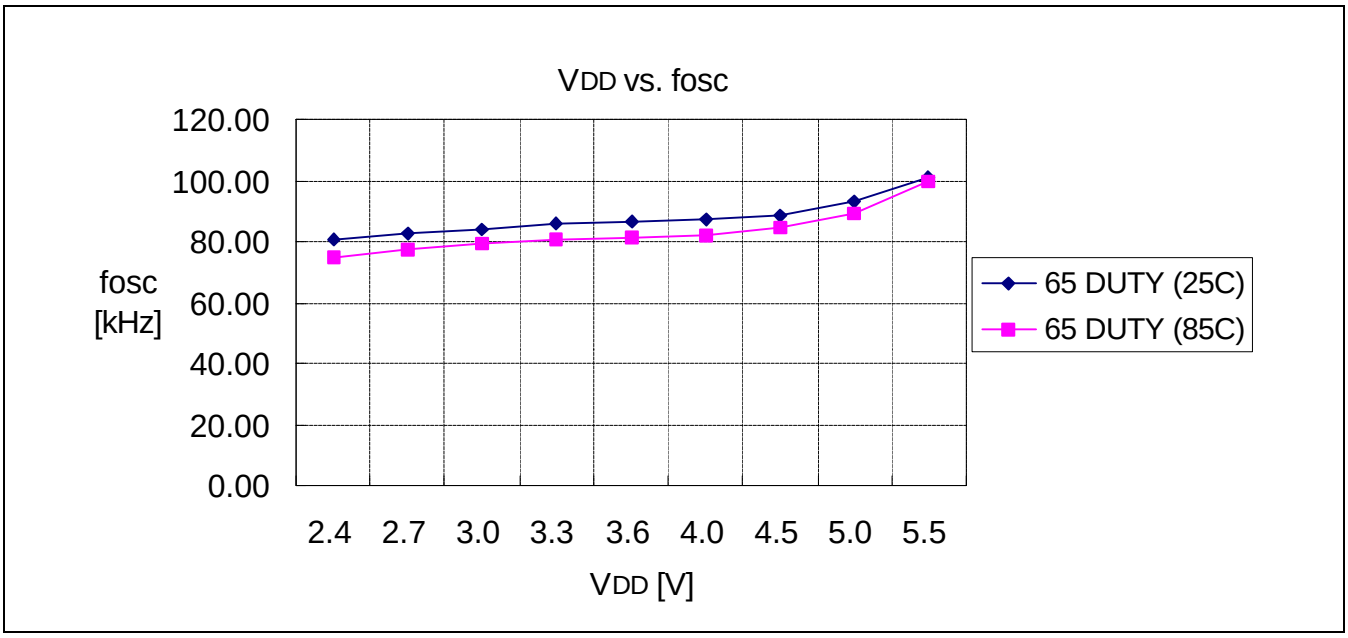


Figure 9. V_{DD} vs. fosc

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in **Figure 8**.

In a multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. **Table 12** shows the M, CL, and DISP status.

Table 13. Master and Slave Timing Signal Status

Operation Mode	Oscillator	M	CL	DISP
MASTER	ON (Internal clock used)	Output	Output	Output
	OFF(External clock used)	Output	Input	Output
SLAVE	-	Input	Input	Input

FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The KS0711 incorporates an FRC function and a PWM function circuit to display a four-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage. The KS0711 provides four 4-bit palette-registers to assign the desired gray level. These registers are set by the instructions and RESETB.

– Gray scale table of 4 FRC (Frame Rate Control)

Gray Scale Level	MSB(DB7 to DB4)	LSB(DB3 to DB0)
White	2nd FR(FR2)	1st FR(FR1)
	4th FR(FR4)	3rd FR(FR3)
Light Gray	2nd FR(FR2)	1st FR(FR1)
	4th FR(FR4)	3rd FR(FR3)
Dark Gray	2nd FR(FR2)	1st FR(FR1)
	4th FR(FR4)	3rd FR(FR3)
Black	2nd FR(FR2)	1st FR(FR1)
	4th FR(FR4)	3rd FR(FR3)

– Gray scale table of 3 FRC (Frame Rate Control)

Gray Scale Level	MSB(DB7 to DB4)	LSB(DB3 to DB0)
White	2nd FR(FR2)	1st FR(FR1)
	××××	3rd FR(FR3)
Light Gray	2nd FR(FR2)	1st FR(FR1)
	××××	3rd FR(FR3)
Dark Gray	2nd FR(FR2)	1st FR(FR1)
	××××	3rd FR(FR3)
Black	2nd FR(FR2)	1st FR(FR1)
	××××	3rd FR(FR3)

– Gray scale table of 15 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM(on width)	Note
0	00	0000	0(0/15)	
1	01	0001	1/15	
2	02	0010	2/15	
3	03	0011	3/15	
4	04	0100	4/15	
5	05	0101	5/15	
6	06	0110	6/15	
7	07	0111	7/15	
8	08	1000	8/15	
9	09	1001	9/15	
10	0A	1010	10/15	
11	0B	1011	11/15	
12	0C	1100	12/`5	
13	0D	1101	13/15	
14	0E	1110	14/15	
15	0F	1111	1(15/15)	

– Gray scale table of 12 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM(on width)	Note
0	00	0000	0(0/12)	
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1(12/12)	
13	0D	1101	0/12	(NOTE)
14	0E	1110	0/12	(NOTE)
15	0F	1111	0/12	(NOTE)

NOTE: This area is selected to off level (0/12 level).

– Gray scale table of 9 PWM (Pulse Width Modulation)

	Hex	4-Bits	PWM(on width)	Note
0	00	0000	0(0/9)	
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1(9/9)	
10	0A	1010	0/9	(NOTE)
11	0B	1011	0/9	(NOTE)
12	0C	1100	0/9	(NOTE)
13	0D	1101	0/9	(NOTE)
14	0E	1110	0/9	(NOTE)
15	0F	1111	0/9	(NOTE)

NOTE: This area is selected to off level (0/9 level).

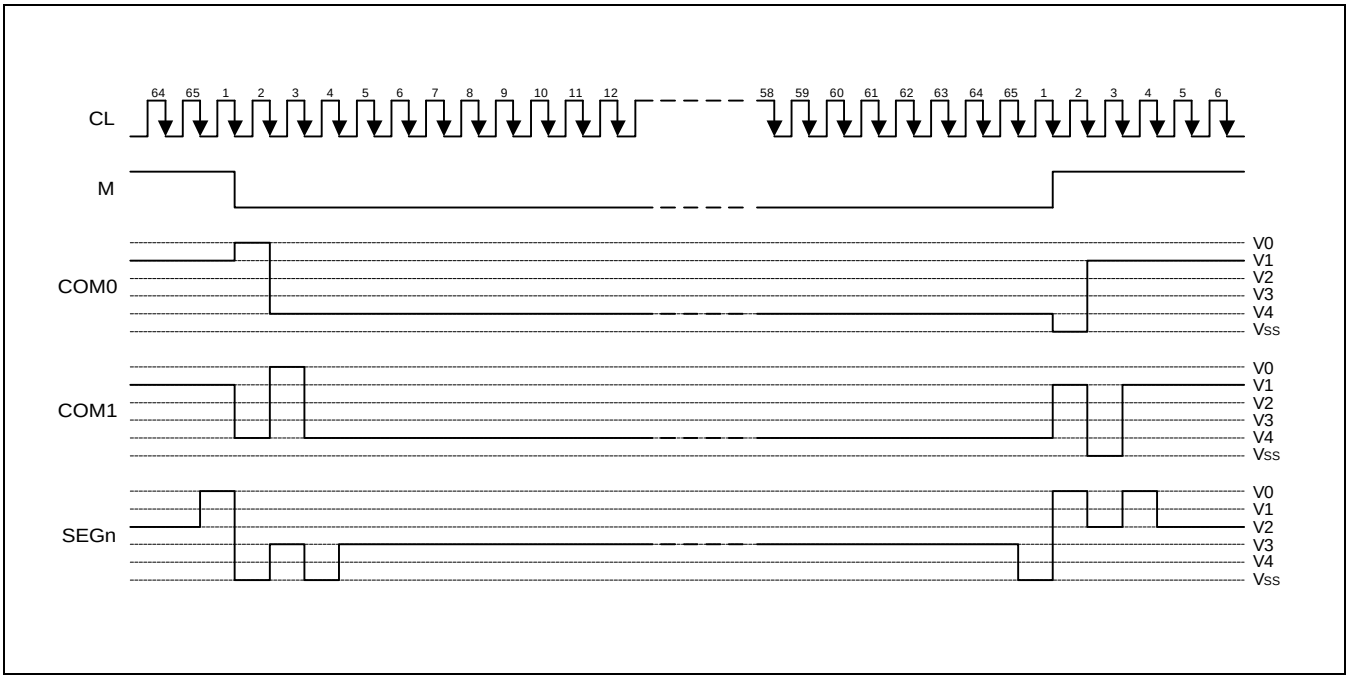


Figure 8. 2-frame AC Driving Waveform (duty ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 13. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common Output Pins						
		COM[0:15]	**COM[16:23]**	**COM[24:31]**	**COM[32:39]**	**COM[40:47]**	**COM[48:63]**	**COMS**
1/33	0	COM[0:15]	*NC				COM[16:31]	COMS
	1	COM[31:16]	*NC				COM[15:0]	
1/49	0	COM[0:23]		*NC		COM[24:47]		COMS
	1	COM[47:24]		*NC		COM[23:0]		
1/65	0	COM[0:63]						COMS
	1	COM[63:0]						

*NC: No Connection

LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel (including 2 COMS channel) common driver and 132-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

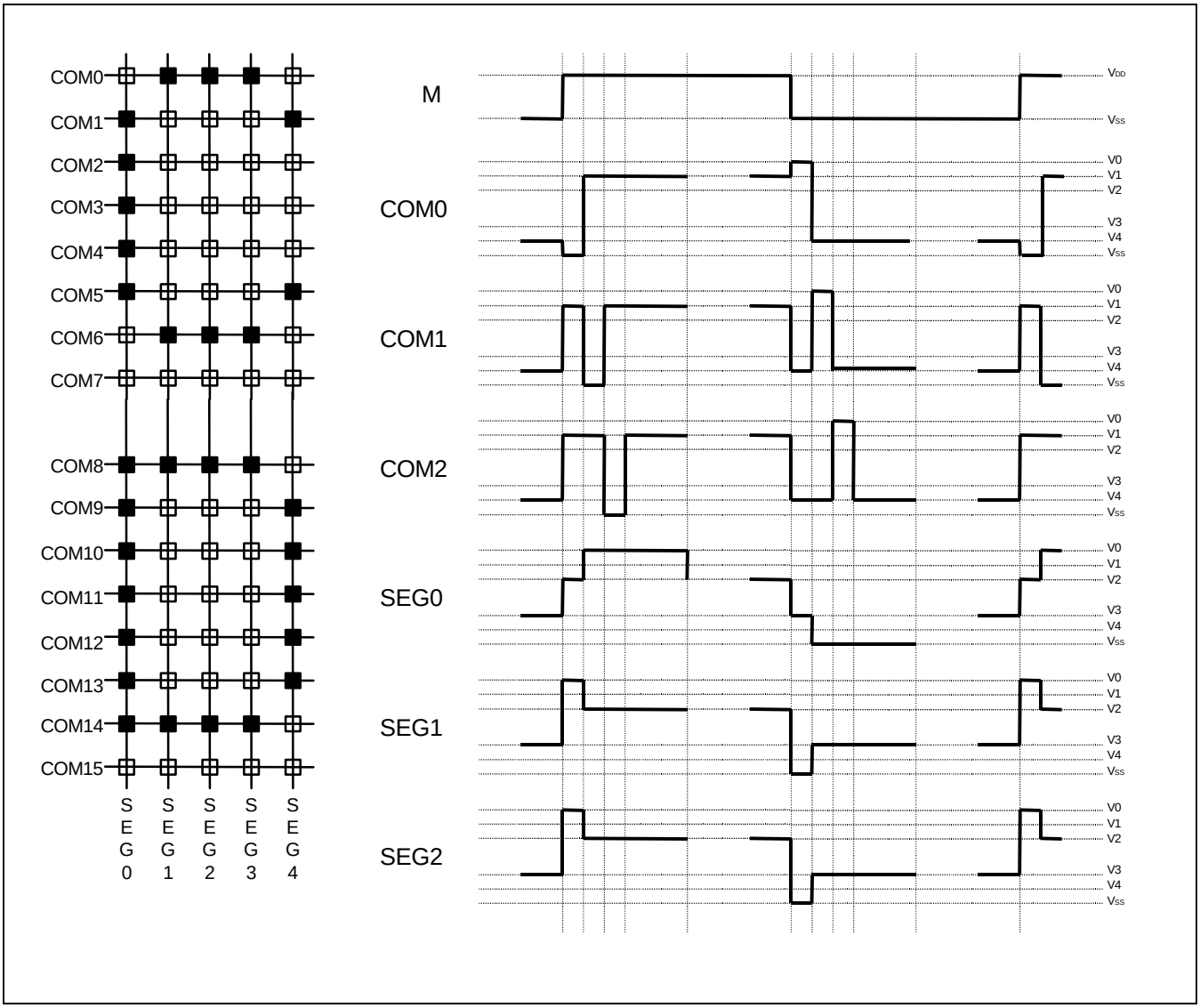


Figure 9. Segment and Common Timing

POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by Power Control instruction. For details, refers to "Instruction Description". **Table 14** shows the referenced combinations in using power supply circuits.

Table 14. Recommended Power Supply Combinations

User Setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

Voltage converter circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, 4, or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 ㎌]

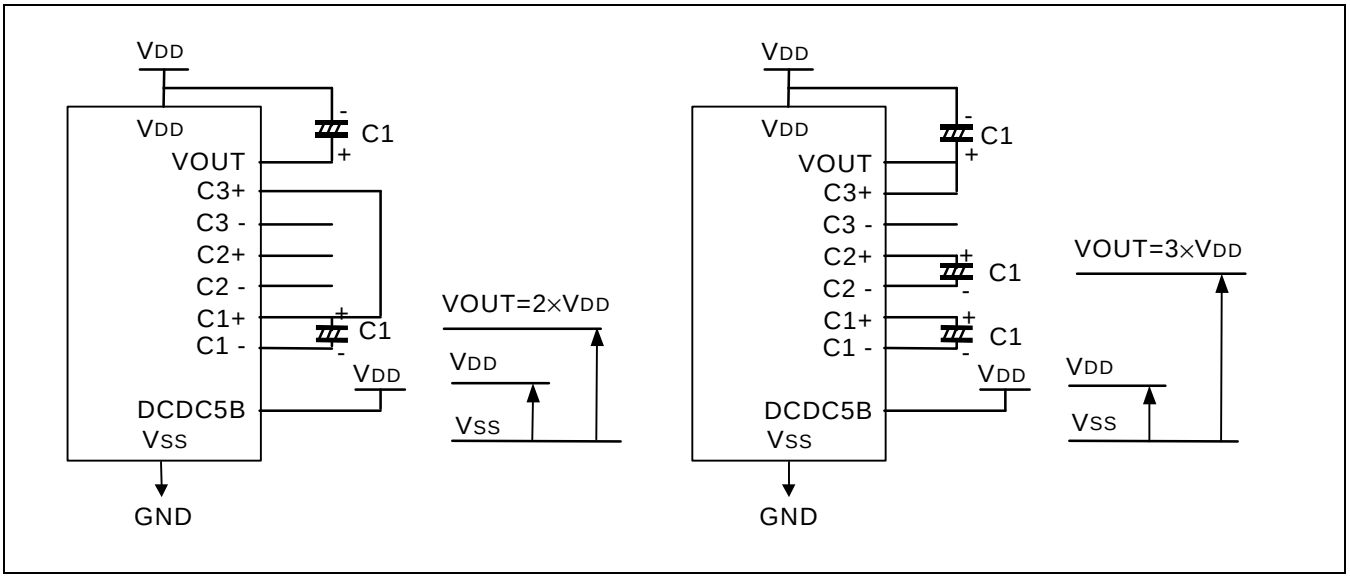


Figure 10. Two times boosting circuit **Figure 11. Three times boosting circuit**

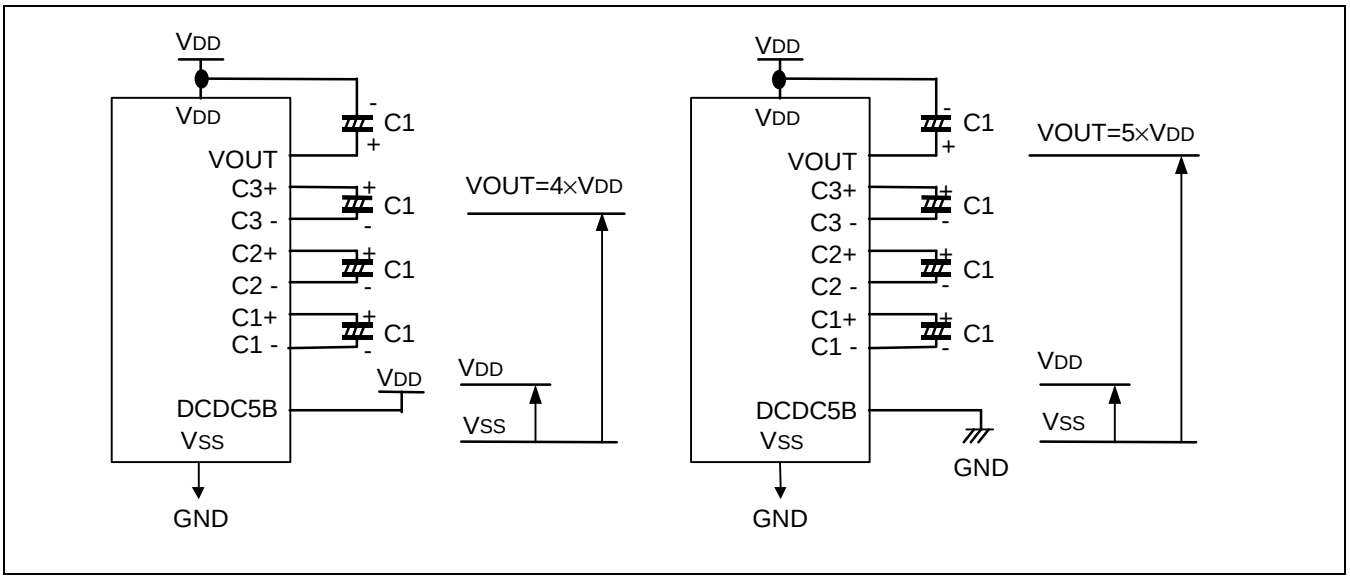


Figure 12. Four times boosting circuit **Figure 13. Five times boosting circuit**

Voltage regulator circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in **Figure 15**, it is necessary to be applied internally or externally.

For the **Eq. 1**, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by **Eq. 2**, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in **Table 15**.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{162}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 15. V_{REF} Voltage at Ta = 25°C

REF	Temp. Coefficient	V_{REF} [V]
H	-0.05%/°C	2.1
	-0.2%/°C	
L	External Input	VEXT

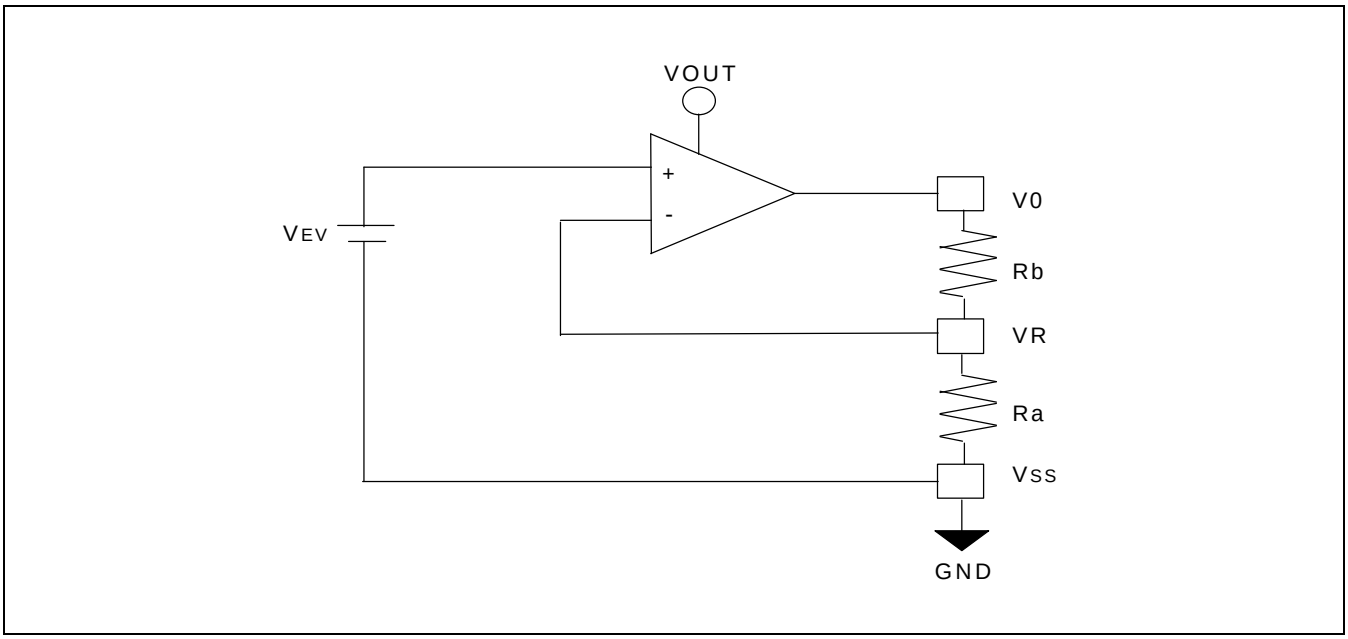


Figure 14. Internal Voltage Regulator Circuit

In case of using internal resistors, Ra and Rb. (INTRS = "H")

When INTRS pin is “H”, resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 16. Internal Rb/Ra ratio depending on 3-bit data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1+(Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.4	5.9	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb/Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

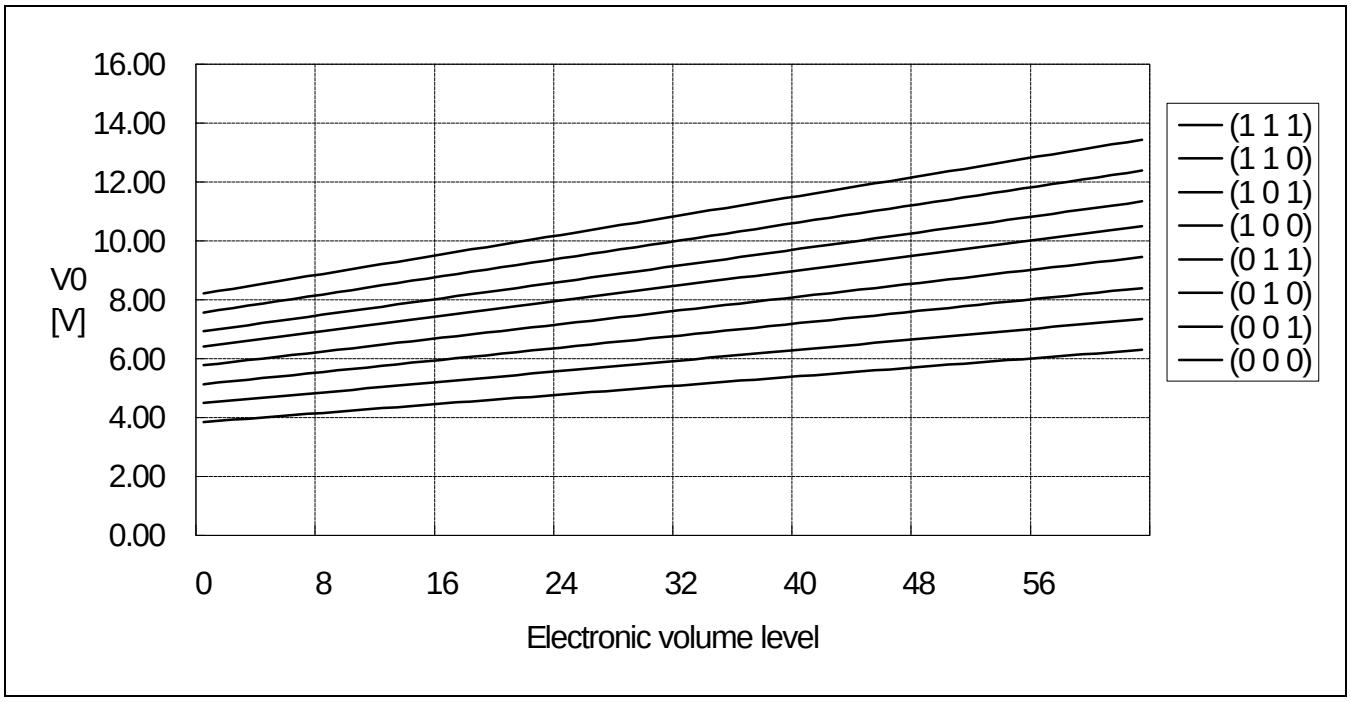


Figure 15. Electronic volume level (Temp. Coefficient = -0.05% / °C, -0.2% / °C)

In case of using external resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1,0,0,0,0,0)
3. Maximum current flowing Ra, Rb = 1 uA

From **Eq. 1**

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ } (\textbf{Eq. 3})$$

From **Eq. 2**

$$V_{EV} = \left(1 - \frac{(63 - 32)}{162}\right) \times 2.1 = 1.698 \quad [V] \text{ ------ } (\textbf{Eq. 4})$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ } (\textbf{Eq. 5})$$

From equations **Eq. 3, 4** and **5**
Ra = 1.69 [MΩ]
Rb = 8.31 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 17. V0 depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	**7.59**	**.....**	**10.00**	**.....**	**12.43**

Voltage follower circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower for increasing drive capability. **Table 18** shows the relationship between V1 to V4 level and each duty ratio.

Table 18. The relationship between V1 to V4 level and each duty ratio

Duty Ratio	DUTY1	DUTY0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
			1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/49	L	H	1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
			1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
1/65	H	L/H	1/7	6/7 x V0	5/7 x V0	2/7 x V0	1/7 x V0
			1/9	8/9 x V0	7/9 x V0	2/9 x V0	1/9 x V0

REFERECE CIRCUIT EXAMPLES

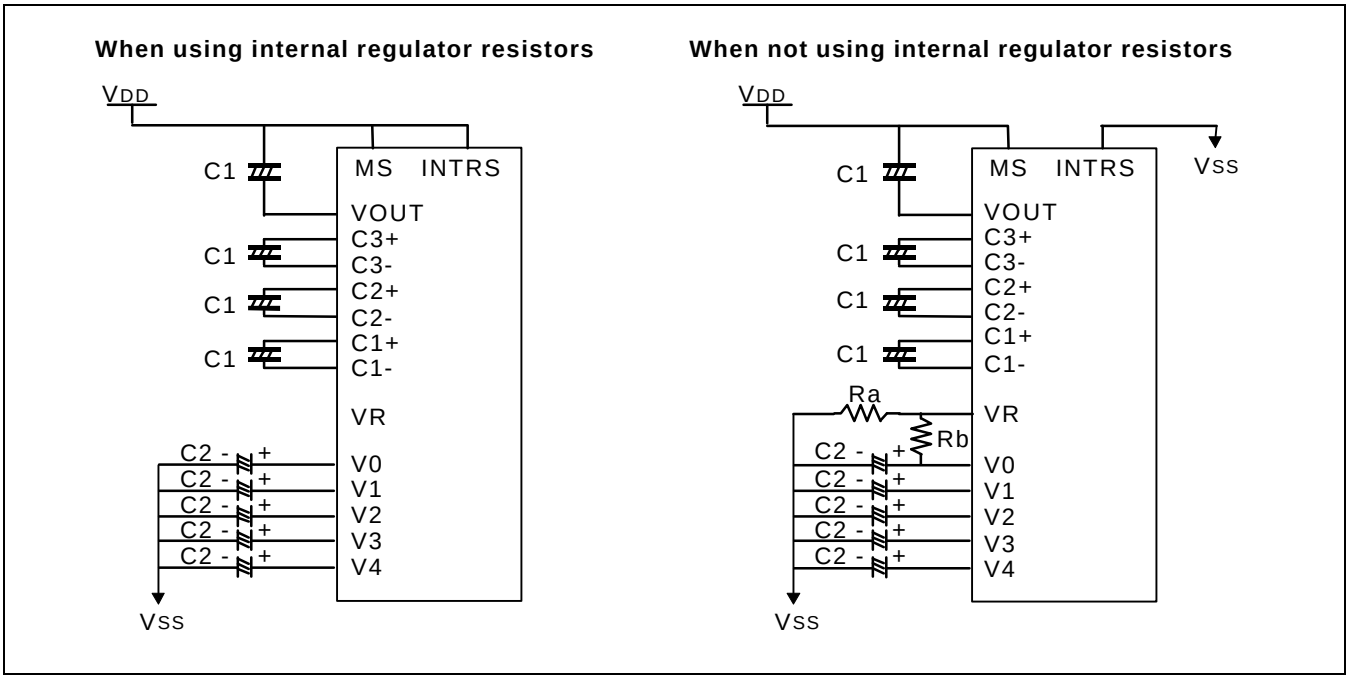


Figure 16. When Using All LCD Power Circuits (4-Times V/C: On, V/R: On, V/F: On)

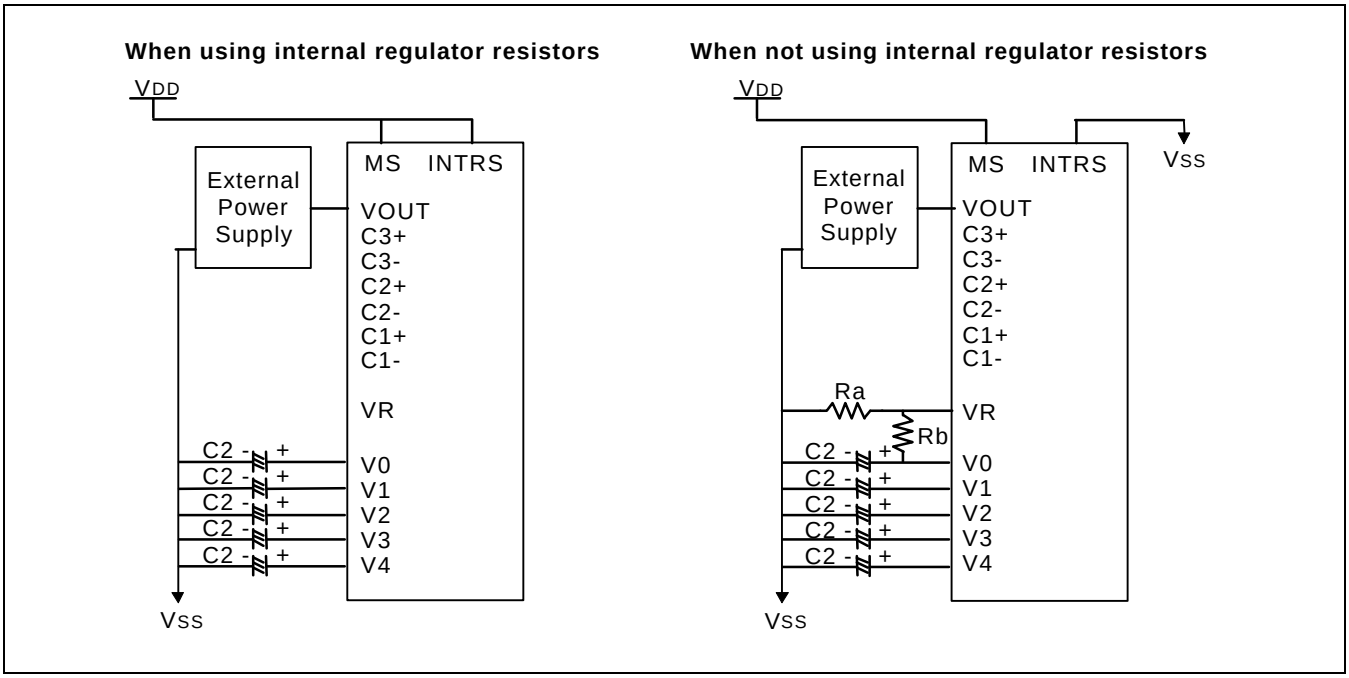


Figure 17. When Using Some LCD Power Circuits (V/C: Off, V/R: On, V/F: On)

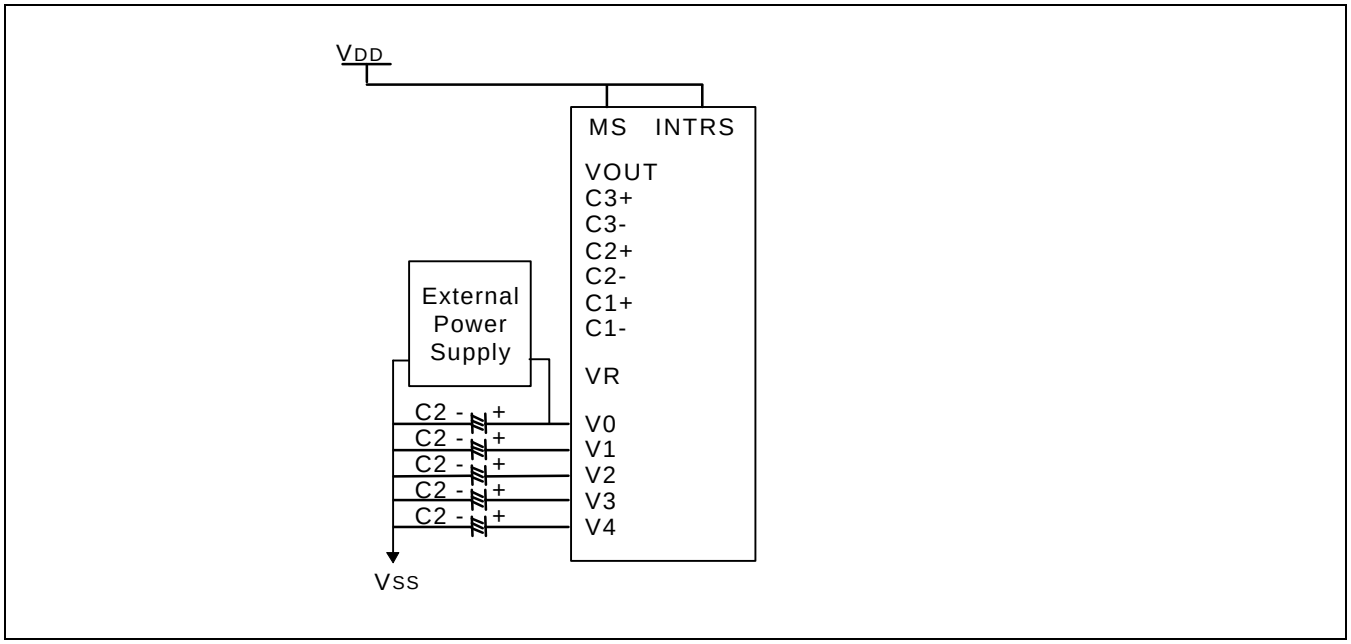
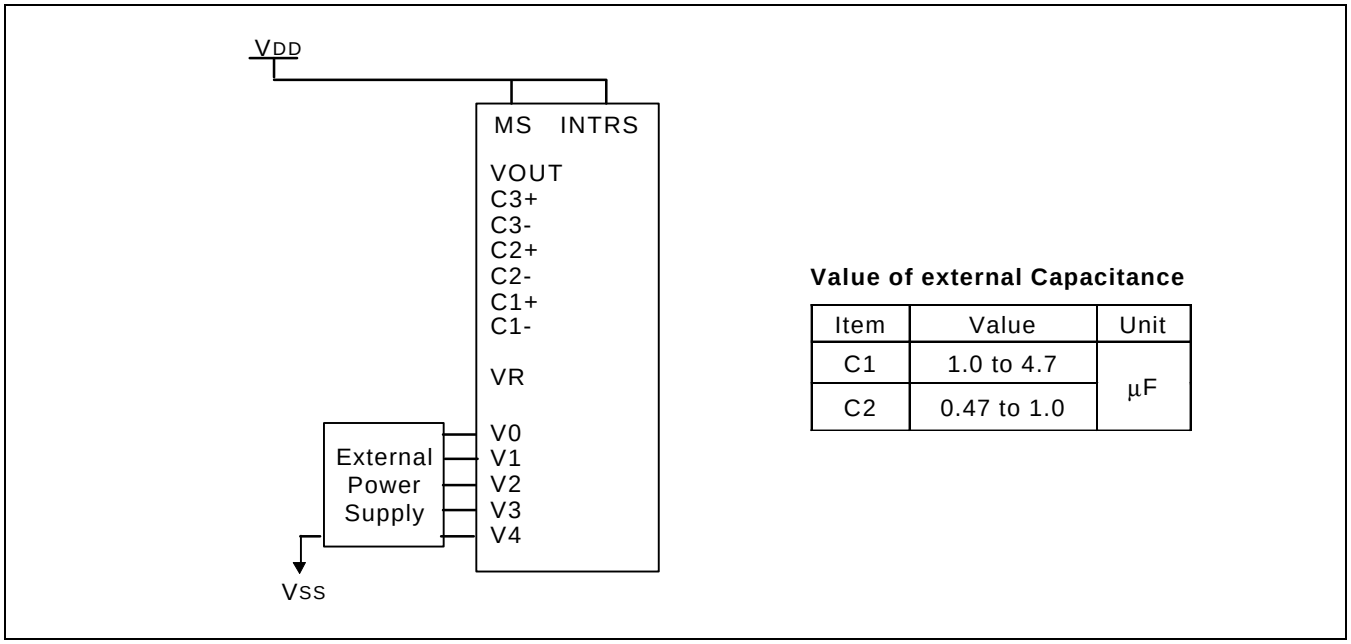


Figure 18. When Using Some LCD Power Circuits (V/C: Off, V/R: Off, V/F: On)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 19. When Not Using Any Internal LCD Power Supply Circuits (V/C: Off, V/R: Off, V/F: Off)

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Display on/off: off
Entire display on/off: off (normal)
Reverse display on/off: off (normal)
ADC select: off (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
LCD bias ratio: 1/7(1/65 Duty), 1/6(1/49 Duty), 1/5(1/33 Duty)
Read-modify-write: off
SHL select: off (normal)
Static indicator mode: off
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: off
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
White mode set: off
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
Light gray mode set: off
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
Dark gray mode set: off
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
Black mode set: off
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
FRC, PWM mode: 4FRC, 9PWM

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: off
SHL select: 0 (normal)
Static indicator mode: off
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: off
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
White mode set: off
White palette register (WG3, WG2, WG1, WG0) = (0, 0, 0, 0)
Light gray mode set: off
Light gray palette register (LG3, LG2, LG1, LG0) = (0, 0, 0, 0)
Dark gray mode set: off
Dark gray palette register (DG3, DG2, DG1, DG0) = (1, 1, 1, 1)
Black mode set: off
Black palette register (BG3, BG2, BG1, BG0) = (1, 1, 1, 1)
FRC, PWM mode: 4FRC, 9PWM

While RESETB is “L” or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 19. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read Display Data	1	1	Read data								Read data from DDRAM
Write Display Data	1	0	Write data								Write data into DDRAM
Read Status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Display On/Off	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set Reference Voltage Mode	0	0	1	0	0	0	0	0	0	1	Set Reference Voltage Mode
Set Reference Voltage Register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set Reference Voltage Register
Set Page Address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set Column Address MSB	0	0	0	0	0	1	Y8	Y7	Y6	Y5	Set column address MSB
Set Column Address LSB	0	0	0	0	0	0	Y4	Y3	Y2	Y1	Set column address LSB
ADC Select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0: normal direction (SEG0→SEG131) When ADC=1: reverse direction (SEG131→SEG0)
Reverse Display ON/OFF	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0: normal display When REV=1: reverse display
Entire Display ON/OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
LCD Bias Select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias When BIAS = 0: 1/7 when BIAS = 1: 1/9
Set Modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0: normal direction (COM0→COM63) When SHL=1: reverse direction (COM63→COM0)
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator Resistor Select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set Static Indicator Mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode When SM = 0: off When SM = 1: on
Set Static Indicator Register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power Save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON

Table 19. Instruction Table (Continued)

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Set white mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	0	0	0	Set white mode and 1st/2nd frame
	0	0	WB3	WB2	WB1	WB0	WA3	WA2	WA1	WA0	Set white 1st/2nd register
Set white mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	0	0	1	Set white mode and 3rd/4th frame
	0	0	WD3	WD2	WD1	WD0	WC3	WC2	WC1	WC0	Set white 3rd/4th register
Set light gray mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	0	0	1	Set light gray mode and 1st/2nd frame
	0	0	LB3	LB2	LB1	LB0	LA3	LA2	LA1	LA0	Set light gray 1st/2nd register
Set light gray mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	0	1	1	Set light gray mode and 3rd/4th frame
	0	0	LD3	LD2	LD1	LD0	LC3	LC2	LC1	LC0	Set light gray 3rd/4th register
Set dark gray mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	1	0	0	Set dark gray mode and 1st/2nd frame
	0	0	DB3	DB2	DB1	DB0	DA3	DA2	DA1	DA0	Set dark gray 1st/2nd register
Set dark gray mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	1	0	1	Set dark gray mode and 3rd/4th frame
	0	0	DD3	DD2	DD1	DD0	DC3	DC2	DC1	DC0	Set dark gray 3rd/4th register
Set black mode and 1st/2nd frame, set pulse width	0	0	1	1	1	1	1	1	1	0	Set black mode and 1st/2nd frame
	0	0	BB3	BB2	BB1	BB0	BA3	BA2	BA1	BA0	Set black 1st/2nd register
Set black mode and 3rd/4th frame, set pulse width	0	0	1	1	1	1	1	1	1	1	Set black mode and 3rd/4th frame
	0	0	BD3	BD2	BD1	BD0	BC3	BC2	BC1	BC0	Set black 3rd/4th register
Set FRC and PWM mode	0	0	1	1	1	1	0	FRC	PWM1	PWM0	FRC(1: 3FRC, 0: 4FRC) PWM1 PWM0 0 0/1 9PWM 1 0 12PWM 1 1 15PWM

■ Read Display Data

8-bit data from display data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

■ Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

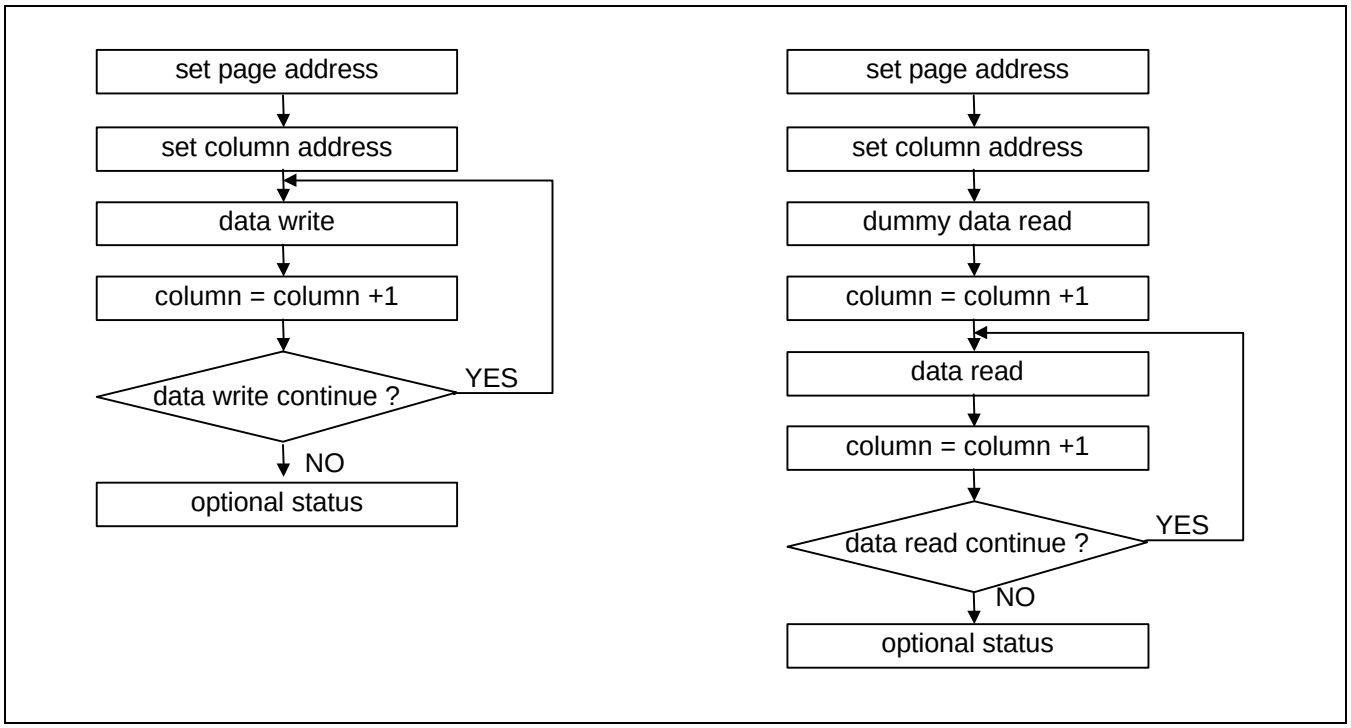


Figure 20. Sequence for Writing Display Data

Figure 21. Sequence for Reading Display Data

■ Read Status

Indicates the internal status of the KS0711.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: Chip is active, 1: Chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: Reverse direction(SEG131 → SEG0), 1: Normal direction(SEG0 → SEG131)
ON/OFF	Indicates display ON/OFF status. 0: Display ON, 1: Display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: Chip is active, 1: Chip is being reset.

■ Display ON/OFF

Turns the display On or Off.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: Display ON
DON = 0: Display OFF

■ Initial Display Line

Sets the line address of display RAM to determine the initial display line. The RAM display data is displayed at the top row (COM0) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

■ Reference Voltage Select

Consists of 2-byte instruction.
The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st instruction: Set Reference Voltage Select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd instruction: Set Reference Voltage register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	´	´	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

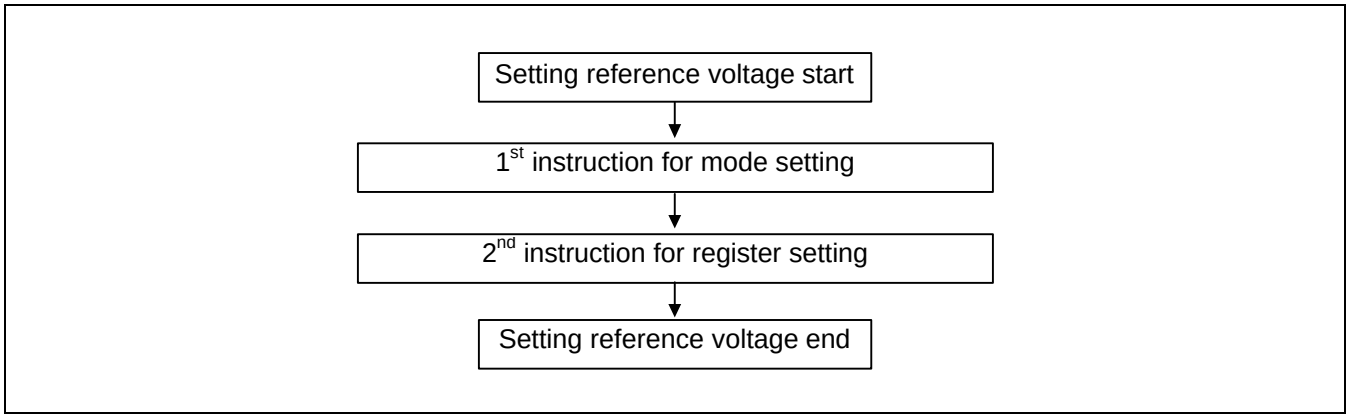


Figure 22. Sequence for setting the reference voltage

■ Set Page Address

Sets the page address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the display RAM to write or read display data. Changing the page address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

■ Set Column Address

Sets the column address of display RAM from the microprocessor into the column address register. Along with the column address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	**Y8**	**Y7**	**Y6**	**Y5**

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**0**	**Y4**	**Y3**	**Y2**	**Y1**

Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	2
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	260
1	0	0	0	0	0	1	1	262

■ **ADC Select**

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: Normal Direction (SEG0 → SEG131)
ADC = 1: Reverse Direction (SEG131 → SEG0)

■ **Reverse Display ON/OFF**

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

■ **Entire Display ON/OFF**

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display On/Off instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: Normal Display
EON = 1: Entire Display On

■ **Select LCD Bias**

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	BIAS

DUTY Ratio	DUTY1	DUTY0	LCD Bias	
			BIAS = 0	BIAS = 1
1/33	0	0	1/5	1/6
1/49	0	1	1/6	1/8
1/65	1	0/1	1/7	1/9

■ Set Modify-read

This instruction stops the automatic increment of the column address by the Read Display Data instruction, but the column address is still increased by the Write Display Data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the Reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

■ Reset Modify-read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the Set Modify Read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

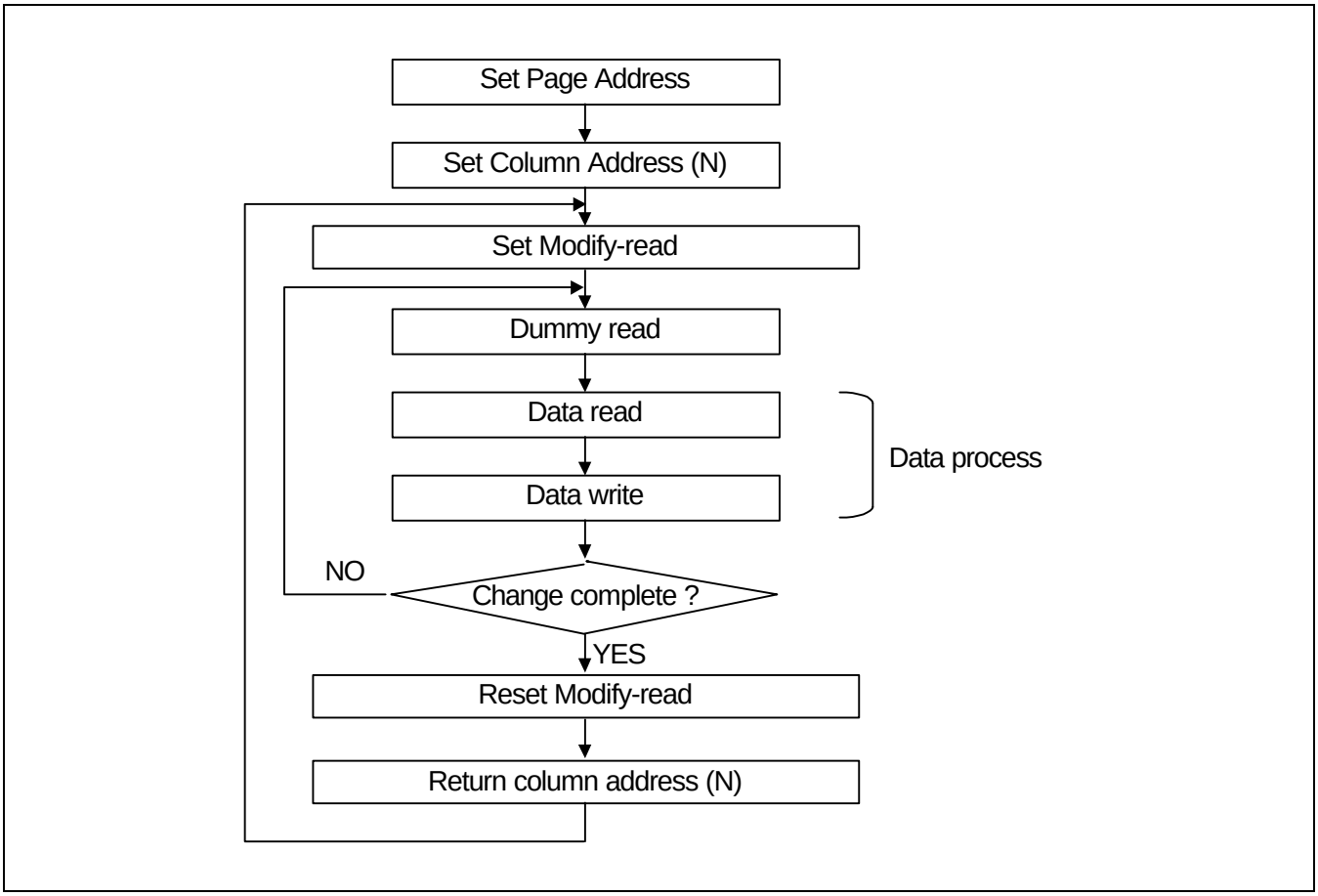


Figure 23. Sequence for cursor display

■ Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

■ SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	´	´	´

× : Don' t care

SHL = 0: Normal Direction (COM0 → COM63)
SHL = 1: Reverse Direction (COM63 → COM0)

■ Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is off Internal voltage converter circuit is on
	0 1		Internal voltage regulator circuit is off Internal voltage regulator circuit is on
		0 1	Internal voltage follower circuit is off Internal voltage follower circuit is on

■ Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the **Table 16**.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**1**	**0**	**0**	**R2**	**R1**	**R0**

R2	R1	R0	[Rb/Ra] Ratio
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

■ Set Static Indicator state

Consists of two bytes instruction. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The 1st instruction: Set Static Indicator Mode (On/Off)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**SM**

SM = 0: Static Indicator OFF
SM = 1: Static Indicator ON

The 2nd instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**´**	**´**	**´**	**´**	**´**	**´**	**S1**	**S0**

S1	S0	Status of Static Indicator Output
0	0	OFF
1	1	ON (Always ON)

■ Set Grayscale Mode & Register

Consists of two bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of grayscale register without issuing any other instruction.

– Set Gray Scale Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	GM2	GM1	GM0

GM2	GM1	GM0	Description
0	0	0	In case of setting white mode and 1st/2nd frame
0	0	1	In case of setting white mode and 3rd/4th frame
0	1	0	In case of setting light gray mode and 1st/2nd frame
0	1	1	In case of setting light gray mode and 3rd/4th frame
1	0	0	In case of setting dark gray mode and 1st/2nd frame
1	0	1	In case of setting dark gray mode and 3rd/4th frame
1	1	0	In case of setting black mode and 1st/2nd frame
1	1	1	In case of setting black mode and 3rd/4th frame

– Set Gray Scale Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	GB3	GB2	GB1	GB0	GA3	GA2	GA1	GA0
0	0	GD3	GD2	GD1	GD0	GC3	GC2	GC1	GC0

GA3,GB3, GC3,GD3	GA2,GB2, GC2, GD2	GA1,GB1, GC1,GD1	GA0,GB0, GC0, GD0	Pulse Width (9PWM)	Pulse Width (12PWM)	Pulse Width (15PWM)
0	0	0	0	0/9	0/12	0/15
0	0	0	1	1/9	1/12	1/15
:	:	:	:	:	:	:
1	0	0	1	9/9	9/12	9/15
1	0	1	0	0/9	10/12	10/15
1	0	1	1	0/9	11/12	11/15
1	1	0	0	0/9	12/12	12/15
1	1	0	1	0/9	0/12	13/15
1	1	1	0	0/9	0/12	14/15
1	1	1	1	0/9	0/12	15/15

∗ GA3=WA3,LA3,DA3,BA3 GA2=WA2,LA2,DA2,BA2 GA1=WA1,LA1,DA1,BA1 GA0=WA0,LA0,DA0,BA0
GB3=WB3,LB3,DB3,BB3 GA2=WB2,LB2,DB2,BB2 GA1=WB1,LB1,DB1,BB1 GA0=WB0,LB0,DB0,BB0
GC3=WC3,LC3,DC3,BC3 GA2=WC2,LC2,DC2,BC2 GA1=WC1,LC1,DC1,BC1 GA0=WC0,LC0,DC0,BC0
GD3=WD3,LD3,DD3,BD3 GA2=WD2,LD2,DD2,BD2 GA1=WD1,LD1,DD1,BD1 GA0=WD0,LD0,DD0,BD0

■ Set PWM & FRC

Selects 3/4 FRC and 9/12/15 PWM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	FRC	PWM1	PWM0

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	9PWM
	0	1	9PWM
	1	0	12PWM
	1	1	15PWM

■ Power Save (compound instruction)

If the Entire Display ON/OFF instruction is issued during the display OFF state, KS0711 enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When Static Indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the Display ON & Entire Display OFF instruction.

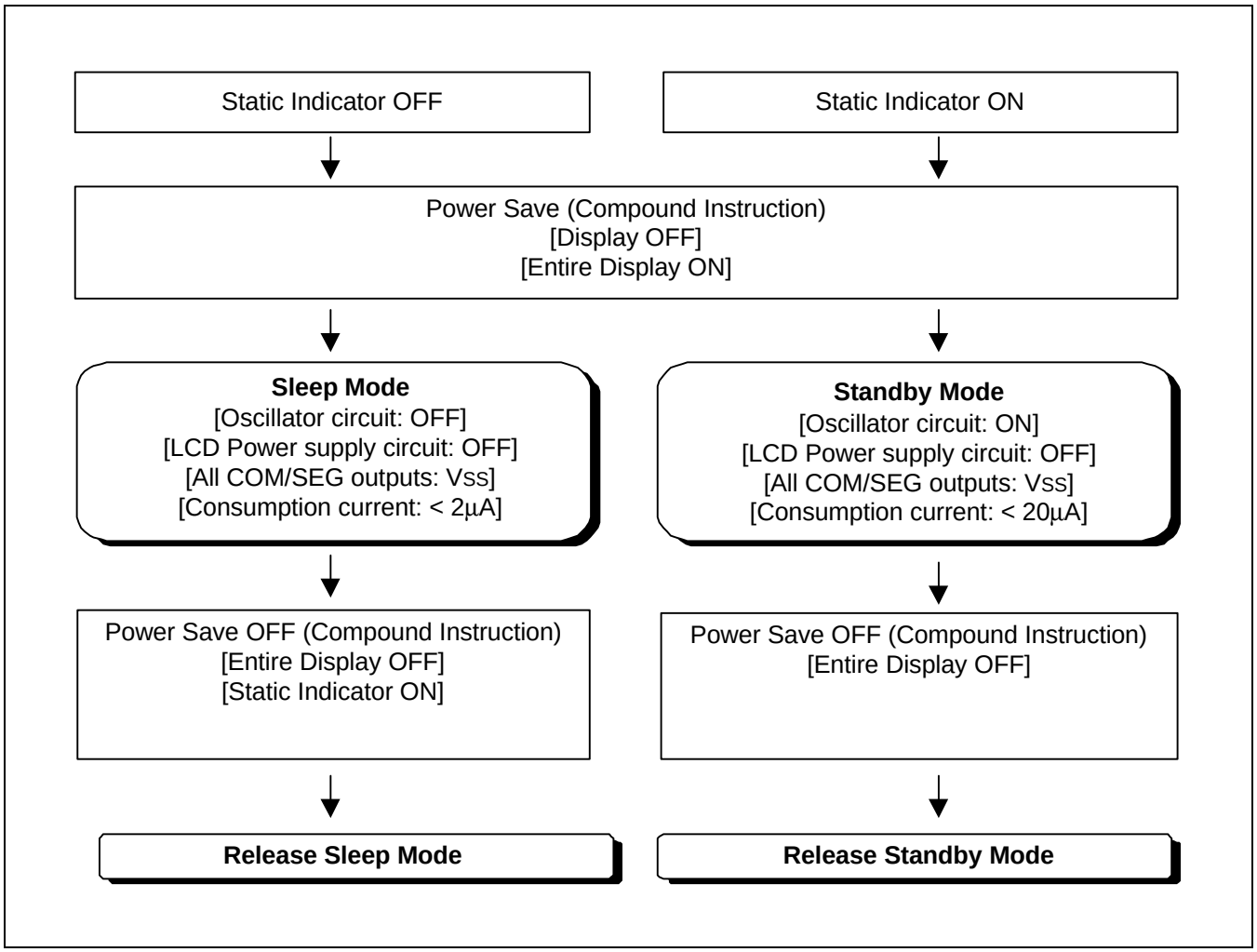


Figure 24. Power Save Routine

■ Referential Instruction Setup Flow (1)

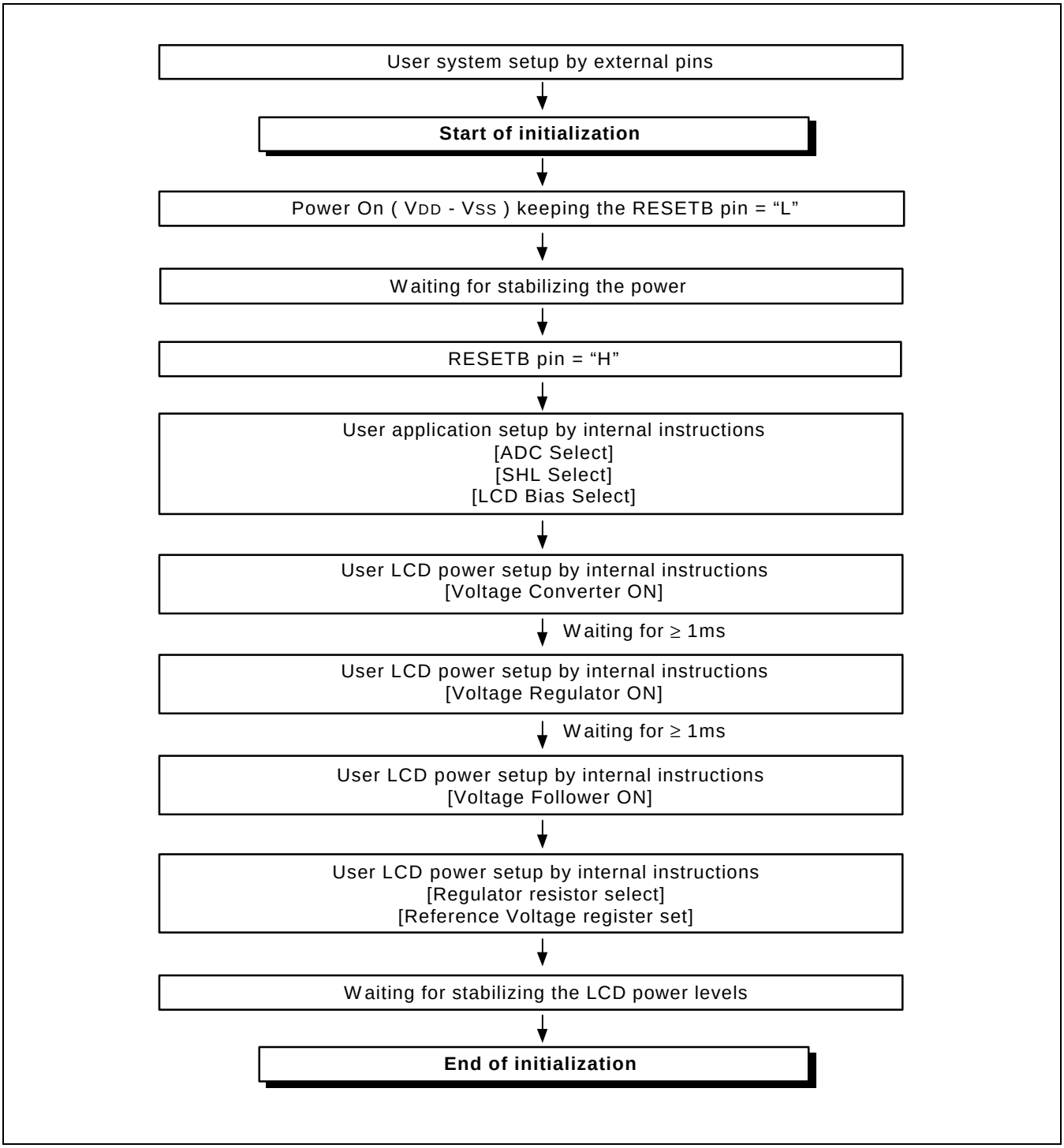


Figure 25. Initializing with the built-in power supply circuits

■ Referential Instruction Setup Flow (2)

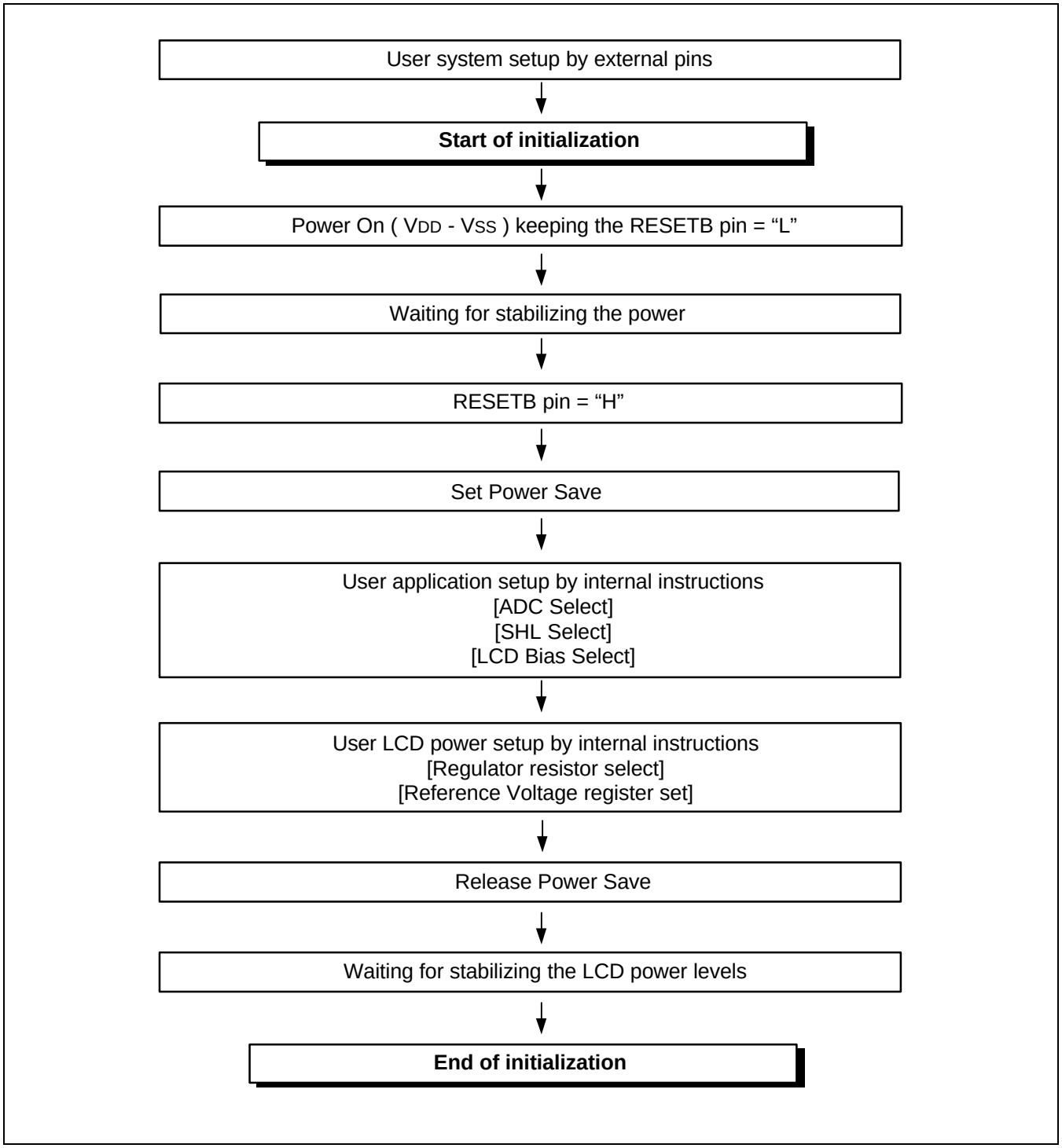


Figure 26. Initializing without the built-in power supply circuits

■ **Referential Instruction Setup Flow (3)**

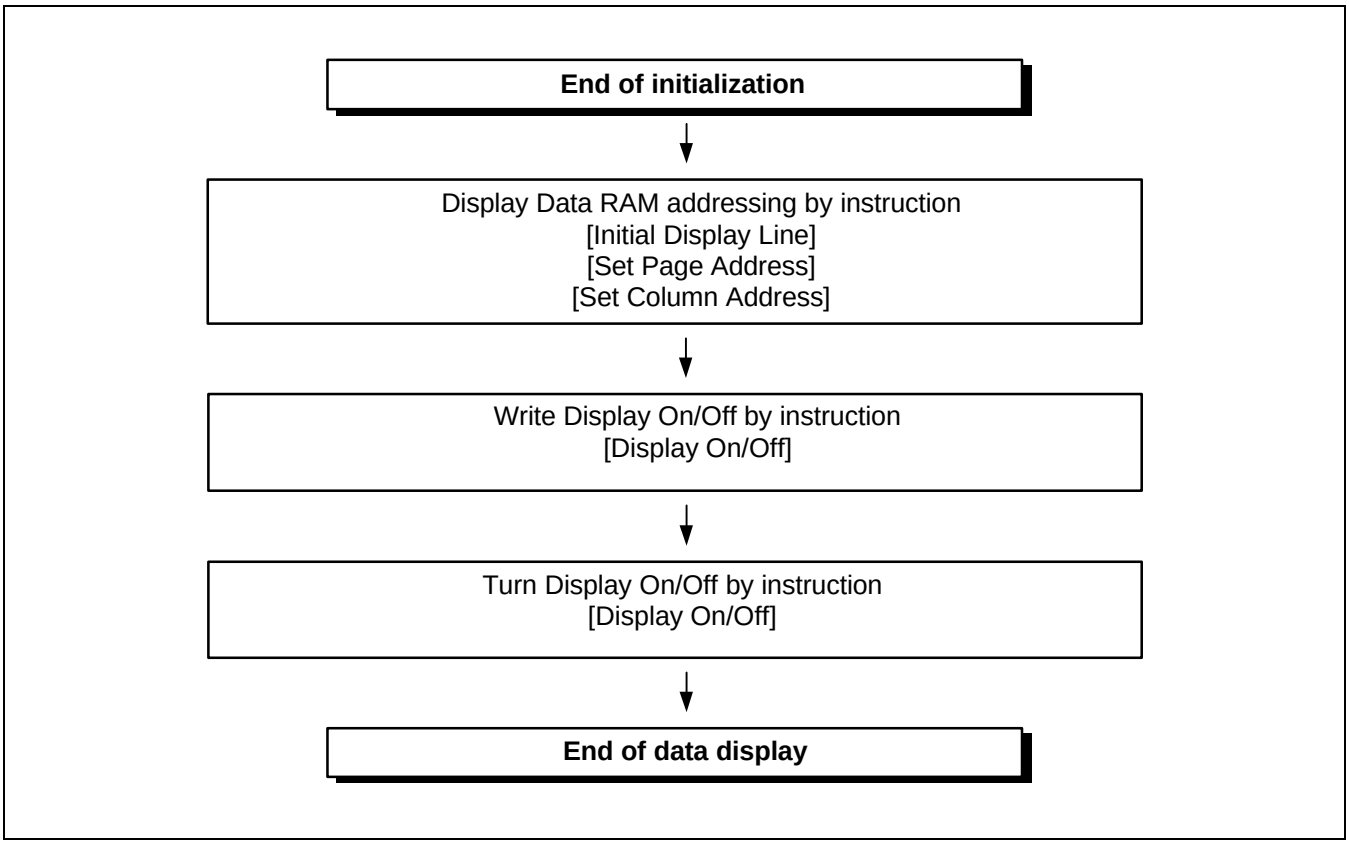


Figure 27. Data displaying

■ Referential Instruction Setup Flow (4)

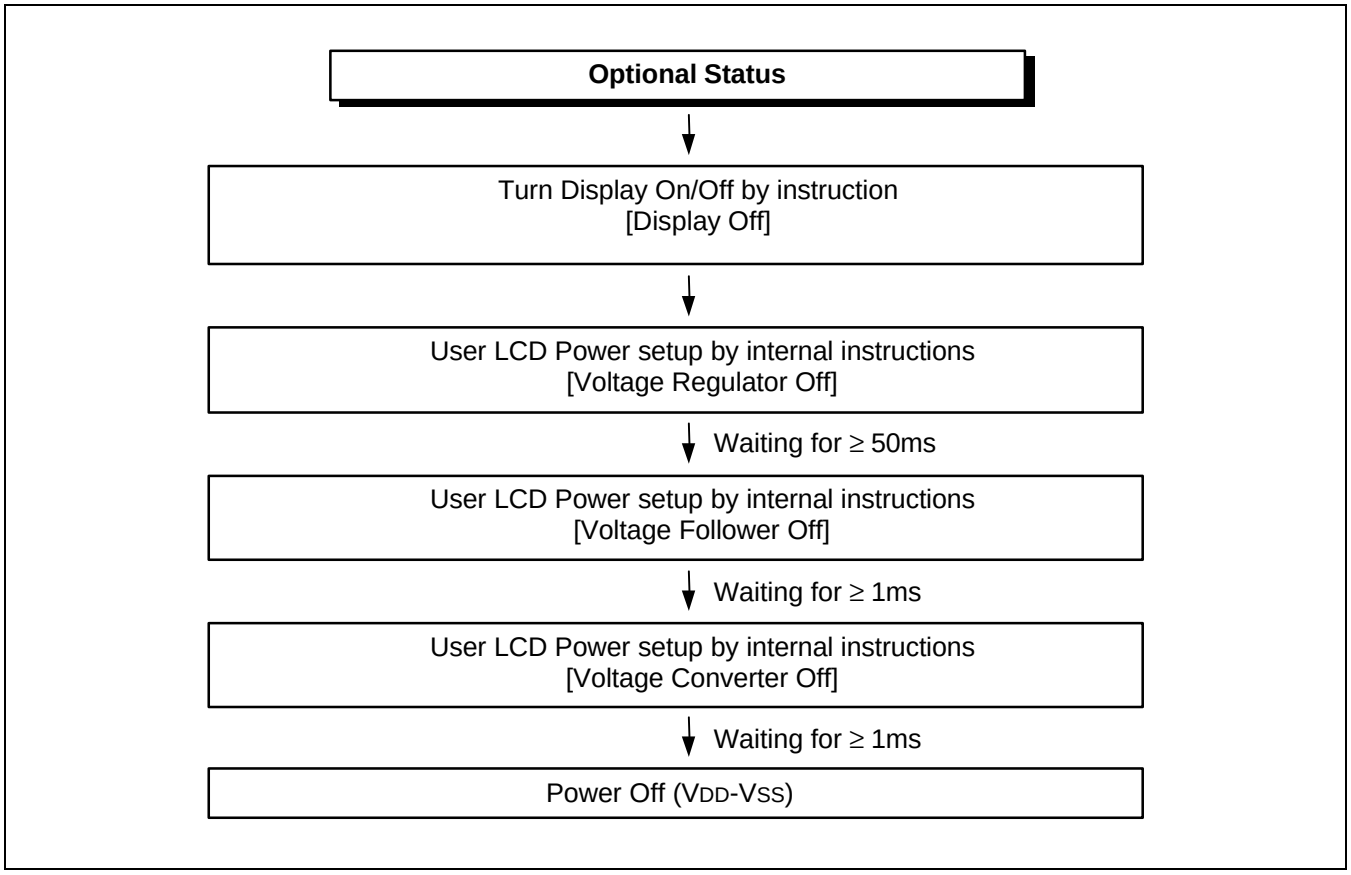


Figure 28. Power Off

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 20. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STR}	-55 to +125	°C

Notes:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V_{SS} must always be satisfied.(V_{LCD} = V0 – V_{SS})
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 21. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin used
Operating voltage(1)		V_{DD}		2.4	-	5.5	V	V_{DD} *1
Operating voltage(2)		V0		4.0	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Operating frequency		f_{OSC}	Ta = 25°C REXT = 250kΩ	58	82	106	kHz	OSSCK
Voltage converter Input voltage		V_{DD}	× 2	2.4	-	5.5	V	V_{DD}
			× 3	2.4	-	5.0		
			× 4	2.4	-	3.75		
			× 5	2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		4.0	-	15.0	V	VOUT
Voltage follower operating voltage		V0		4.0	-	15.0	V	V0 *8
Reference voltage		V_{REF}	Ta = 25°C	2.04	2.1	2.16	V	*9

Dynamic Current Consumption (1) when the built-in Power circuit is OFF (At operate mode)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption(1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 8.0V 1/65 Duty ratio Display Pattern OFF	-	-	50	μA	*10

Dynamic Current Consumption (2) when the built-in power circuit is ON (At operate mode)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD}=3.0V, quad boosting, V0 - V_{SS}=8.0V, 1/65 Duty ratio, Display Pattern OFF, Normal Power Mode	-	-	150	μA	*11
		V_{DD}=3.0V, quad boosting, V0 - V_{SS}=8.0V, 1/65 Duty ratio, Display Pattern Checker, Normal Power Mode	-	-	200	μA	*11

Dynamic Current Consumption (3) when the built-in power circuit is OFF (At access mode)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption (3)	I_{DD3}	V_{DD}=3.0V, V0 - V_{SS}=8.0V, fcyc = 1MHz	-		1	mA	

Current Consumption during Power Save mode

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Sleep mode current	I_{DDS1}	During Sleep	-	-	2.0	μA	
Standby mode current	I_{DDS2}	During Standby	-	-	20.0	μA	

[* Remark Solves]

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.

*2 In case of external power supply is applied.

*3 CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, DCDC5B, CLS, CL, M, DISP, OSCCK pins.

*4 DB0 to DB7, M, FRS, DISP, CL, OSCCK pins.

*5 CS1B, CS2, RS, DB[7:0], E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, DCDC5B, CLS pins.

*6 Applies when the DB[7:0], M, DISP, OSCCK and CL pins are in high impedance.

*7 Resistance value when ± 0.1[mA] is applied during the On status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)

*8 The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range

*9 On-chip reference voltage source of the voltage regulator circuit to adjust V0.

*10,11 Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is on or off.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc

REFERENCE DATA

IDD1 vs. VDD

* Test condition: Temperature: 25°C & 85°C, V0 = 8V(External), REXT=250 [kΩ], 65 Duty

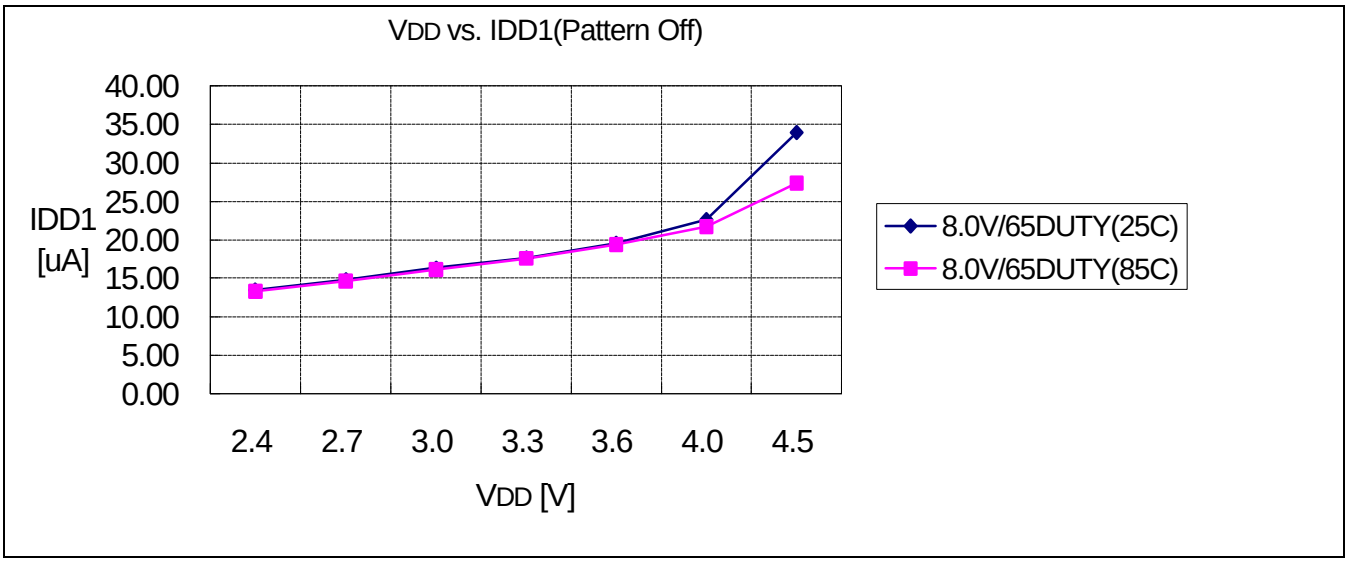


Figure 29. Display Pattern is Off

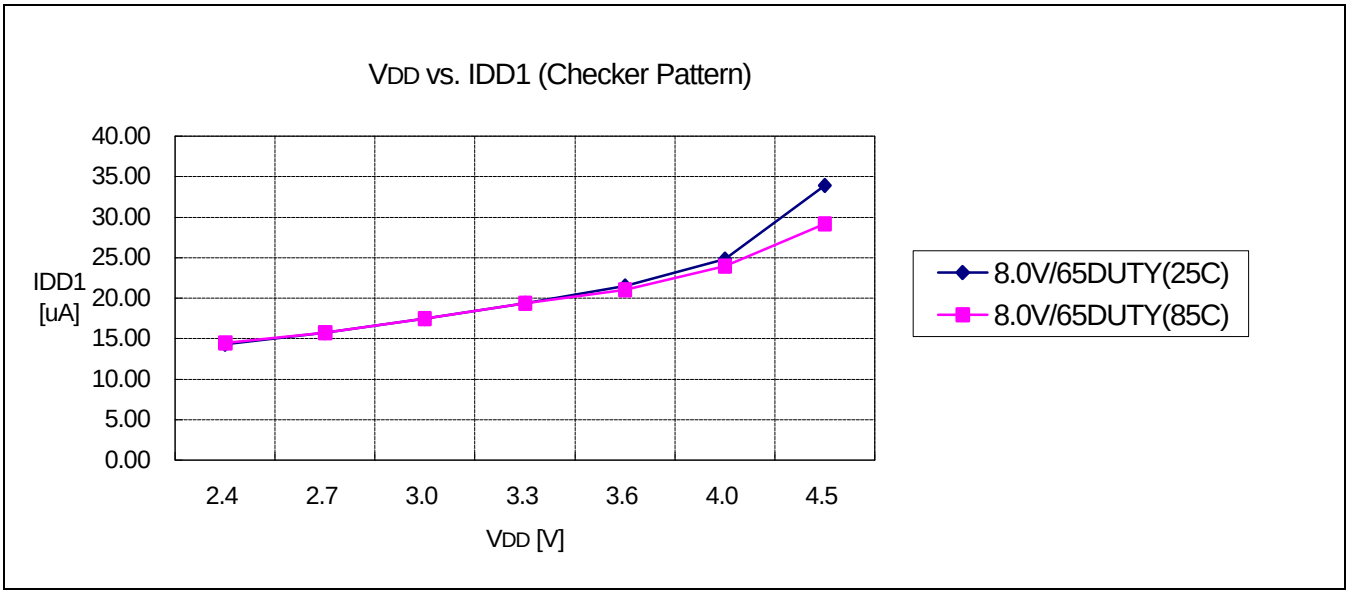


Figure 30. Display Pattern is Checker

IDD2 vs. VDD

* Test condition: Temperature: 25°C & 85°C, Three times boosting, RR=6, EV=32, REXT=250 [kΩ]

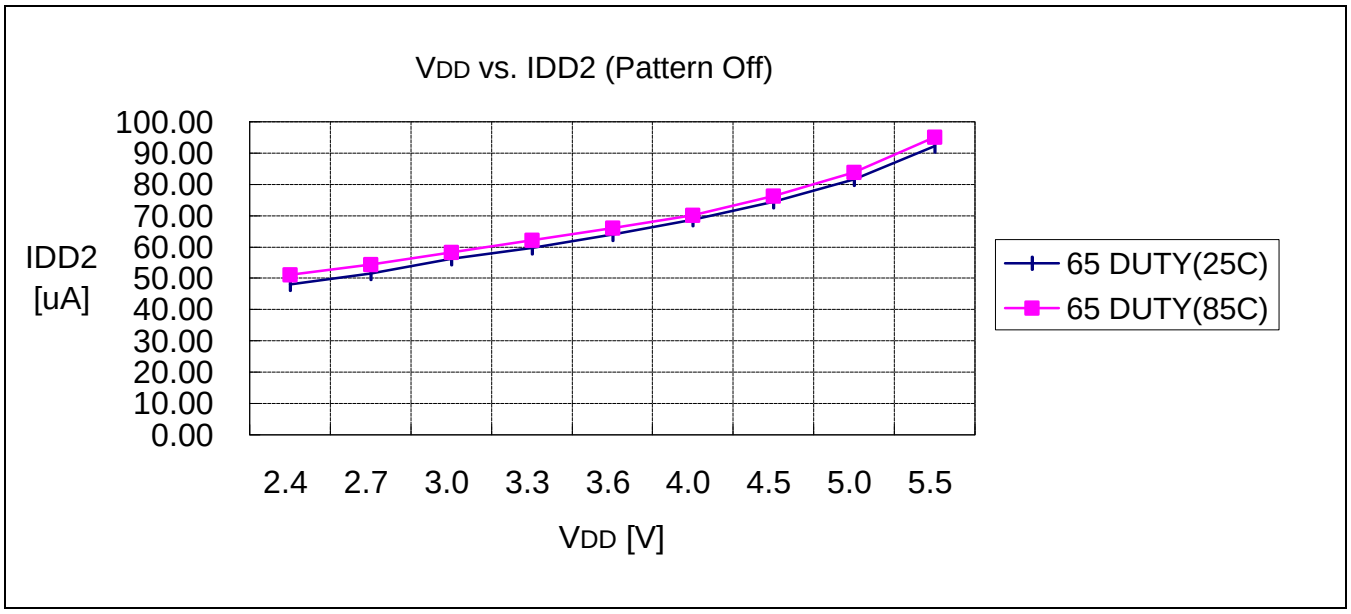


Figure 31. Display Pattern is Off

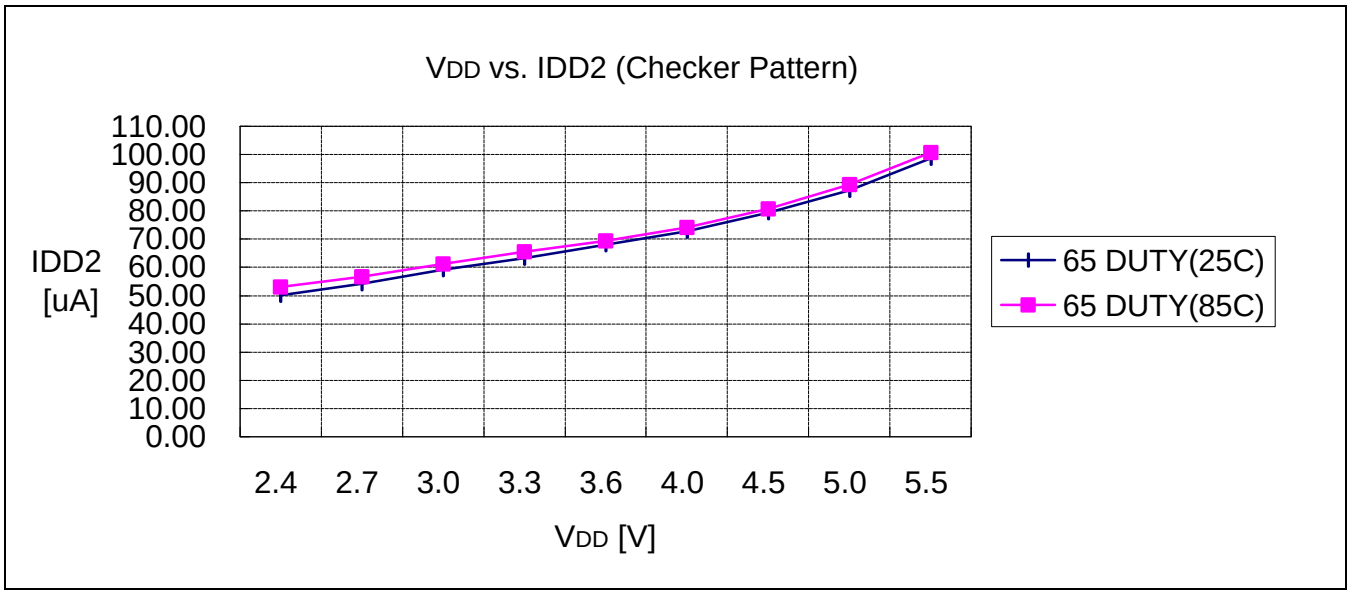


Figure 32. Display Pattern is Checker

AC Characteristics

Read / Write characteristics (8080-series MPU)

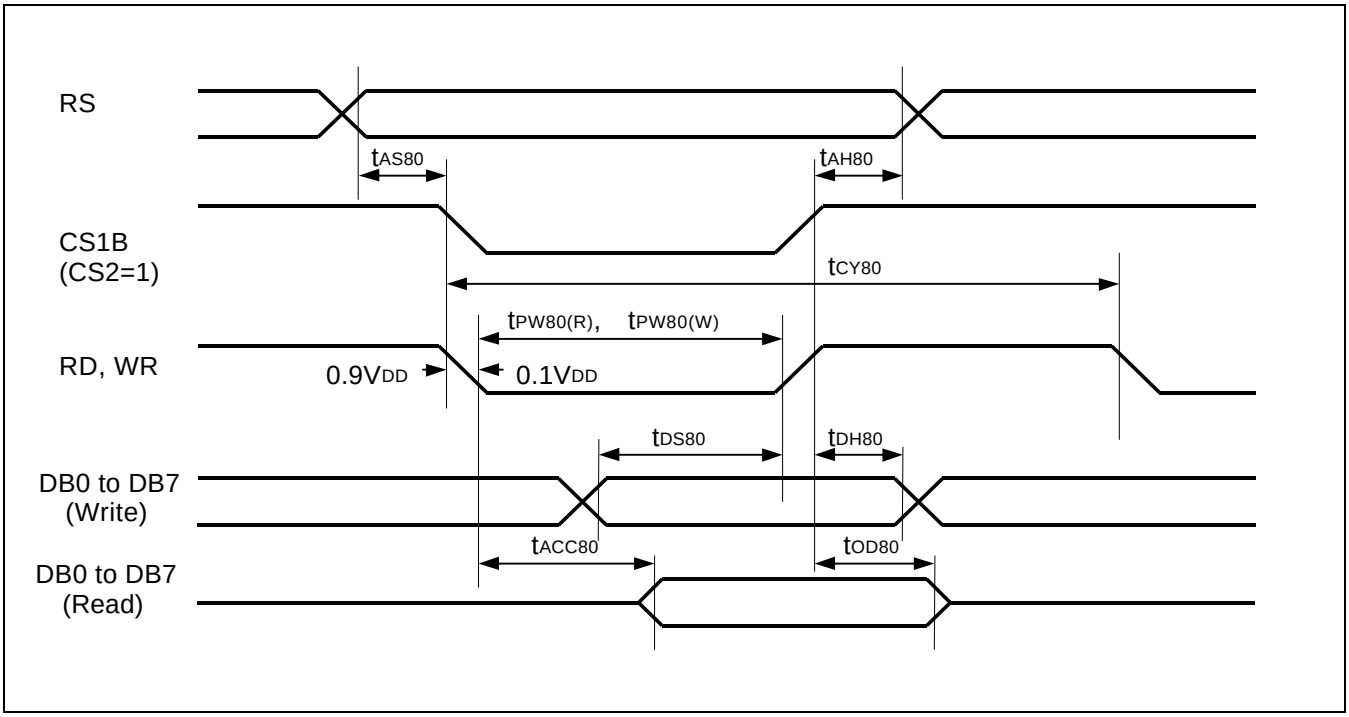


Figure 33. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}	13 17	-	-	ns	
System Cycle time	RS	t_{CY80}	400	-	-	ns	
Pulse Width(WR)	RW_WR	$t_{PW80(W)}$	55	-	-	ns	
Pulse Width(RD)	E_RD	$t_{PW80(R)}$	125	-	-	ns	
Data Setup Time Data Hold Time	DB7 to DB0	t_{DS80} t_{DH80}	35 13	-	-	ns	
Read Access time Output Disable time		t_{ACC80} t_{OD80}	- 10	-	125 90	ns	C_L = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Address Setup Time Address Hold Time	RS	t_{AS80} t_{AH80}	10 10	-	-	ns	
System Cycle time	RS	t_{CY80}	150	-	-	ns	
Pulse Width(WR)	RW_WR	$t_{PW80(W)}$	25	-	-	ns	
Pulse Width(RD)	E_RD	$t_{PW80(R)}$	65	-	-	ns	
Data Setup Time Data Hold Time	DB7 to DB0	t_{DS80} t_{DH80}	18 10	-	-	ns	
Read Access time Output Disable time		t_{ACC80} t_{OD80}	- 10	-	65 45	ns	C_L = 100 pF

Read / Write characteristics (6800-series Microprocessor)

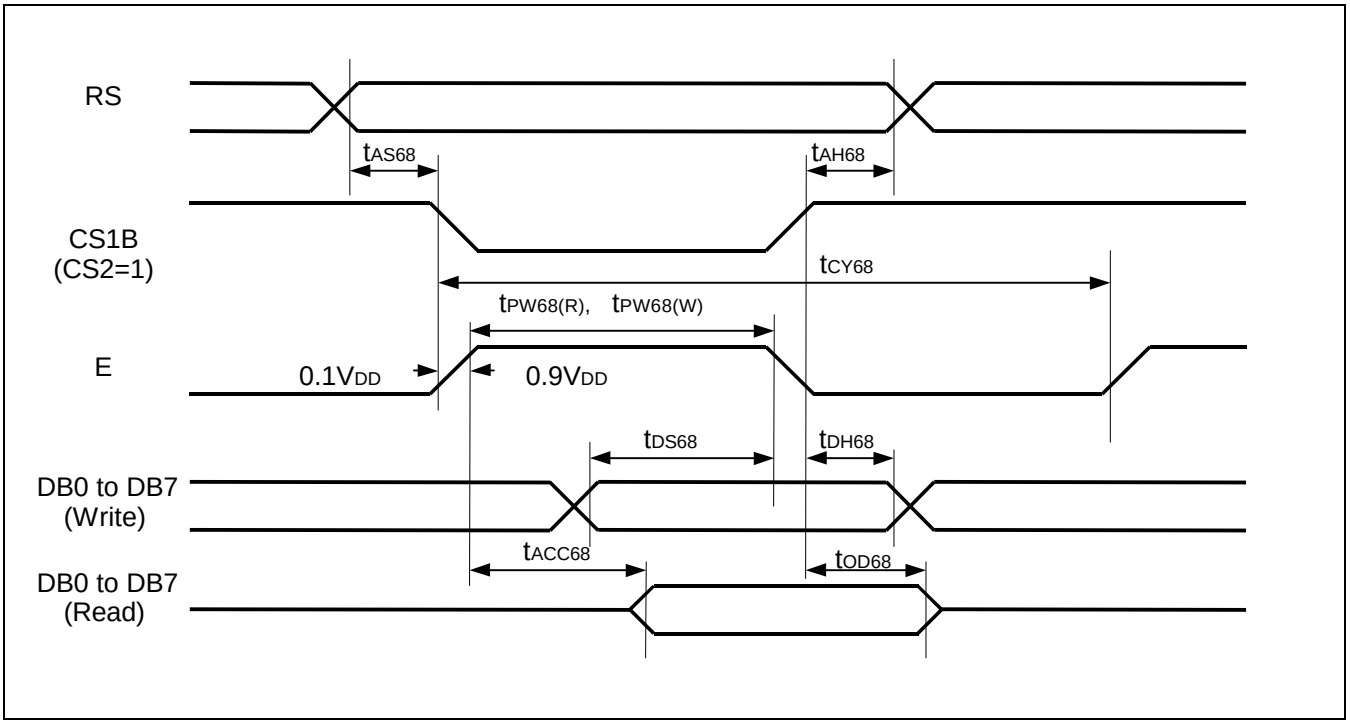


Figure 34. Read / Write characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.3V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min	Typ	Max	Unit	Remark
Address Setup Time Address Hold Time		RS	t_{AS68} t_{AH68}	13 17	-	-	ns	
System Cycle time		RS	t_{CY68}	400	-	-	ns	
Data Setup Time Data Hold Time		DB7 to DB0	t_{DS68} t_{DH68}	35 13	-	-	ns	
Access time Output Disable time			t_{ACC68} t_{OD68}	- 10	-	125 90	ns	C_L = 100 pF
Enable Pulse Width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	125 55	-	-	-	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min	Typ	Max	Unit	Remark
Address Setup Time Address Hold Time		RS	t_{AS68} t_{AH68}	10 10	-	-	ns	
System Cycle time		RS	t_{CY68}	150	-	-	ns	
Data Setup Time Data Hold Time		DB7 to DB0	t_{DS68} t_{DH68}	18 10	-	-	ns	
Access time Output Disable time			t_{ACC68} t_{OD68}	- 10	-	65 45	ns	C_L = 100 pF
Enable Pulse Width	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	65 25	-	-	-	

Serial Interface Characteristics

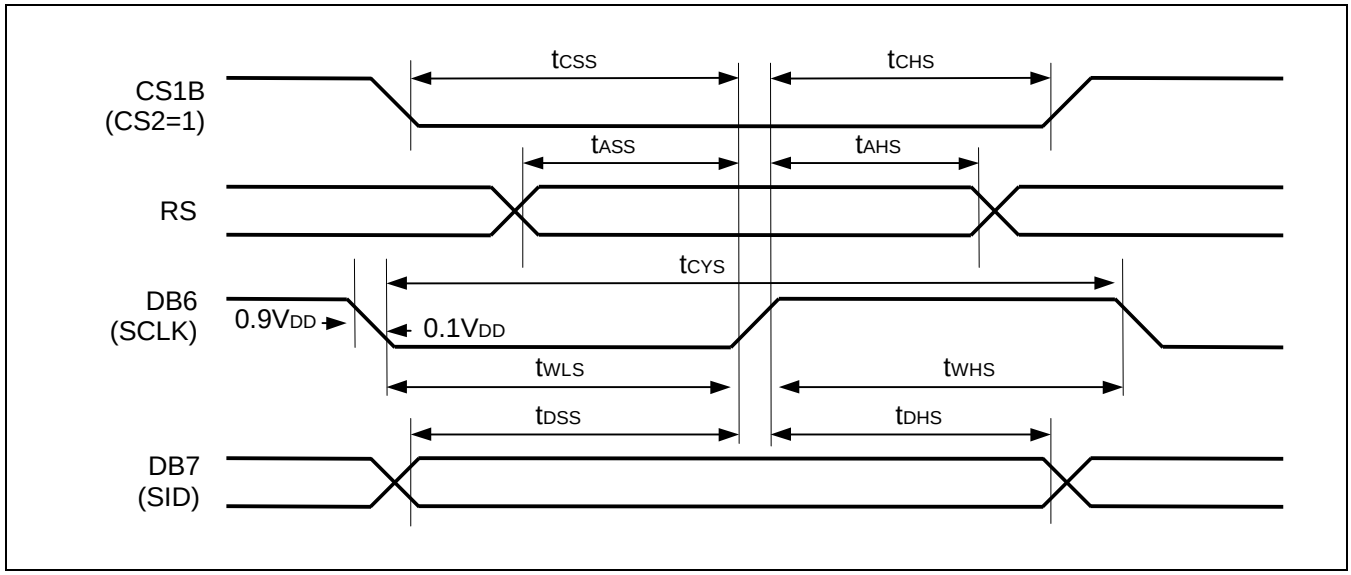


Figure 35. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Serial Clock Cycle SCLK High pulse Width SCLK Low pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	- - -	- - -	ns	
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}	90 360	- -	- -	ns	
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}	90 90	- -	- -	ns	
CS1B Setup Time CS1B Hold Time	CS1B	t_{CSS} t_{CHS}	55 180	- -	- -	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Serial Clock Cycle SCLK High pulse Width SCLK Low pulse Width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	225 90 70	- - -	- - -	ns	
Address Setup Time Address Hold Time	RS	t_{ASS} t_{AHS}	45 180	- -	- -	ns	
Data Setup Time Data Hold Time	DB7 (SID)	t_{DSS} t_{DHS}	45 45	- -	- -	ns	
CS1B Setup Time CS1B Hold Time	CS1B	t_{CSS} t_{CHS}	25 90	- -	- -	ns	

Reset Input Timing

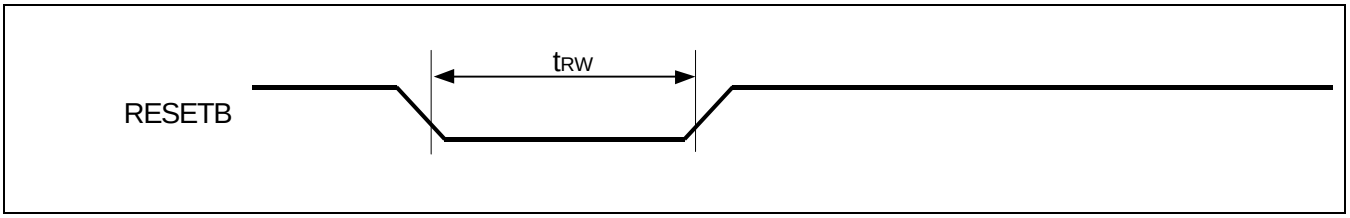


Figure 36. Reset Input Timing

(V_{DD} = 2.4 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Reset Low Pulse Width	RESETB	t_{RW}	900	-	-	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
Reset Low Pulse Width	RESETB	t_{RW}	450	-	-	ns	

Display Control Output Timing

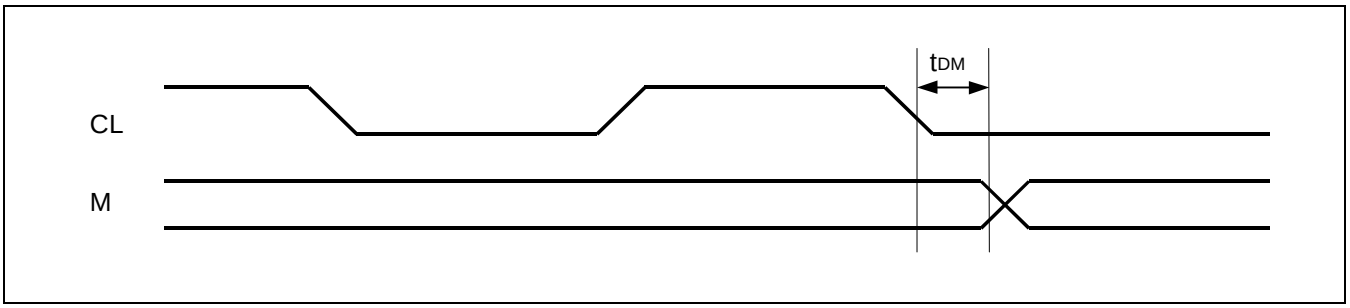


Figure 37. Display Control Output Timing

(V_{DD} = 2.4 to 3.3V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
M Delay Time	M	t_{DM}	-	13	70	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min	Typ	Max	Unit	Remark
M Delay Time	M	t_{DM}	-	10	35	ns	

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In case of interfacing with 6800-series (PS = “H”, C68 = “H”)

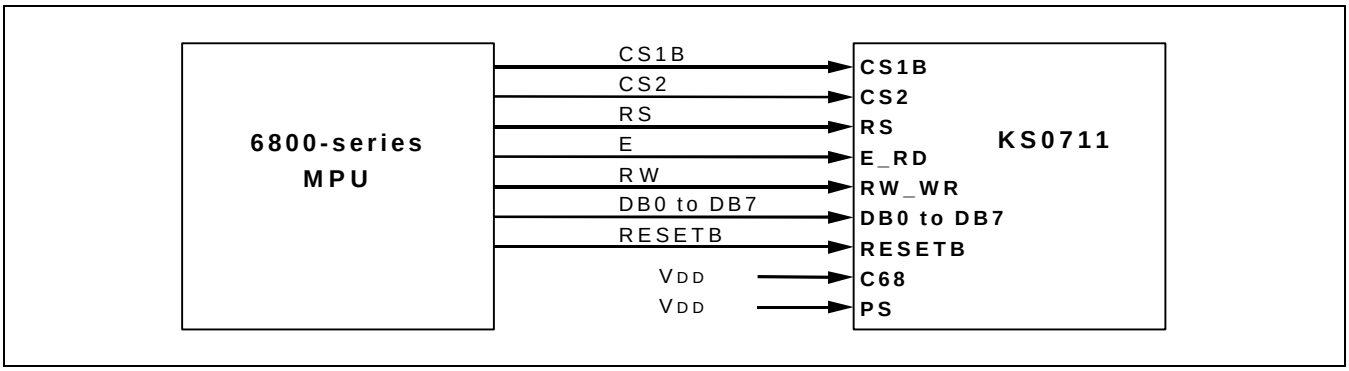


Figure 38. Interfacing with 6800-series (PS = “H”, C68 = “H”)

In case of interfacing with 8080-series (PS = “H”, C68 = “L”)

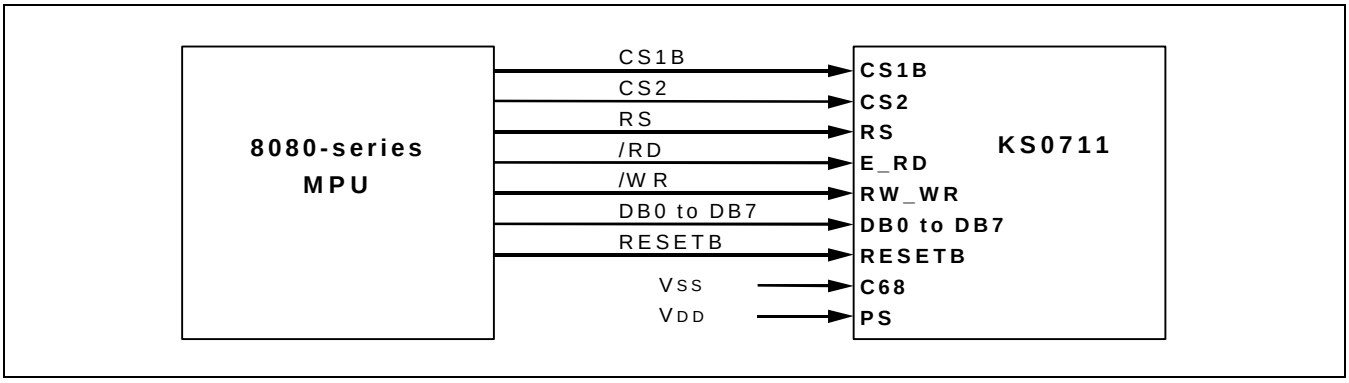


Figure 39. Interfacing with 8080-series (PS = “H”, C68 = “L”)

In case of serial interface (PS = “L”, C68 = “H/L”)

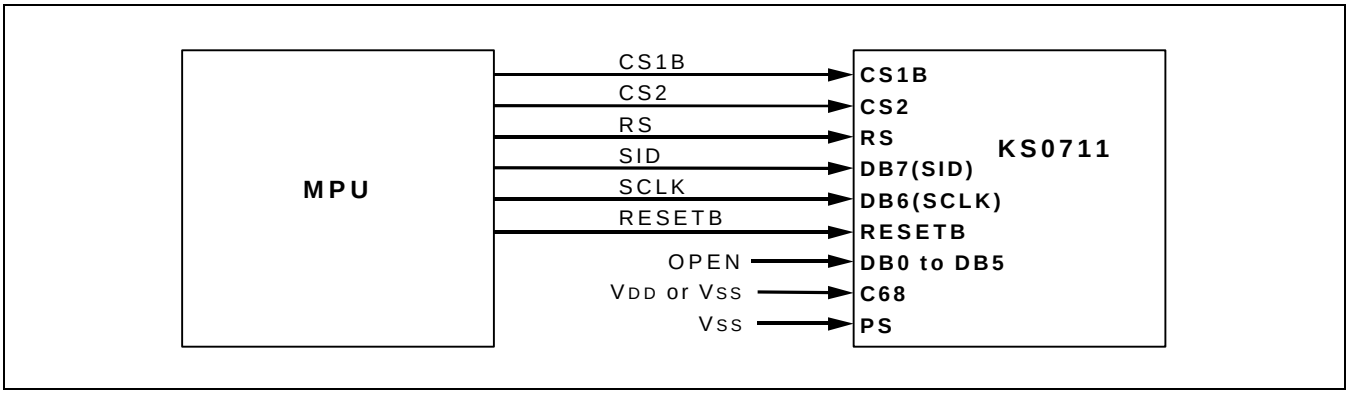


Figure 40. Serial interface (PS = “L”, C68 = “H/L”)

CONNECTIONS BETWEEN KS0711 AND LCD PANEL

Single Chip Configuration (1/65 Duty configurations)

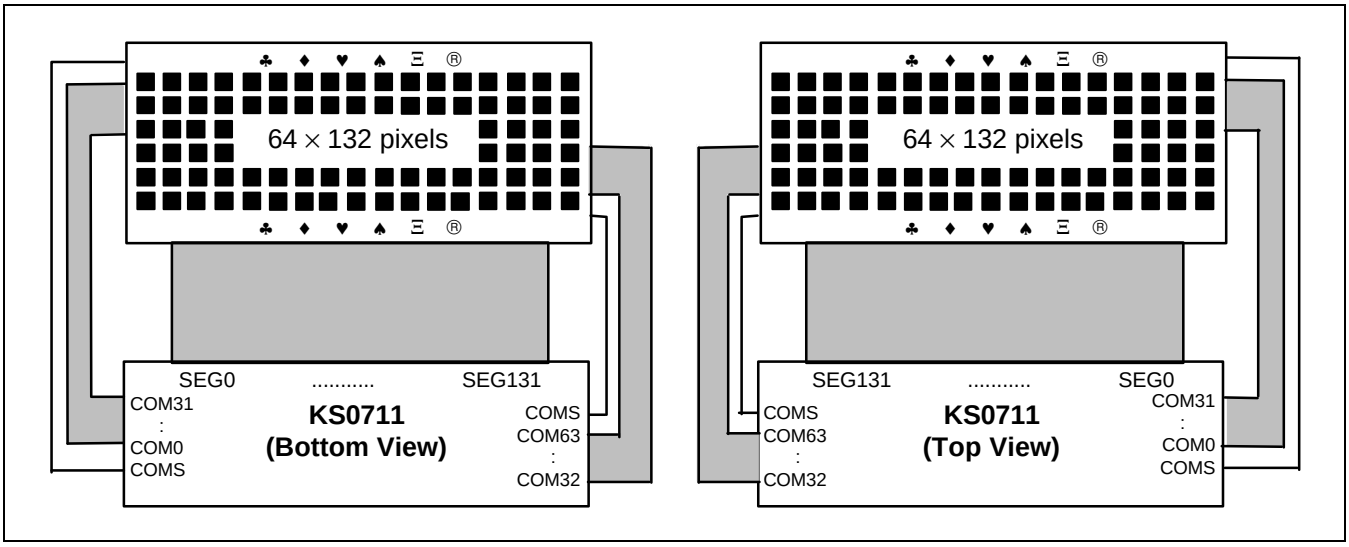


Figure 41. SHL = 0, ADC = 0

Figure 42. SHL = 0, ADC = 1

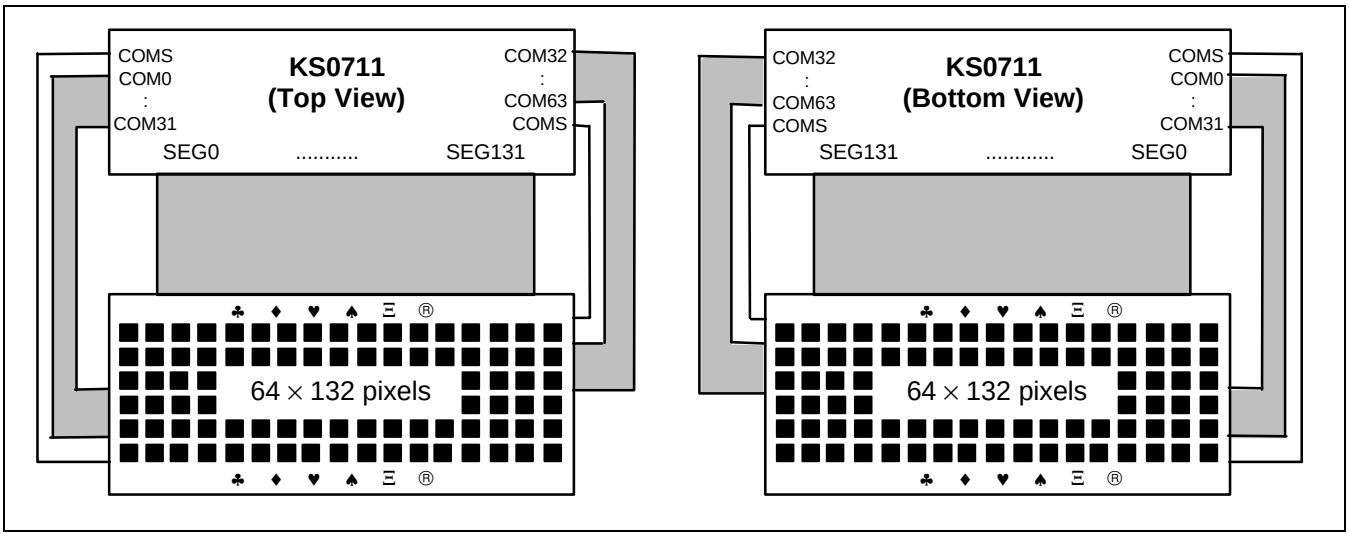


Figure 43. SHL = 1, ADC = 0

Figure 44. SHL = 1, ADC = 1

Single Chip Configuration (1/49 Duty configurations)

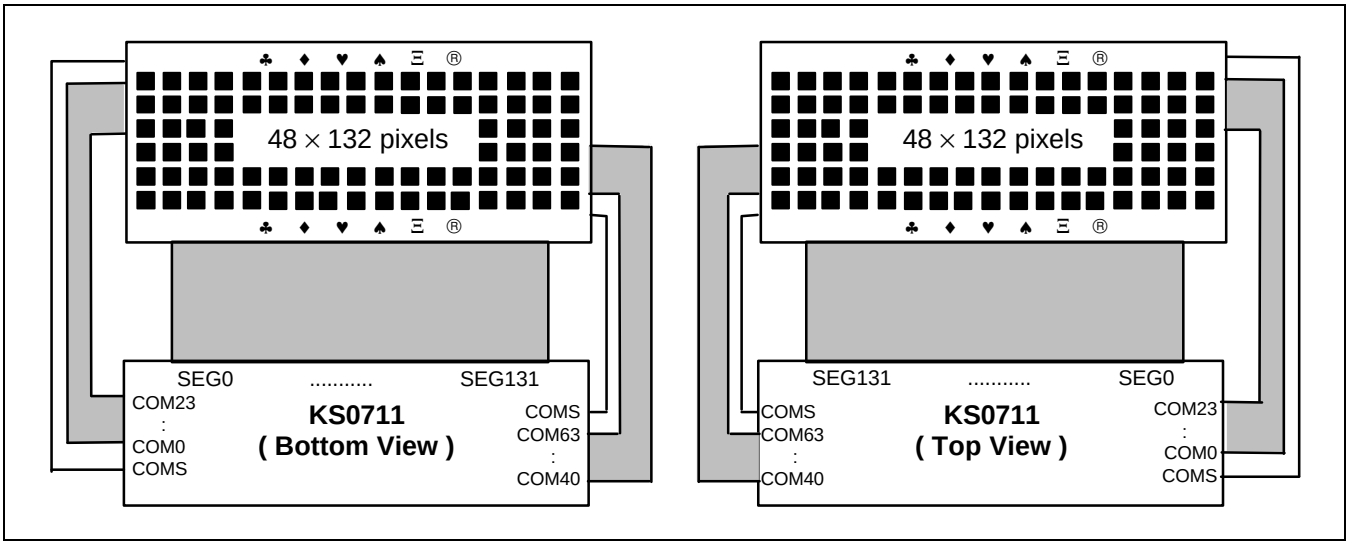


Figure 45. SHL = 0, ADC = 0

Figure 46. SHL = 0, ADC = 1

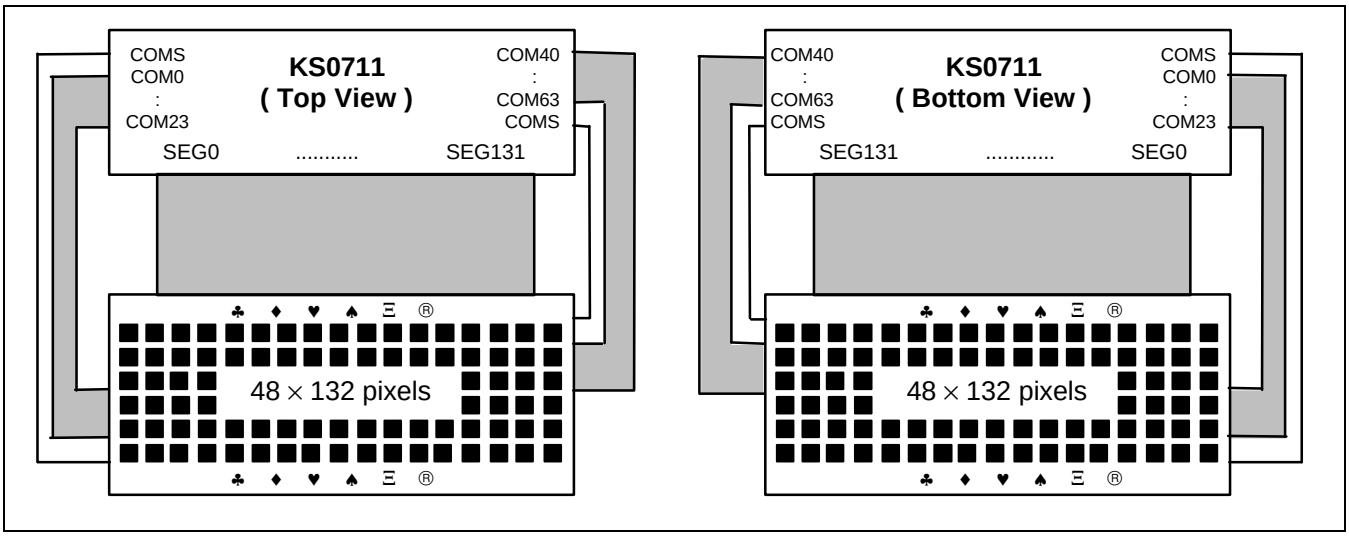


Figure 47. SHL = 1, ADC = 0

Figure 48. SHL = 1, ADC = 1

Single Chip Configuration (1/33 Duty configurations)

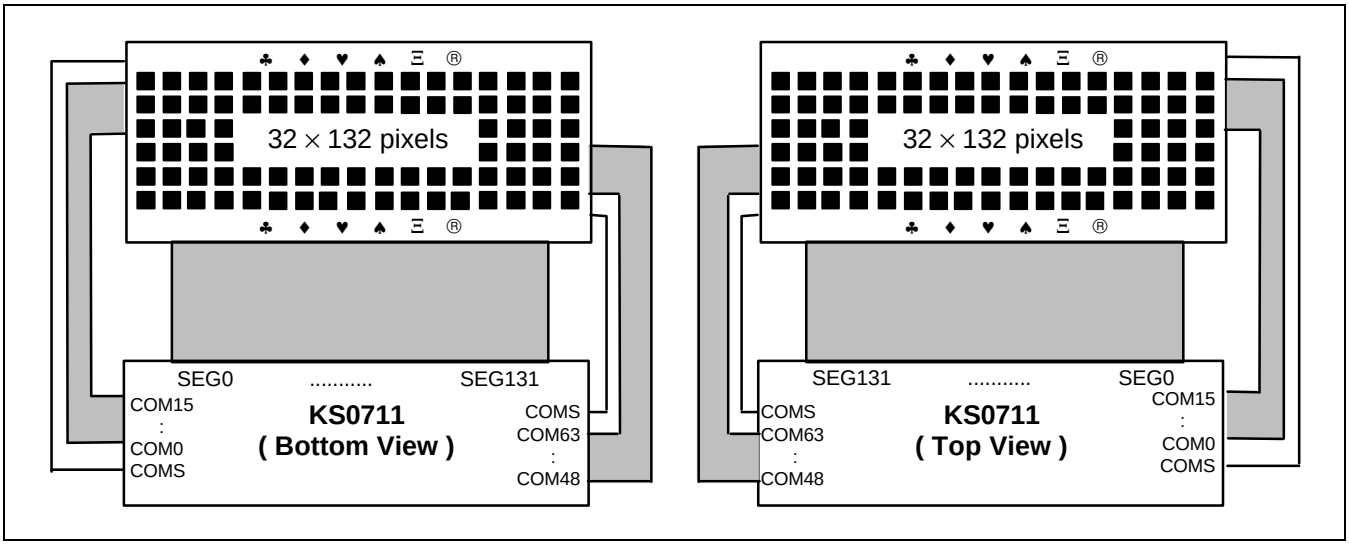


Figure 49. SHL = 0, ADC = 0

Figure 50. SHL = 0, ADC = 1

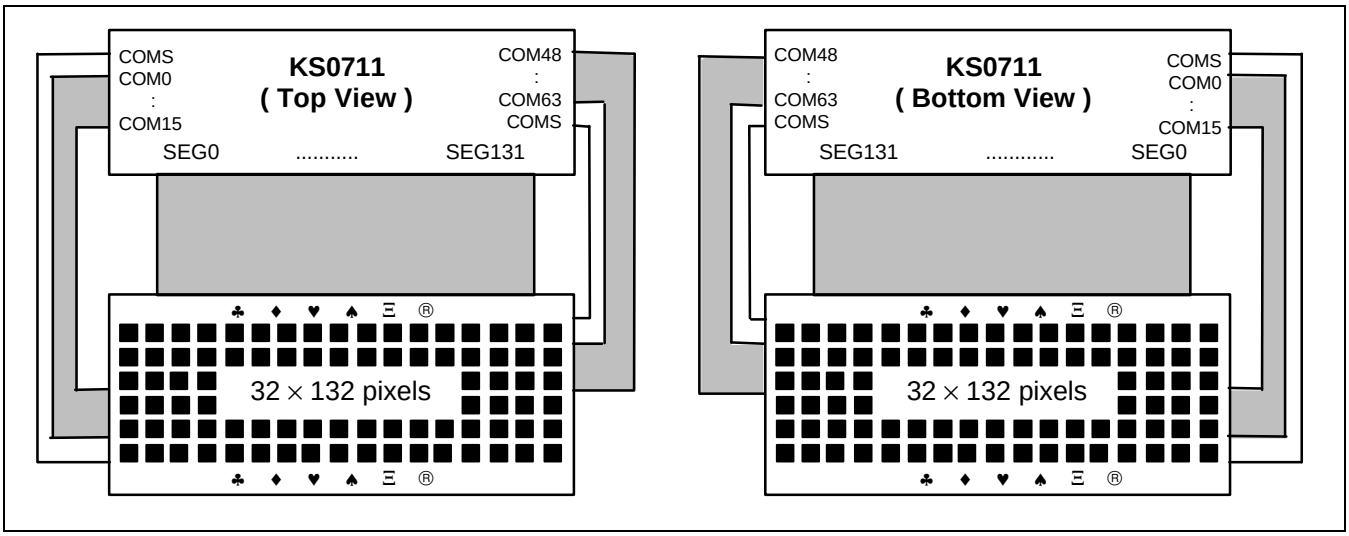


Figure 51. SHL = 1, ADC = 0

Figure 52. SHL = 1, ADC = 1

Multiple Chip Configuration

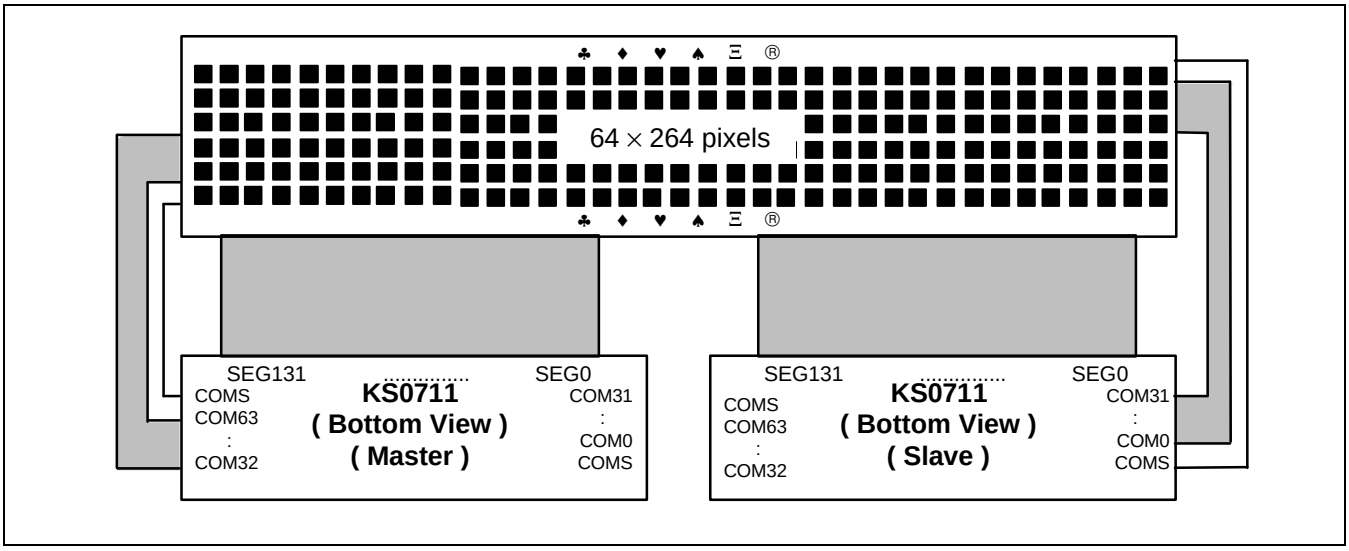


Figure 53. SHL = 0, ADC = 1

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M, OSCCK
  - Display Control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

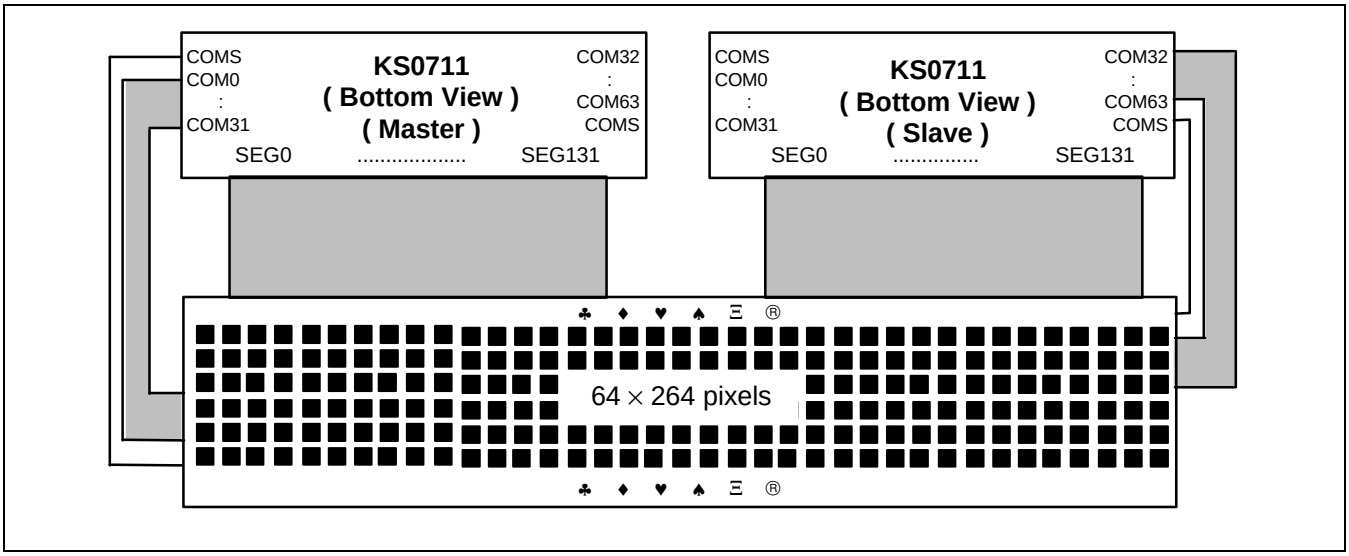


Figure 54. SHL = 1, ADC = 0

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M, OSCCK
  - Display Control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4