11 32-BIT TIMERS

OVERVIEW

The KS32C50100 has two 32-bit timers. These timers can operate in interval mode or in toggle mode. The output signals are TOUT0 and TOUT1, respectively.

You enable or disable the timers by setting control bits in the timer control register, TCON. An interrupt request is generated whenever a timer count-out (down count) occurs.

INTERVAL MODE OPERATION

In interval mode, a timer generates a one-shot pulse of a preset timer clock duration whenever a time-out occurs. This pulse generates a time-out interrupt that is directly output at the timer's configured output pin (TOUTn). In this case, the timer frequency monitored at the TOUTn pin is calculated as:

$f_{TOUT} = f_{MCLK}$ / Timer data value

TOGGLE MODE OPERATION

In toggle mode, the timer pulse continues to toggle whenever a time-out occurs. An interrupt request is generated whenever the level of the timer output signal is inverted (that is, when the level toggles). The toggle pulse is output directly at the configured output pin.

Using toggle mode, you can achieve a flexible timer clock range with 50% duty. In toggle mode, the timer frequency monitored at the TOUTn pin is calculated as follows:

$f_{TOUT} = f_{MCLK}$ / (2 * Timer data value)

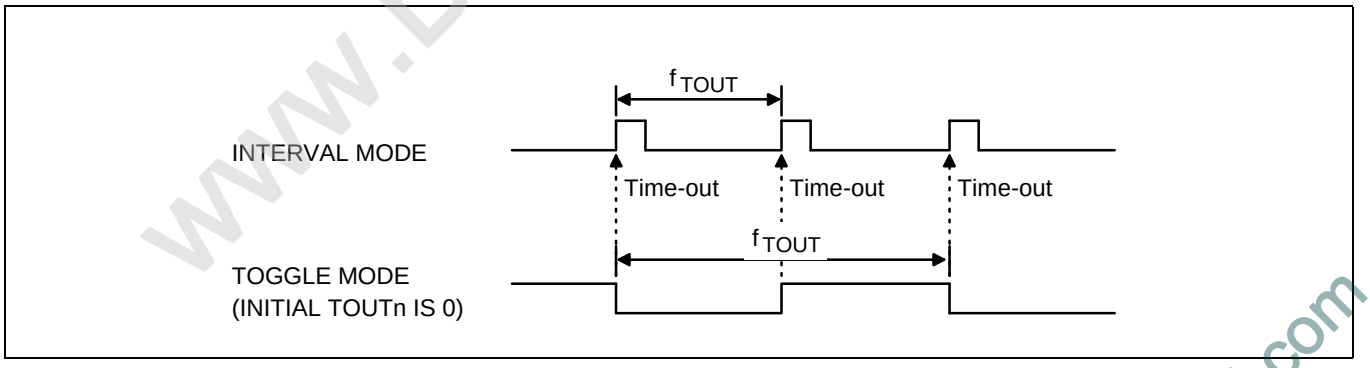


Figure 11-1 Timer Output Siganl Timing

TIMER OPERATION GUIDELINES

The block diagram in Figure 11-2 shows how the 32-bit timers are configured in the KS32C50100. The following guidelines apply to timer functions.

- When a timer is enabled, it loads a data value to its count register and begins decrementing the count register value.
- When the timer interval expires, the associated interrupt is generated. The base value is then reloaded and the timer continues decrementing its count register value.
- If a timer is disabled, you can write a new base value into its registers.
- If the timer is halted while it is running, the base value is not automatically re-loaded.

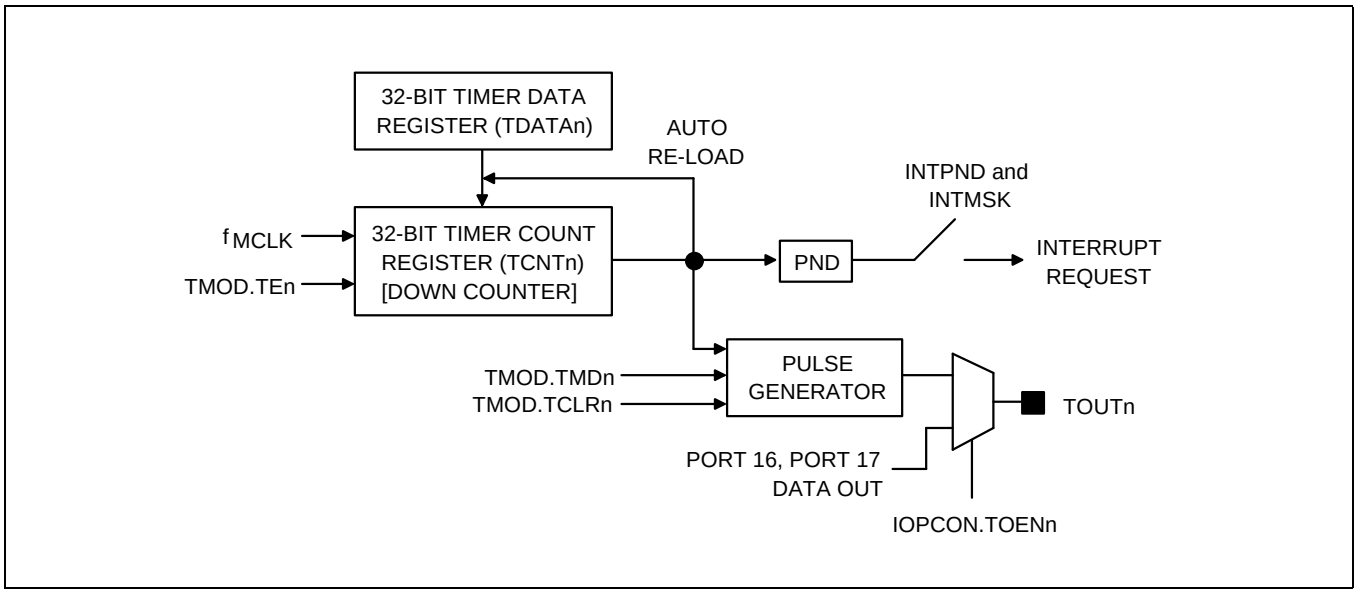


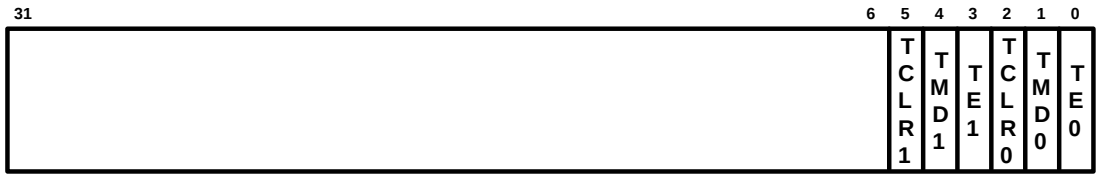
Figure 11-2 32-Bit Timer Block Diagram

TIMER MODE REGISTER

The timer mode register, TMOD, is used to control the operation of the two 32-bit timers. TMOD register settings are described in Figure 11-3.

Table 11-1 TMOD Register

Register	Offset Address	R/W	Description	Reset Value
TMOD	0x6000	R/W	Timer mode register	32'h00000000



[0] Timer 0 enable (TE0)
0 = Disable timer 0
1 = Enable timer 0

[1] Timer 0 mode selection (TMD0)
0 = Interval mode
1 = Toggle mode

[2] Timer 0 initial TOUT0 value (TCLR0)
0 = Initial TOUT0 is 0 in toggle mode
1 = Initial TOUT0 is 1 in toggle mode

[3] Timer 1 enable (TE1)
0 = Disable timer 1
1 = Enable timer 1

[4] Timer 1 mode seletion (TMD1)
0 = Interval mode
1 = Toggle mode

[5] Timer 1 initial TOUT1 value (TCLR1)
0 = Initial TOUT1 is 0 in toggle mode
1 = Initial TOUT1 is 1 in toggle mode

Figure 11-3 Timer Mode Register (TMOD)

TIMER DATA REGISTERS

The timer data registers, TDATA0 and TDATA1, contain a value that specifies the time-out duration for each timer. The formula for calculating the time-out duration is: (Timer data + 1) cycles.

Table 11-2 TDATA0 and TDATA1 Registers

Register	Offset Address	R/W	Description	Reset Value
TDATA0	0x6004	R/W	Timer 0 data register	0x00000000
TDATA1	0x6008	R/W	Timer 1 data register	0x00000000

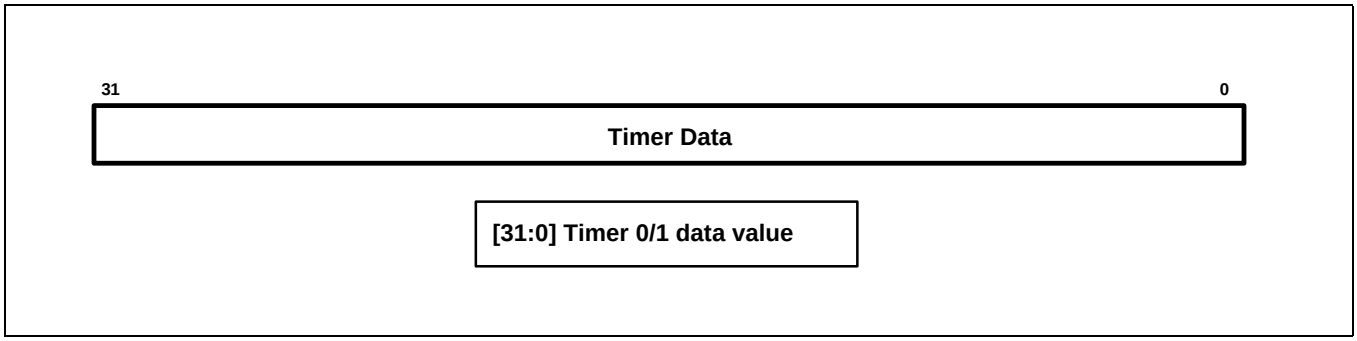


Figure 11-4 Timer Data Registers (TDATA0, TDATA1)

TIMER COUNT REGISTERS

The timer count registers, TCNT0 and TCNT1, contain the current timer 0 and 1 count value, respectively, during normal operation.

Table 11-3 TCNT0 and TCNT1 Registers

Register	Offset Address	R/W	Description	Reset Value
TCNT0	0x600C	R/W	Timer 0 count register	0xffffffff
TCNT1	0x6010	R/W	Timer 1 count register	0xffffffff

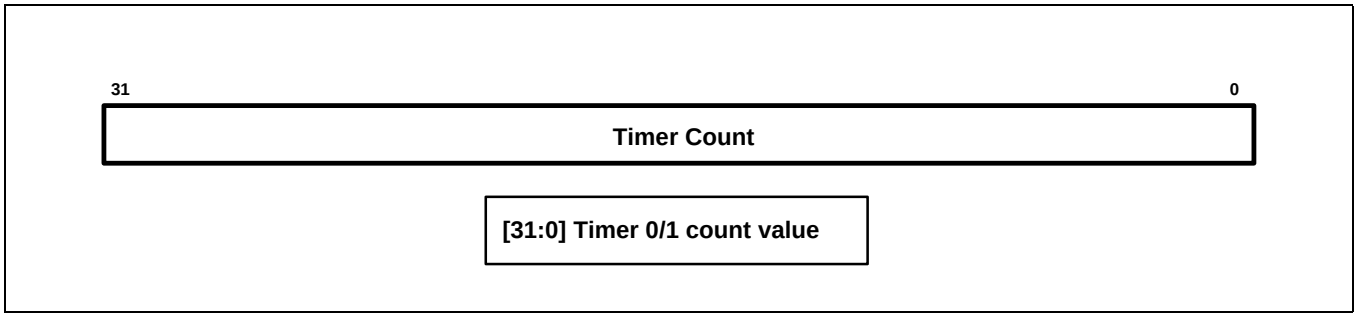


Figure 11-5 Timer Count Registers (TCNT0, TCNT1)

NOTES