DESCRIPTION

The KS57C0002/0004 single-chip 4-bit microcontroller is fabricated using an advanced CMOS process. With comparator inputs, high-current LED direct drive pins, serial I/O interface, and a versatile 8-bit timer/counter, the KS57C0002/0004 offers an excellent design solution for a wide range of general applications.

FEATURES

Memory

- 256 x 4-bit data memory (KS57C0002)
  512 x 4-bit data memory (KS57C0004)
- 2048 x 8-bit program memory (KS57C0002)
  4096 x 8-bit program memory (KS57C0004)

24 I/O Pins

- I/O: 18 pins, including 8 high-current pins
- Input-only: 6 pins

Comparator

- 4-channel mode: internal reference, 4-bit resolution; 16-step variable reference voltage
- 3-channel mode: external reference, 150 mV resolution (worst case)

8-Bit Basic Timer

- Programmable interval timer

8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter clock output to TCLO0 pin

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- Four frequency outputs to BUZ pin

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive-only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Interrupts

- Two external interrupt vectors
- Three internal interrupt vectors
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode: only CPU clock stops
- Stop mode: system clock stops

Oscillation Sources

- Crystal, ceramic, or RC for system clock
- Crystal/ceramic: 4.19 MHz (typical)
- RC: 1 MHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz

Operating Temperature

- – 40 °C to 85 °C

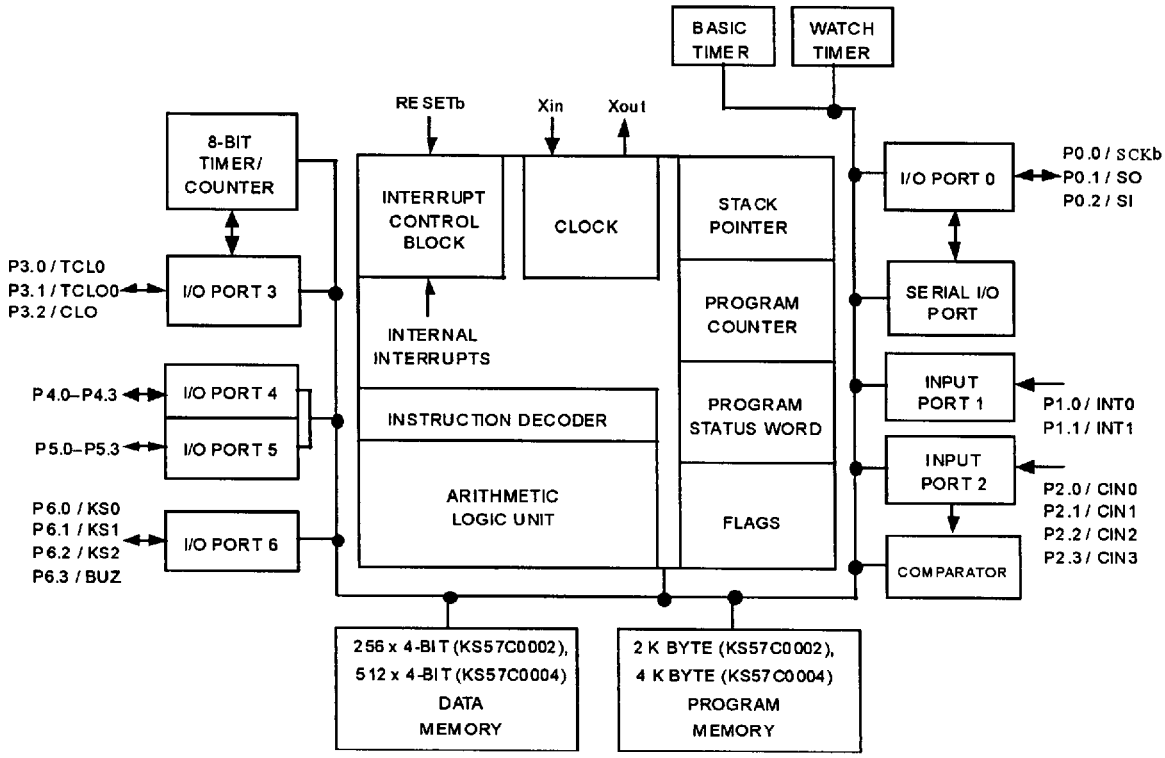
Operating Voltage Range

- 2.7 V to 6.0 V

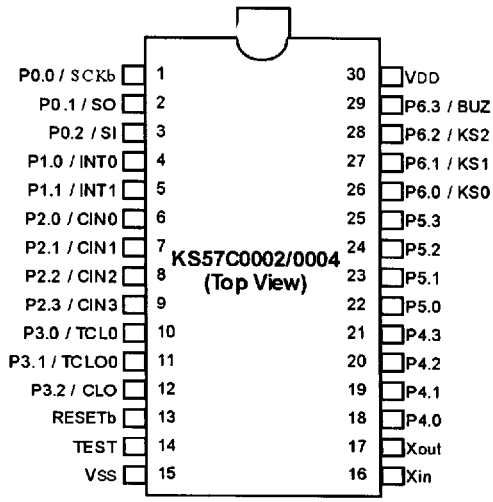
Package Types

- 30-pin SDIP, 32-pin SOP

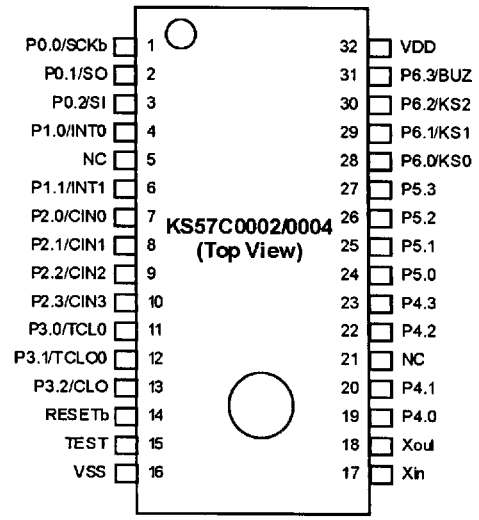
BLOCK DIAGRAM



PIN ASSIGNMENTS



30-pin SDIP



32-pin SOP

PIN DESCRIPTIONS

Pin Name	Pin Type	Description	Pin Number	Share Pin
P0.0 P0.1 P0.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	1 (1) 2 (2) 3 (3)	SCKb SO SI
P1.0 P1.1	I	2-bit input port. 1-bit or 2-bit read and test is possible. Pull-up resistors are assignable by software.	4 (4) 5 (6)	INT0 INT1
P2.0–P2.3	I	4-bit input port. 1-bit or 4-bit read and test is possible.	6–9 (7–10)	CIN0–CIN3
P3.0 P3.1 P3.2	I/O	Same as port 0	10 (11) 11 (12) 12 (13)	TCL0 TCLO0 CLO
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-, or 8-bit read/write and test is possible. Pins are individually configurable as input or output. Ports can be configurable as n-channel, open-drain by mask option (maximum 9V).	18–21 (19–23) 22–25 (24–27)	–
P6.0 P6.1 P6.2 P6.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	26 (28) 27 (29) 28 (30) 29 (31)	KS0 KS1 KS2 BUZ
INT0	I	External interrupts with detection of rising and falling edges	4 (4)	P1.0
INT1	I	External interrupts with detection of rising or falling edges	5 (6)	P1.1
CIN0–CIN3	I	4-channel comparator input. CIN0–CIN2: comparator input only. CIN3: comparator input or external reference input	6–9 (7–10)	P2.0–P2.3
SCKb	I/O	Serial interface clock signal	1 (1)	P0.0
SO	I/O	Serial data output	2 (2)	P0.1
SI	I/O	Serial data input	3 (3)	P0.2
TCL0	I/O	External clock input for timer/counter	10 (11)	P3.0
TCLO0	I/O	Timer/counter clock output	11 (12)	P3.1
CLO	I/O	CPU clock output	12 (13)	P3.2
BUZ	I/O	2-kHz, 4-kHz, 8-kHz, or 16-kHz frequency output at 4.19 MHz for buzzer sound	29 (31)	P6.3

NOTE: Pin numbers shown in parentheses '( )' are for the 32-pin SOP package; other pin numbers are for the 30-pin SDIP package.

PIN DESCRIPTIONS (Continued)

Pin Name	Pin Type	Description	Pin Number	Share Pin
KS0–KS2	I/O	Quasi-interrupt input with falling edge detection	26–28 (28–30)	P6.0–P6.2
V_{DD}	–	Main power supply	30 (32)	–
V_{SS}	–	Ground	15 (16)	–
RESETb	I	RESETb signal	13 (14)	–
TEST	I	Test signal input (must be connected to V_{SS})	14 (15)	–
X_{IN}, X_{OUT}	–	Crystal, ceramic, or RC oscillator signal for system clock	16 (17) 17 (18)	–

NOTE: Pin numbers shown in parentheses '( )' are for the 32-pin SOP package; other pin numbers are for the 30-pin SDIP package.

FUNCTION OVERVIEW

SAM4 CPU

All KS57-series microcontrollers have the advanced SAM4 CPU core. The SAM4 CPU can directly address up to 32 K bytes of program memory. The arithmetic logic unit (ALU) performs 4-bit addition, subtraction, logical, and shift-and-rotate operations in one instruction cycle and most 8-bit arithmetic and logical operations in two cycles.

CPU REGISTERS

Program Counter

A 11-bit program counter (PC) stores addresses for instruction fetch during program execution. Usually, the PC is incremented by the number of bytes of the instruction being fetched. An exception is the 1-byte instruction REF which is used to reference instructions stored in a look-up table in the ROM.

Stack Pointer

An 8-bit stack pointer (SP) stores addresses for stack operations. The stack area is located in the general-purpose data memory bank 0. The SP is read or written by 8-bit instructions and SP bit 0 must always be set to logic zero.

PROGRAM MEMORY

In its standard configuration, the device's 2048 x 8-bit (KS57C0002), or 4096 x 8-bit (KS57C0004) program memory has four areas that are directly addressable by the program counter (PC):

— 16-byte general-purpose area

— 16-byte area for vector addresses

— 96-byte instruction reference area

— 1920-byte (KS57C0002), 3968-byte (KS57C0004) general-purpose area

The REF instruction references 2 ¥ 1-byte and 2-byte instructions stored in locations 0020H–007FH. The REF instruction can also reference three-byte instructions such as JP or CALL. So that a REF instruction can reference these instructions, however, JP or CALL must be shortened to a 2-byte format. To do this, JP or CALL is written to the reference area with the format TJP or TCALL instead of the normal instruction name. Unused locations in the reference area can be used as general-purpose registers.

DATA MEMORY

Overview

The 256 x 4-bit (KS57C0002), or the 512 x 4-bit (KS57C0004) data memory has four areas:

— 32 x 4-bit working registers

— 224 x 4-bit general-purpose area in bank0 which is also used as the stack area

— 256¥x 4-bit general-purpose area in bank1 **(KS57C0004 only)**

— 128 x 4-bit area in bank 15 for memory-mapped I/O addresses

Data Memory Addressing Modes

The enable memory bank (EMB) flag controls the addressing mode for data memory banks 0 or 15. When the EMB flag is logic zero, restricted area can be accessed. When the EMB flag is set to logic one, all two data memory banks can be accessed according to the current SMB value.

Working Registers

The RAM's working register area in data memory bank 0 is further divided into four *register* banks. Each register bank has eight 4-bit registers that are addressable either by 1-bit or 4-bit instructions. Paired 4-bit registers can be addressed as double registers by 8-bit instructions.

Register A is the 4-bit accumulator and double register EA is the 8-bit extended accumulator. Double registers WX, WL, and HL are used as data pointers for indirect addressing. Unused working registers can be used as general-purpose memory.

CONTROL REGISTERS

Select Bank (SB) Register

Two 4-bit registers store address values used to access specific memory and register banks: the select memory bank register, SMB, and the select register bank register, SRB.

The 'SMB n' instruction selects a data memory bank (0 or 15) and stores the upper four bits of the 12-bit data memory address in the SMB register. To select register bank 0, 1, 2, or 3, and store the address data in the SRB, you use the instruction 'SRB n'.

The instructions "PUSH SB" and "POP SB" move SRB and SMB values to and from the stack for interrupts and subroutines.

INTERRUPTS

Interrupt requests can be generated internally by on-chip processes (INTB, INTT0, and INTS) or externally by peripheral devices (INT0 and INT1). There are two quasi-interrupts: INTK and INTW.
The following components support interrupt processing:

— Interrupt enable flags
— Interrupt request flags
— Interrupt priority registers
— Power-down release circuit

POWER-DOWN

To reduce power consumption, there are two power-down modes: Idle and Stop. The IDLE instruction initiates Idle mode; the STOP instruction initiates Stop mode.

In Idle mode, the CPU clock stops while peripherals continue to operate normally. In Stop mode, system clock oscillation stops completely, halting all operations except for a few basic peripheral functions. A power-down is released either by a RESETb or by an interrupt.

RESETb

When RESETb is input during normal operation or during power-down mode, a reset operation is initiated and the CPU enters Idle mode. When the standard oscillation stabilization time interval (31.3 ms at 4.19 MHz) has elapsed, normal CPU operation resumes.

I/O PORTS

The KS57C0002/0004 has two input ports and five I/O ports. There are total of 6 input pins and 18 configurable I/O pins, including 8-high current I/O pins. This gives a total number of 24 I/O pins.

TIMERS and TIMER/COUNTER

The timer function has three main components: an 8-bit basic timer, an 8-bit timer/counter, and a watch timer. The 8-bit basic timer generates interrupt requests at precise intervals, based on the selected internal clock frequency.

The 8-bit timer/counter is used for counting events, modifying internal clock frequencies, and dividing external clock signals. The 8-bit timer/counter generates a clock signal (SCKb) for the serial I/O interface. The watch timer consists of an 8-bit watch timer mode register, and a frequency divider circuit. Its functions include real-time and watch-time measurement, and clock generation for buzzer frequency output.

SERIAL I/O INTERFACE

The serial I/O interface supports the transmission or reception of 8-bit serial data with an external device. The serial interface has the following functional components:

— 8-bit mode register
— Clock selector circuit
— 8-bit buffer register
— 3-bit serial clock counter

BIT SEQUENTIAL CARRIER

The bit sequential carrier (BSC) is a 16-bit register that can be manipulated using 1-bit, 4-bit, and 8-bit instructions.

Using 1-bit indirect addressing, addresses and bit locations can be specified sequentially. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register. BSC data can also be manipulated using direct addressing.

COMPARATOR

The KS57C0002/0004 contains a 4-channel comparator that can be multiplexed to a normal I/O port. The comparison results are read from the 4-bit CMPREG register after the specified conversion time.

D.C. ELECTRICAL CHARACTERISTICS

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 4 and 5	$0.7V_{DD}$	—	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 3, 6, and RESETb	$0.8V_{DD}$	—	V_{DD}	
	V_{IH3}	X_{in} and X_{out}	V_{DD} – 0.5	—	V_{DD}	
Input Low Voltage	V_{IL1}	Ports 4 and 5	—	—	$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 2, 3, 6, and RESETb			$0.2V_{DD}$	
	V_{IL3}	X_{in} and X_{out}			0.2	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 1 mA Ports 0, 3, 4, 5, 6	V_{DD} – 1.0	—	—	V
		V_{DD} = 4.5 V to 6.0 V I_{OH} = – 3.0 mA Ports 0, 3, 4, 5, 6	V_{DD} – 2.0			
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 4 and 5 only	—	0.4	2	V
		V_{DD} = 4.5 V to 6.0 V I_{OL} = 1.6 mA Ports 0, 3, 6 only		—	0.4	
		V_{DD} = 4.5 V to 6.0 V I_{OL} = 4.0 mA Ports 0, 3, 6 only			2	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{in} and X_{out}	—	—	3	μA
	I_{LIH2}	V_{IN} = V_{DD} X_{in} and X_{out}			20	
	I_{LIH3}	V_{IN} = 9 V Ports 4 and 5 are open-drain			10	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{in}, X_{out} and RESETb	—	—	– 3	μA
	I_{LIL2}	V_{IN} = 0 V X_{in} and X_{out}			– 20	

D.C. ELECTRICAL CHARACTERISTICS (Continued)

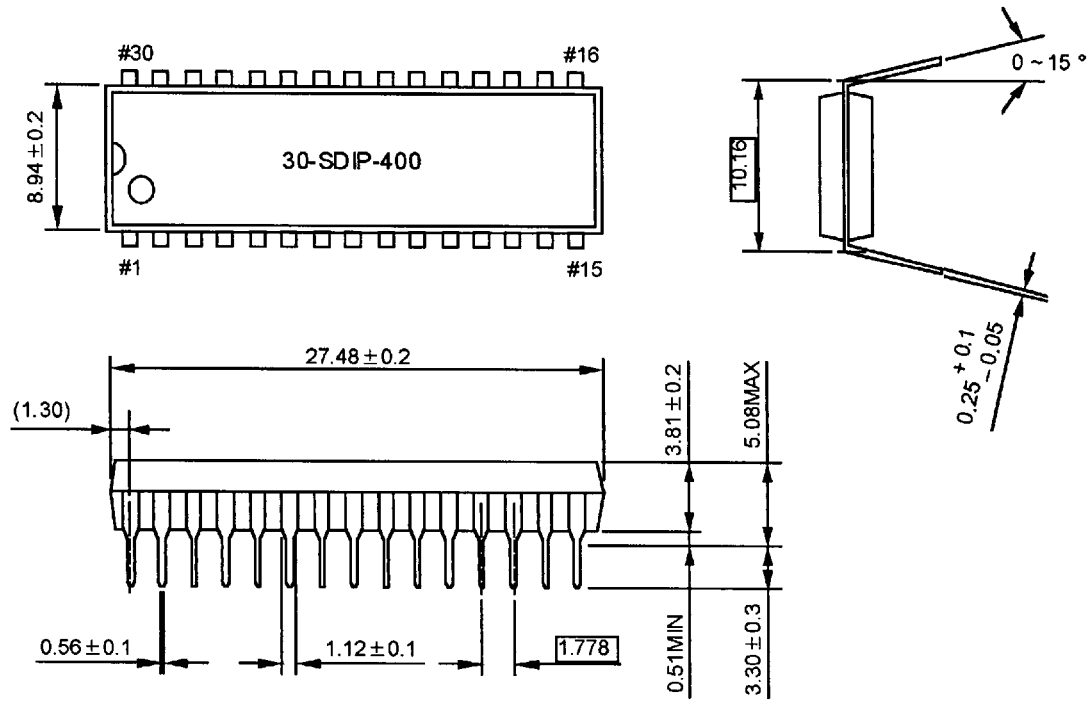
(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Leakage Current	I_{LOH1}	$V_O = V_{DD}$ All output pins except for port 4 and port 5	—	—	3	μA
	I_{LOH2}	V_O = 9 V Ports 4 and 5 are open-drain			10	
Output Low Leakage Current	I_{LOL}	V_O = 0 V	—	—	– 3	μA
Pull-Up Resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Port 0, 1, 3, 6	15	40	80	kΩ
		V_{IN} = 0 V; V_{DD} = 3 V ± 10% Port 0, 1, 3, 6	30		200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% RESETb	100	230	400	
		V_{IN} = 0 V; V_{DD} = 3 V ± 10% RESETb	200	490	800	
Supply Current (1)	I_{DD1}	V_{DD} = 5 V 귓10% (2) 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	2.5	8	mA
		V_{DD} = 3 V ± 10% (3) 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.62	1.2	
	I_{DD2}	Idle mode; V_{DD} = 5 V귓 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	1.2	1.8	mA
		Idle mode; V_{DD} = 3 V ± 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.58	1.0	
	I_{DD3}	Stop mode V_{DD} = 5 V ± 10%		0.5	5	μA
		Stop mode V_{DD} = 3 V ± 10%		0.3	3	

NOTES:

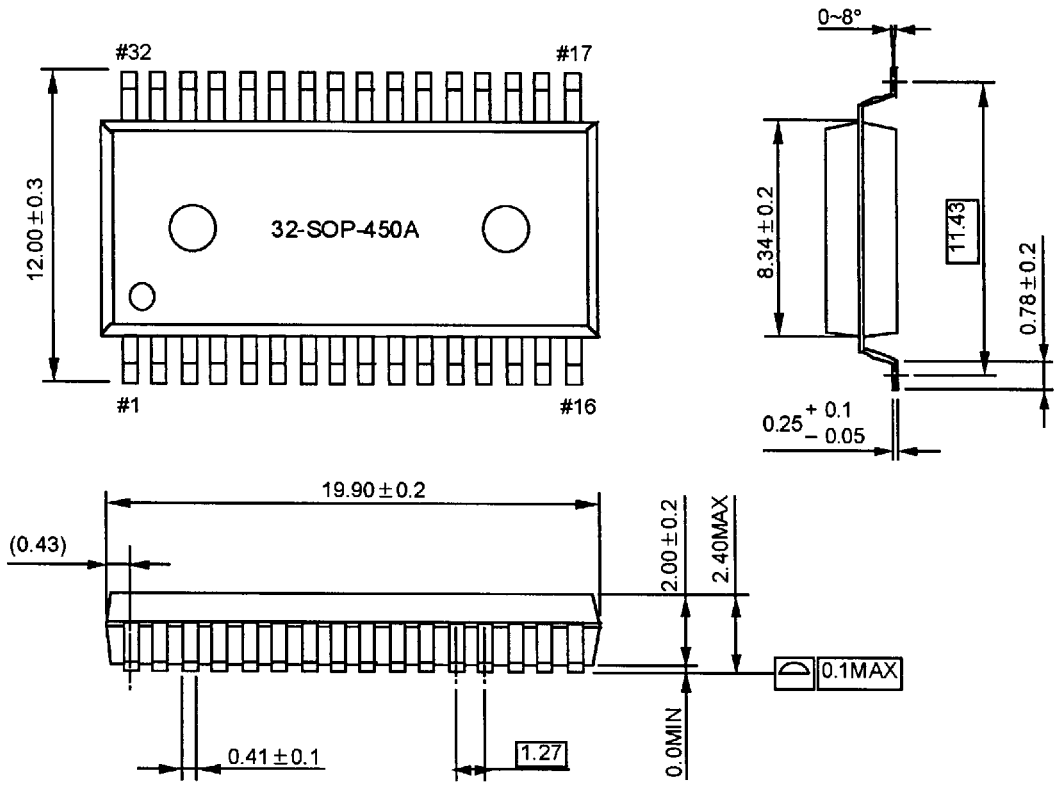
1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistors.
2. For high-speed controller operation, set the PCON register to 0011B.
3. For low-speed controller operation, set the PCON register to 0000B.

PACKAGE DIMENSIONS



NOTE: Dimensions are in millimeters.

PACKAGE DIMENSIONS (Continued)



NOTE: Dimensions are in millimeters.