KS57C2408A/2416A
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2408A/2416A single-chip CMOS microcontroller is designed for very high performance using Samsung's newest 4-bit product development approach, SAM4 (Samsung Arrangeable Microcontrollers). Its main features are an up-to-12-digit LCD direct drive capability, 8-bit × 6-channel A/D converter, and versatile 8-bit and 16-bit counter/ timers. The "2408A/2416A" gives you an excellent design solution for a variety of LCD-related applications.

Up to 50 pins of the available 80-pin QFP packages can be dedicated to I/O. And eight vectored interrupts provide fast response to internal and external events. In addition, the 2408A/2416A's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 8192 × 8-bit (KS57C2408A)
  16384 × 8-bit (KS57C2416A)
- Data memory mapped I/O

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (4, 8, 64)

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Interrupts

- 5 internal vectored interrupts
- 3 external vectored interrupts
- 2 quasi-interrupts

50 I/O Pins

- 10 input pins
- 12 output pins
- 20 configurable I/O pins
- 8 n-channel open-drain pins

8-Bit Basic Timer

- 4 interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider

Watch Timer

- Real-time and interval time measurement
- Clock generation for LCD
- Four frequency outputs for buzzer sound

LCD Controller/Driver

- Maximum 12-digit LCD direct drive capability
- Display modes: static, 1/2duty (1/2 bias)
- 1/3 duty (1/2 or1/3 bias), 1/4duty (1/3 bias)

A/D Converter

- Six analog input channels
- 19.09-μs conversion speed at 4.19 MHz
- 8-bit conversion resolution

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz (main)
- 122 μs at 32.768 kHz (subsystem)

Operating Temperature Range

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 80-pin QFP package

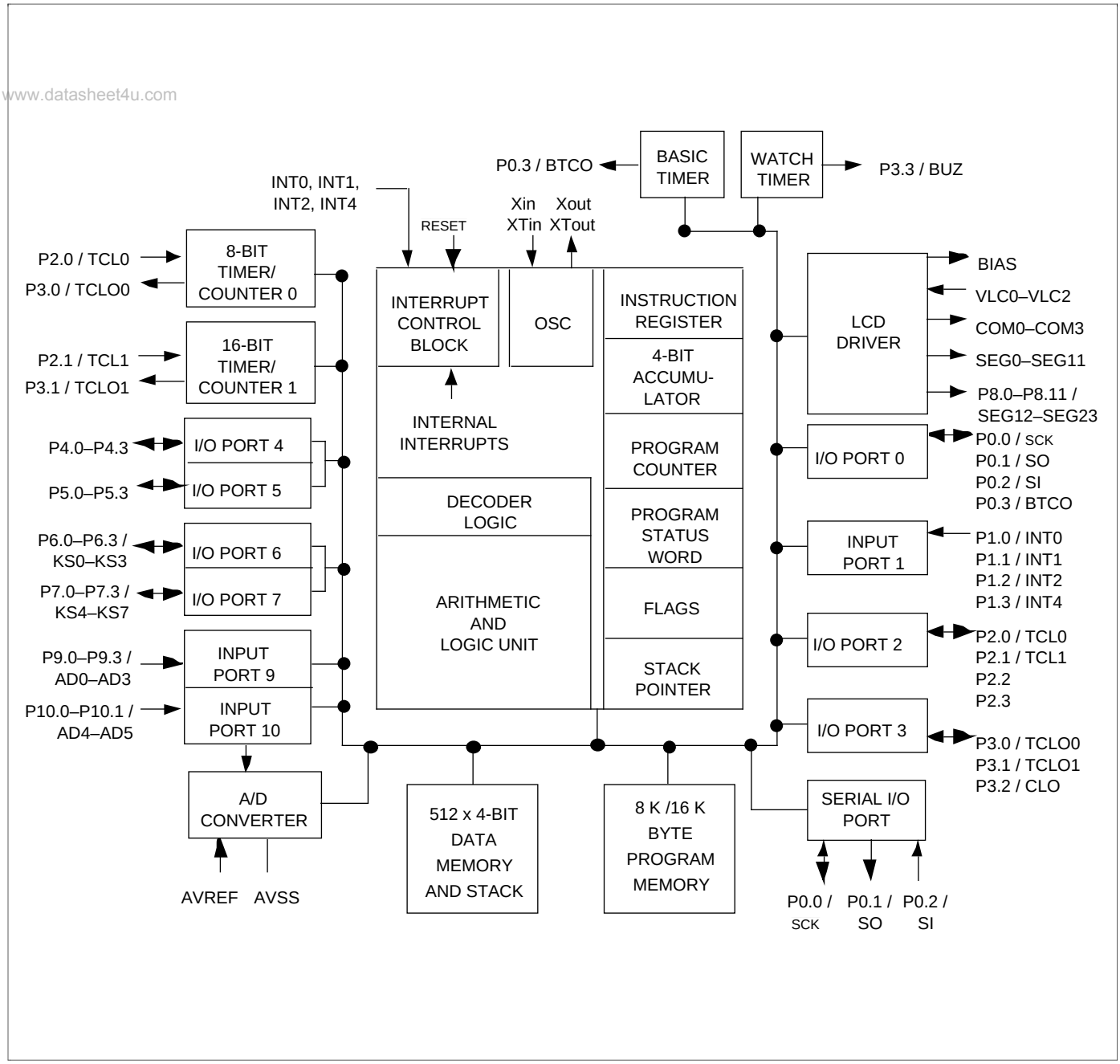


Figure 1. KS57C2408A/2416A Block Diagram

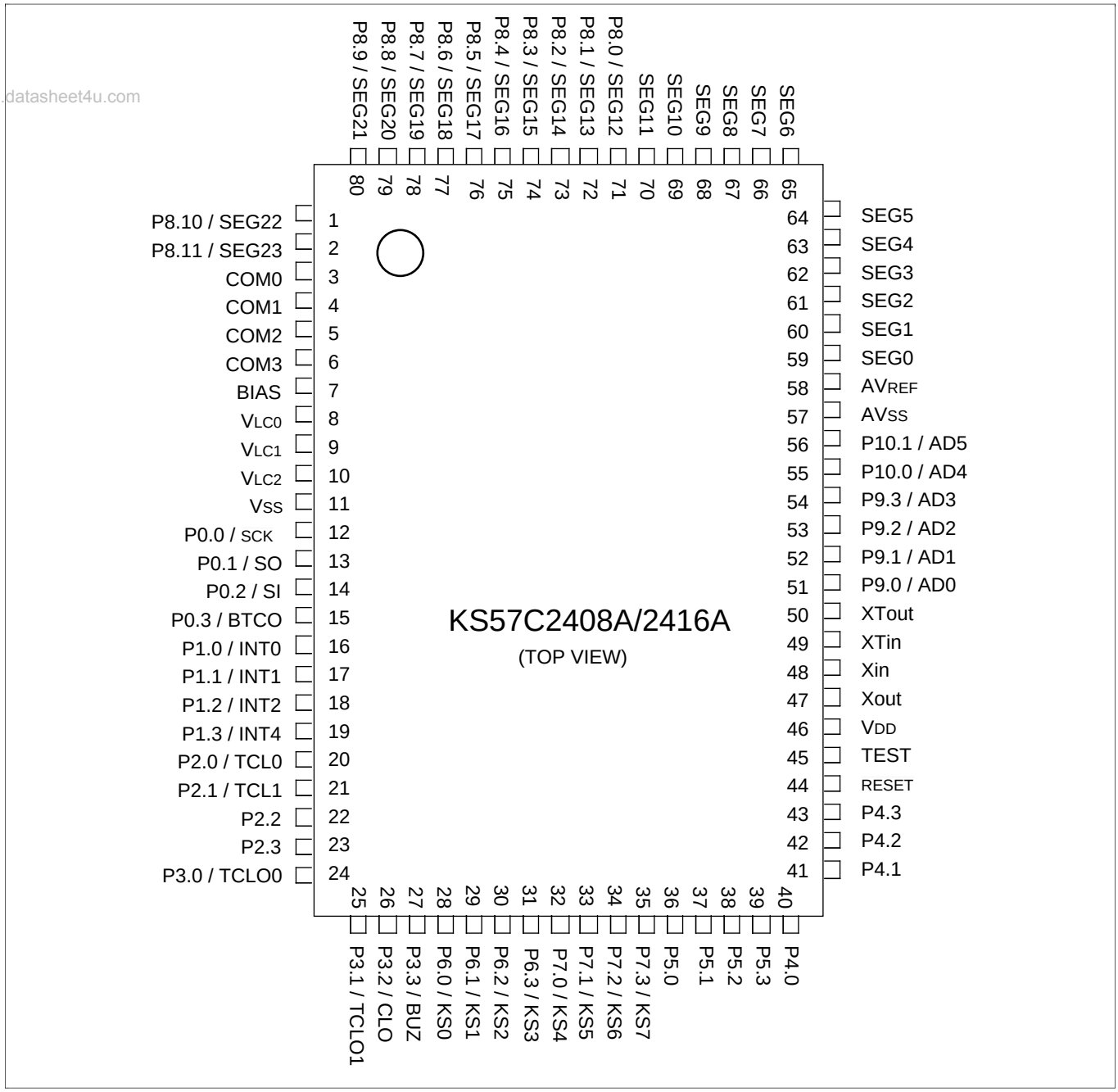


Figure 2. KS57C2408A/2416A Pin Assignments (80–QFP)

Table 1. KS57C2408A/2416A Pin Descriptions

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable.	12 13 14 15	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are software assignable to pins P1.0, P1.1, and P1.2.	16 17 18 19	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	20 21 22 23	TCL0 TCL1
P3.0 P3.1 P3.2 P3.3		Same as port 0.	24 25 26 27	TCLO0 TCLO1 CLO BUZ
P4.0–P4.3 P5.0–P5.3		4-bit I/O ports. N-channel open-drain output up to 9volts. 1 -, 4-, and 8-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	40–43 36–39	— —
P6.0–P6.3 P7.0–P7.3		4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	28–31 32–35	KS0–KS3 KS4–KS7
P8.0–P8.11	O	Output port for 1-bit data (for use as CMOS driver only).	71–80, 1–2	SEG12–SEG23
P9.0–P9.3 P10.0–P10.1	I	Input ports for 1-bit or 4-bit data. 1-bit and 4-bit read and test is possible.	51–56	AD0–AD3 AD4–AD5
CLO	I/O	CPU clock output	26	P3.2
BUZ		2, 4, 8, or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	27	P3.3
X_{in}, X_{out}	—	Crystal, ceramic, or RC oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out}.)	48, 47	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock. (For external clock input, use XT_{in} and input XT_{in}'s reverse phase to XT_{out}).	49, 50	—
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	16–17	P1.0, P1.1

Table 1. KS57C2408A/2416A Pin Descriptions (Continued)

Pin Names	Pin Type	Description	Number (80-QFP)	Share Pin
INT2	I	Quasi-interrupt with detection of rising edges	18	P1.2
INT4		External interrupt with detection of rising or falling edges	19	P1.3
KS0–KS7	I/O	Quasi-interrupt input with falling edge detection	28–35	P6.0–P7.3
TCL0		External clock input for timer/counter 0	20	P2.0
TCL1		External clock input for timer/counter 1	21	P2.1
TCLO0		Timer/counter 0 clock output	24	P3.0
TCLO1		Timer/counter 1 clock output	25	P3.1
COM0–COM3	O	LCD common signal output	3–6	—
SEG0–SEG11		LCD segment output	59–70	—
SEG12–SEG23		1-bit LCD segment data output	71–80, 1–2	P8.0–P8.11
BIAS	—	LCD power control	7	—
V_{LC0}–V_{LC2}		LCD power supply. Voltage dividing resistors are assignable by mask option.	8–10	—
AD0–AD5	I	A/D converter analog input channels	51–56	P9.0–P9.3 P10.0–P10.1
AV_{SS}	—	A/D converter ground	57	—
AV_{REF}		A/D converter analog reference voltage	58	—
SCK	I/O	Serial I/O interface clock signal	12	P0.0
SO		Serial data output	13	P0.1
SI		Serial data input	14	P0.2
BTCO		Basic interval timer clock output	15	P0.3
RESET	I	Reset signal	44	—
V_{DD}	—	Main power supply	46	—
V_{SS}		Ground	11	—
TEST		Test signal input (must be connected to $V_{SS)}$	45	—

NOTE: Pull-up resistors for ports 0, 2, 3, 6, and 7 are automatically disabled if they are configured to output mode.

Table 2. Supplemental KS57C2408A/2416A Pin Data

Pin Numbers (80-QFP)	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1, 2	P8.10, P8.11	SEG22–SEG23	O	Low	9
3–6	COM0–COM3	—	O	Low	8
7	BIAS	—	—	—	—
8–10	V_{LC0}–V_{LC2}	—	—	—	—
11	V_{SS}	—	—	—	—
12–15	P0.0–P0.3	SCK , SO, SI, BTCO	I/O	Input	6
16–18	P1.0–P1.2	INT0, INT1, INT2	I		3
19	P1.3	INT4	I		2
20, 21	P2.0, P2.1	TCL0, TCL1	I/O		6
22, 23	P2.2, P2.3	—			6
24–27	P3.0–P3.3	TCLO0, TCLO1, CLO, BUZ			5
28–31	P6.0–P6.3	KS0–KS3			6
32–35	P7.0–P7.3	KS4–KS7			6
36–39	P5.0–P5.3	—	I/O	(Note)	10
40–43	P4.0–P4.3	—	I/O	(Note)	10
44	RESET	—	—	—	12
45	TEST	—	—	—	—
46	V_{DD}	—	—	—	—
47, 48	X_{in}, X_{out}	—	—	—	—
49, 50	XT_{in}, XT_{out}	—	—	—	—
51–54	P9.0–P9.3	AD0–AD3	I	Input	11
55, 56	P10.0, P10.1	AD4, AD5	I	Input	11
57, 58	AV_{SS}, AV_{REF}	—	—	—	—
59–70	SEG0–SEG11	—	O	Low	7
71–80	P8.0–P8.9	SEG12–SEG21	O	Low	9

NOTE: High level (when pull-up resistors are provided) or high impedance.

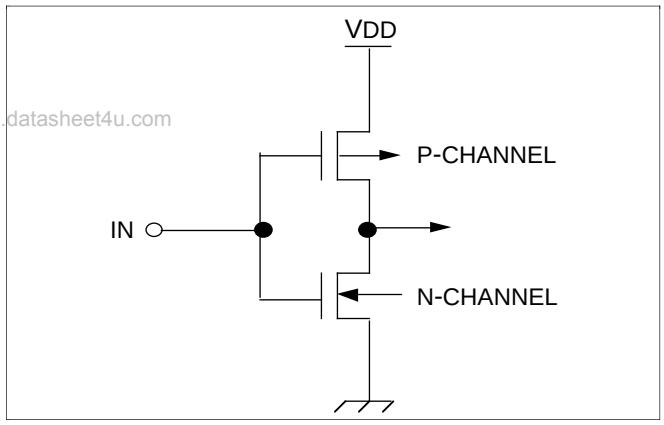


Figure 3. Pin Circuit Type 1

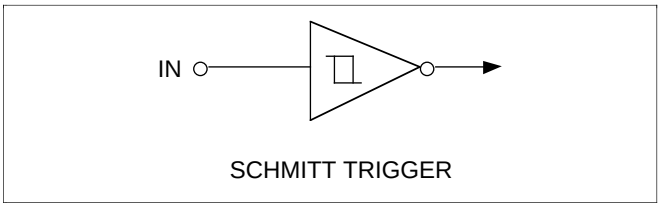


Figure 4. Pin Circuit Type 2

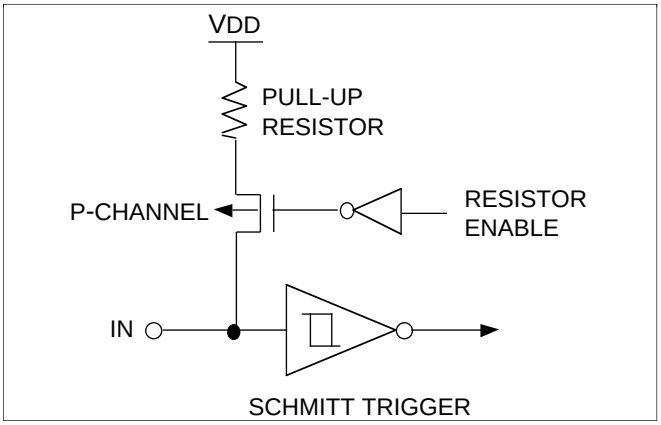


Figure 5. Pin Circuit Type 3

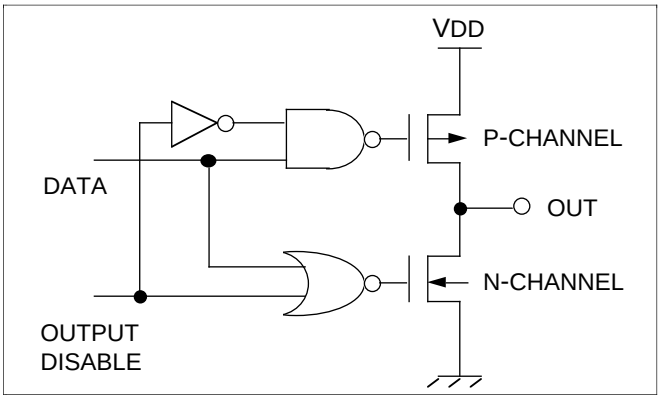


Figure 6. Pin Circuit Type 4

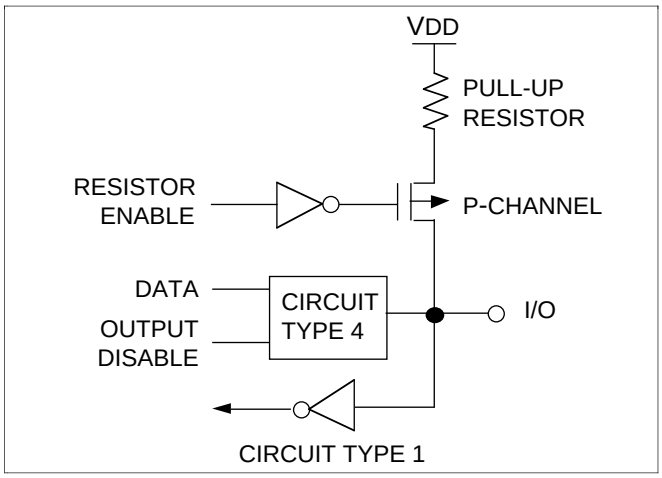


Figure 7. Pin Circuit Type 5

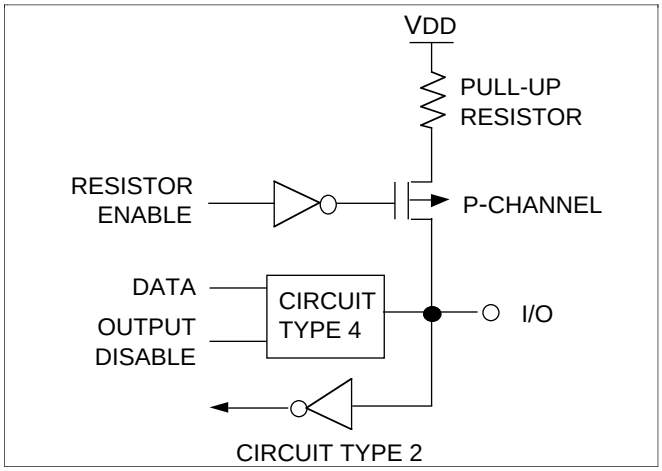


Figure 8. Pin Circuit Type 6

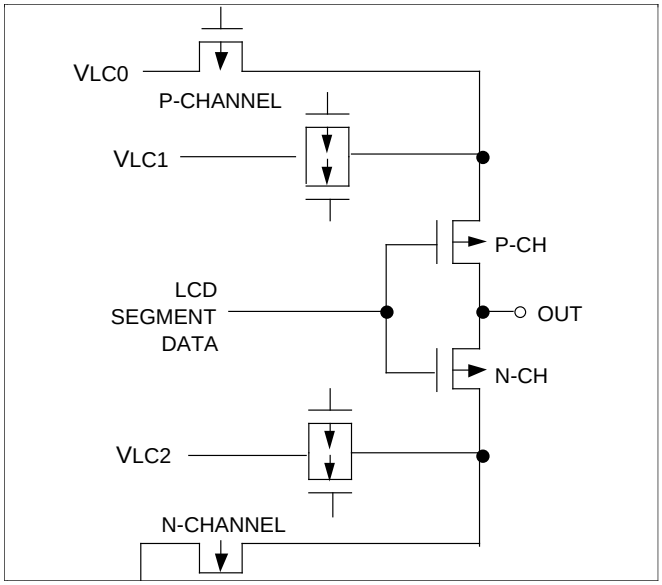


Figure 9. Pin Circuit Type 7

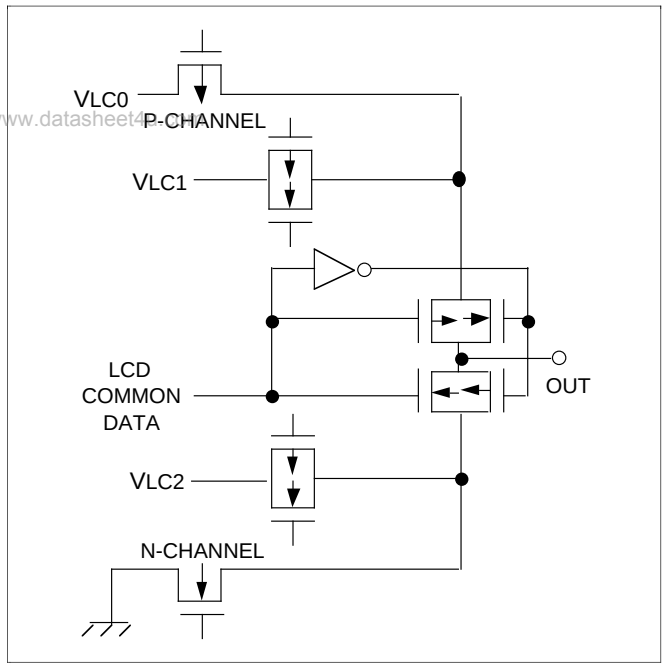


Figure 10. Pin Circuit Type 8

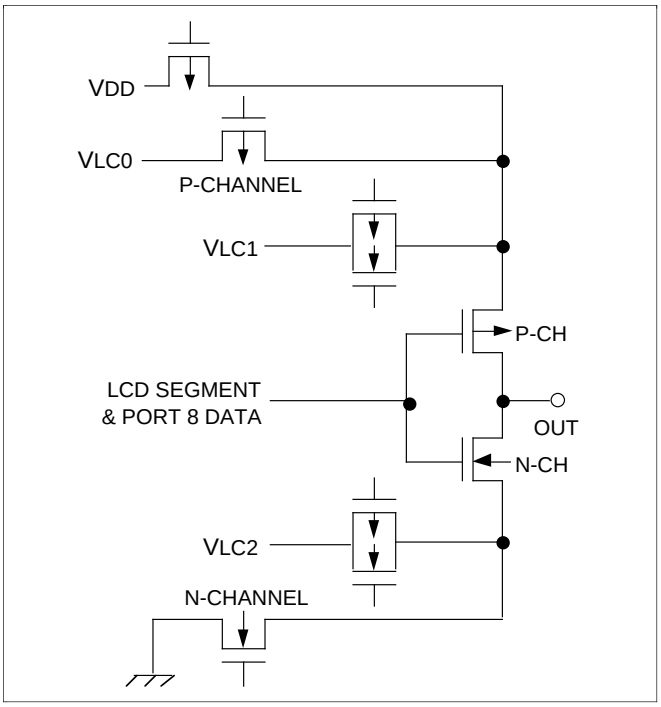


Figure 11. Pin Circuit Type 9

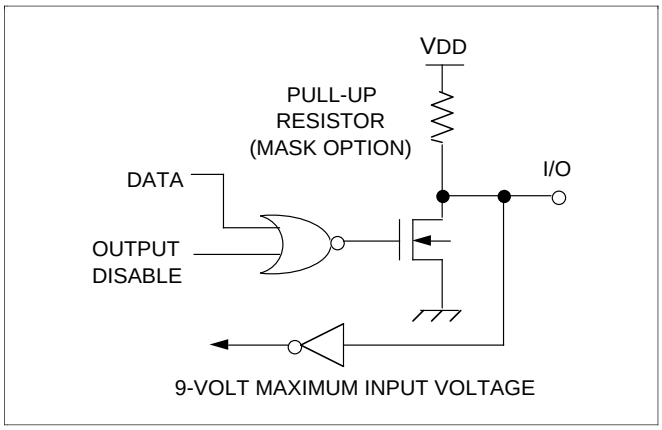


Figure 12. Pin Circuit Type 10

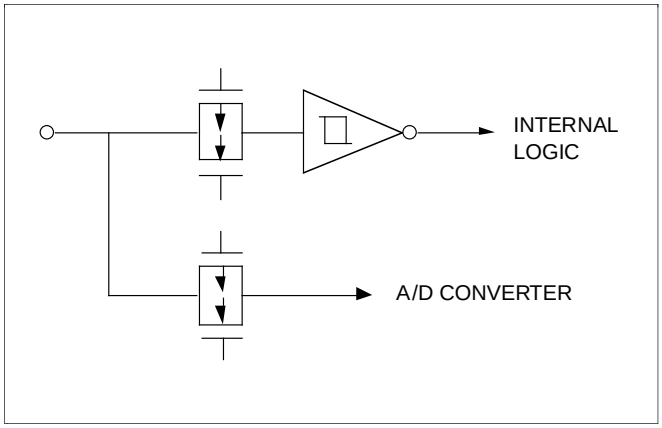


Figure 13. Pin Circuit Type 11

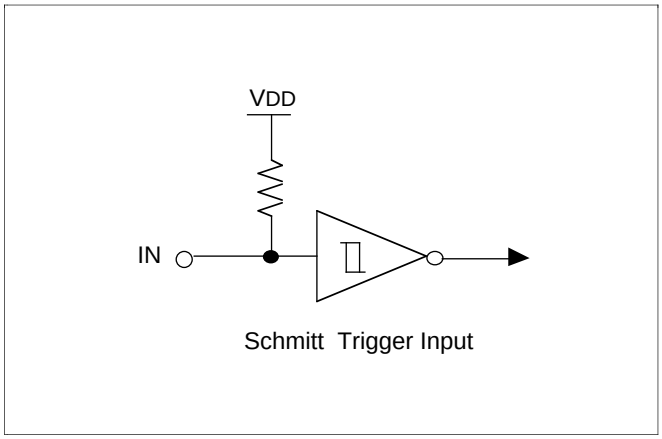


Figure 14. Pin Circuit Type 12

PROGRAM MEMORY (ROM)

ROM maps for KS57 devices are mask programmable at the factory. In its standard configuration, the device's 8192 × 8-bit / 16384 × 8-bit program memory has four areas that are directly addressable by the program counter (PC):

- 16-byte general-purpose area
- 8064 / 16256-bytegeneral-purpose area
- 16-byte area for vector addresses
- 96-byte instruction reference area

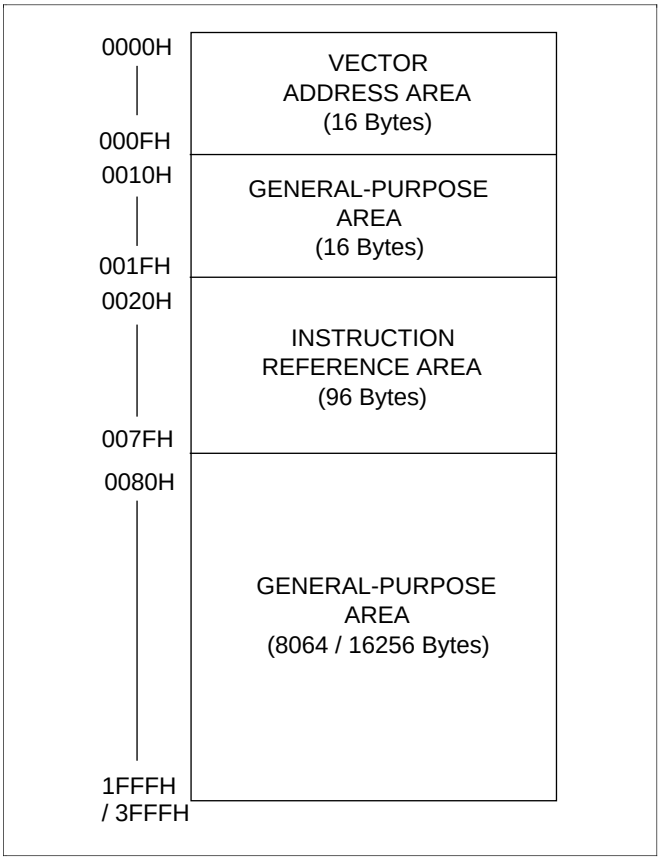


Figure 15. ROM Map

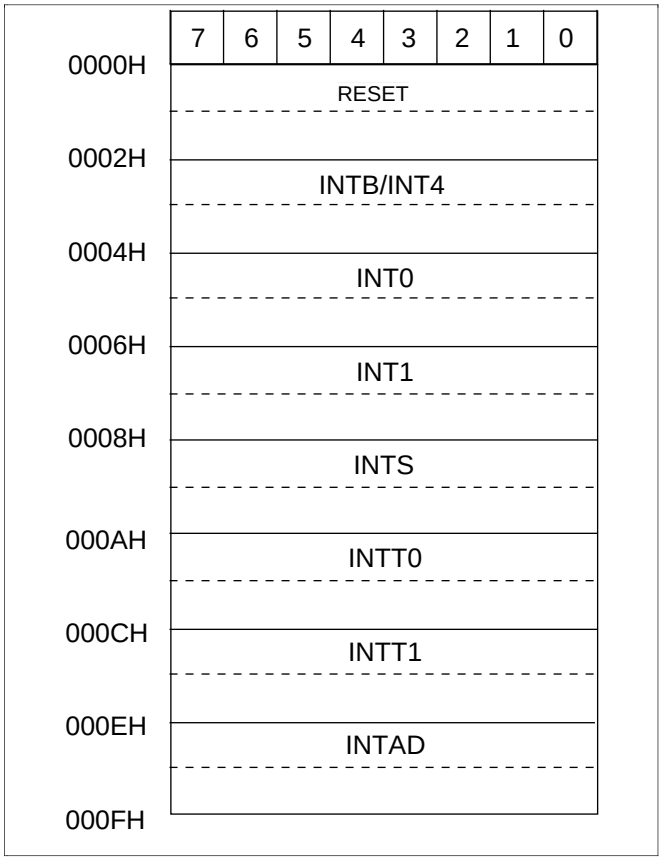


Figure 16. Vector Address Map

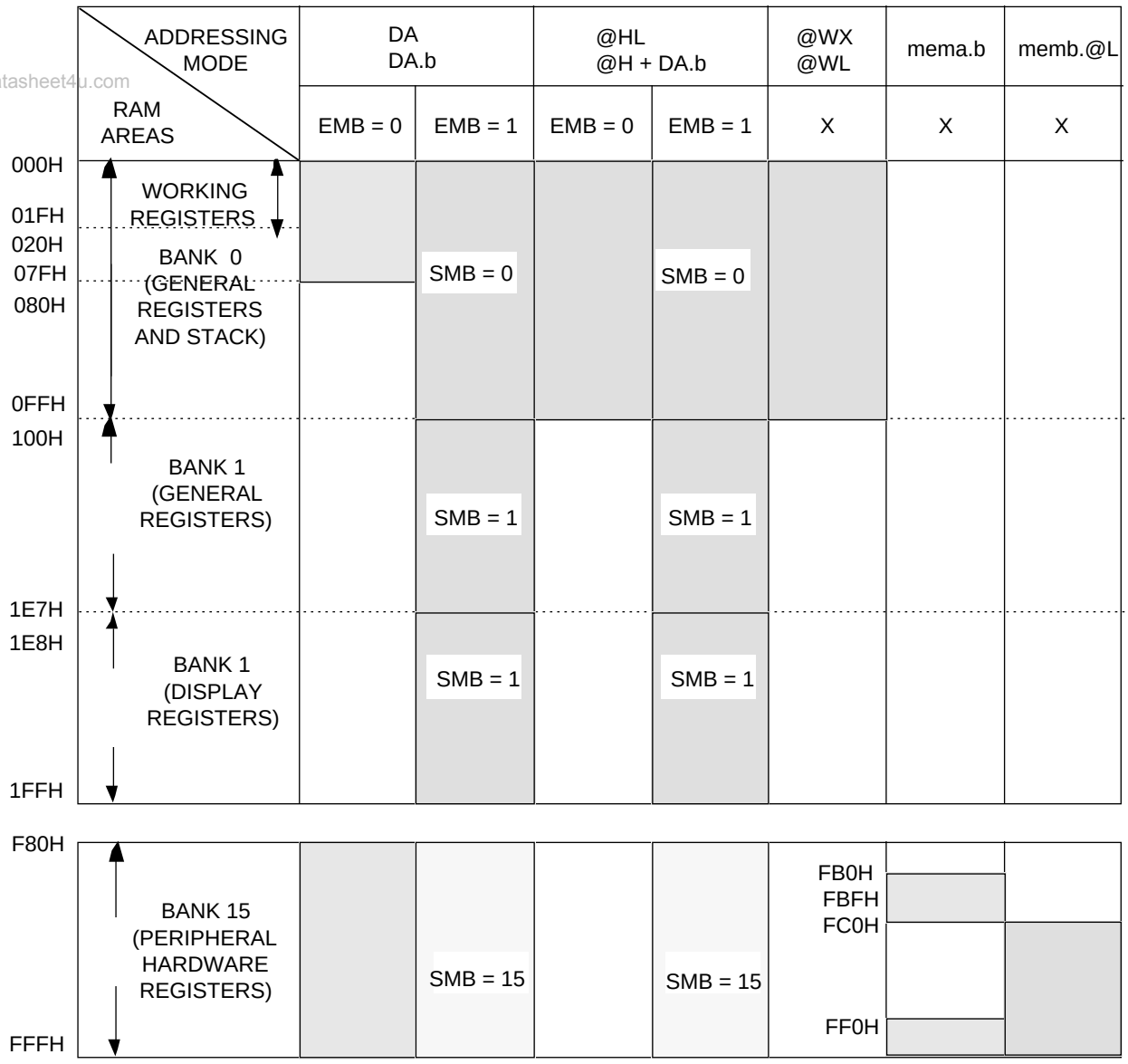
DATA MEMORY (RAM)

In its standard configuration, the 512× 4 -bit data memory has five areas:

- 32 ×4-bit working register area
- 224× 4 -bit general-purpose area (also used as stack area)
- 232× 4 -bit general-purpose area
- 24 ×4-bit area for LCD data
- 128× 4-bit area for memory-mapped I/O addresses

I/O MAP FOR HARDWARE REGISTERS

Table 3 contains detailed information about I/O mapping for peripheral hardware in bank 15 (register locations F80H–FFFH).



NOTES: 1. 'X' means don't care.
2. Blank columns indicate RAM areas that are not addressable, given the addressing method and enable memory bank (EMB) flag setting shown in the column headers.

Figure 17. Data Memory (RAM) Address Structure

Table 3. I/O Map for Memory Bank 15

Memory Bank 15						Addressing Mode			
Address	Register	Name				R/W	1-Bit	4-Bit	8-Bit
F81H–F80H	SP	Stack Pointer				R/W	No	No	Yes
F85H	BMOD	Basic Timer Mode Register				W	.3	Yes	No
F87H–F86H	BCNT	Basic Timer Counter Register				R	No	No	Yes
F89H–F88H	WMOD	Watch Timer Mode Register				W	.3 (R)	No	Yes
F8DH–F8CH	LMOD	LCD Mode Register				W	.3 (W)	No	Yes
F8EH	LCON	LCD Control Register				W	No	Yes	No
F91H–F90H	TMOD0	Timer/Counter 0 Mode Register				W	.3 (W)	No	Yes
F92H		TOE1	TOE0	BOE	"0"	R/W	Yes	Yes	No
F95H–F94H	TCNT0	Timer/Counter 0 Counter Register				R	No	No	Yes
F97H–F96H	TREF0	Timer/Counter 0 Reference Reg				W	No	No	Yes
FA1H–FA0H	TMOD1	Timer/Counter 1 Mode Register				W	.3 (W)	No	Yes
FA5H–FA4H	TCNT1 A	Timer/Counter 1 Counter Register A				R	No	No	Yes
FA7H–FA6H	TCNT1 B	Timer/Counter 1 Counter Register B				R	No	No	Yes
FA9H–FA8H	TREF1 A	Timer/Counter 1 Reference Reg A				W	No	No	Yes
FABH–FAAH	TREF1 B	Timer/Counter 1 Reference Reg B				W	No	No	Yes
FB0H	PSW	IS1	IS0	EMB	ERB	R/W	Yes	Yes	Yes
FB1H		C (1)	SC2	SC1	SC0	R	No	No	
FB2H	IPR	Interrupt Priority Register				W	IME	Yes	No
FB3H	PCON	Power Control Register				W	No	Yes	No
FB4H	IMOD0	External Interrupt 0 Mode Register				W	No	Yes	No
FB5H	IMOD1	External Interrupt 1 Mode Register							
FB6H	IMOD2	External Interrupt 2 Mode Register							
FB7H	SCMOD	System Clock Mode Register				W	Yes	No	No
FB8H		IE4	IRQ4	IEB	IRQB	R/W	Yes	Yes	No
FBAH		"0"	"0"	IEW	IRQW				
FBBH		IEAD	IRQAD	IET1	IRQT1				
FBCH		"0"	"0"	IET0	IRQT0				
FBDH		"0"	"0"	IES	IRQS				
FBEH		IE1	IRQ1	IE0	IRQ0				
FBFH		"0"	"0"	IE2	IRQ2				
FC0H	BSC0	Bit Sequential Carrier 0				R/W	Yes	Yes	Yes
FC1H	BSC1	Bit Sequential Carrier 1							
FC2H	BSC2	Bit Sequential Carrier 2							Yes

Table 3. I/O Map for Memory Bank 15 (Continued)

Memory Bank 15			Addressing Mode			
Address	**Register**	**Name**	**R/W**	**1-Bit**	**4-Bit**	**8-Bit**
FC3H	BSC3	Bit Sequential Carrier 3	R/W	Yes	Yes	Yes
FD0H	CLMOD	Clock Mode Register	W	No	Yes	No
FD9H–FD8H	ADATA	ADC Data Register	R	No	No	Yes
FDAH	ADMOD	ADC Mode Register	R/W	Yes	Yes	No
FDBH	AFLAG	ADC Flag Register	(2)	Yes	Yes	No
FDDH–FDCH	PUMOD	Pull-up Mode Register	W	No	No	Yes
FE1H–FE0H	SMOD	SIO Mode Register	W	.3	No	Yes
FE5H–FE4H	SBUF	SIO Buffer Register	R/W	No	No	Yes
FE9H–FE8H	PMG1	Port Mode Group 1	W	No	No	Yes
FEBH–FEAH	PMG2	Port Mode Group 2				
FEDH–FECH	PMG3	Port Mode Group 3				
FF0H	P0	Port 0	R/W	Yes	Yes	No
FF1H	P1	Port 1	R	Yes	Yes	No
FF2H	P2	Port 2	R/W	Yes	Yes	No
FF3H	P3	Port 3	R/W	Yes	Yes	No
FF4H	P4	Port 4	R/W	Yes	Yes	Yes
FF5H	P5	Port 5	R/W	Yes	Yes	
FF6H	P6	Port 6	R/W	Yes	Yes	Yes
FF7H	P7	Port 7	R/W	Yes	Yes	
FF8H	P9	Port 9	R	Yes	Yes	No
FF9H	P10	Port 10	R	Yes	Yes	

NOTES:5
1. The carry flag can be read or written by specific bit manipulation instructions only.
2. The ADSTR bit of the AFLAG register is 1- bit or 4-bit write-only; the EOC bit is 1-bit or 4-bit read-only.

BIT SEQUENTIAL CARRIER (BSC)

The bit sequential carrier (BSC) is a 16-bit general register that is mapped in data memory bank 15. Using the BSC, you can specify sequential addresses and bit locations using 1-bit indirect addressing (memb.@L).

BSC bit addressing is independent of the current EMB value. In this way, programs can process 16-bit data by moving the bit location sequentially and then incrementing or decrementing the value of the L register.

For 8-bit manipulations, the 4-bit register names BSC0 and BSC2 must be specified and the upper and lower 8 bits manipulated separately. If the values of the L register are 0H at BSC0.@L, the address and bit location assignment is FC0H.0. If the L register content is FH at BSC0.@L, the address and bit location assignment is FC3H.3.

Table 4. BSC Register Organization

Name	Address	Bit 3	Bit 2	Bit 1	Bit 0
BSC0	FC0H	BSC0.3	BSC0.2	BSC0.1	BSC0.0
BSC1	FC1H	BSC1.3	BSC1.2	BSC1.1	BSC1.0
BSC2	FC2H	BSC2.3	BSC2.2	BSC2.1	BSC2.0
BSC3	FC3H	BSC3.3	BSC3.2	BSC3.1	BSC3.0

☞ **PROGRAMMING TIP — Using the BSC Register to Output 16-Bit Data**

To use the bit sequential carrier (BSC) register to output 16-bit data (5937H) to the P3.0 pin:

```
        BITS    EMB
        SMB     15
        LD      EA,#37H         ;
        LD      BSC0,EA         ;   BSC0 ← A, BSC1 ← E
        LD      EA,#59H         ;
        LD      BSC2,EA         ;   BSC2 ← A, BSC3 ← E
        SMB     0
        LD      L,#0H           ;
AGN LDB     C,BSC0.@L           ;
        LDB     P3.0,C          ;   P3.0 ← C
        INCS    L
        JR      AGN
        RET
```

INTERRUPTS

The KS57C2408A/2416A has three external interrupts, five internal interrupts and two quasi-interrupts. Table 5 shows the conditions for interrupt generation. The request flags that allow these interrupts to be generated are cleared by hardware when the service routine is vectored. The quasi-interrupt's request flags must be cleared by software.

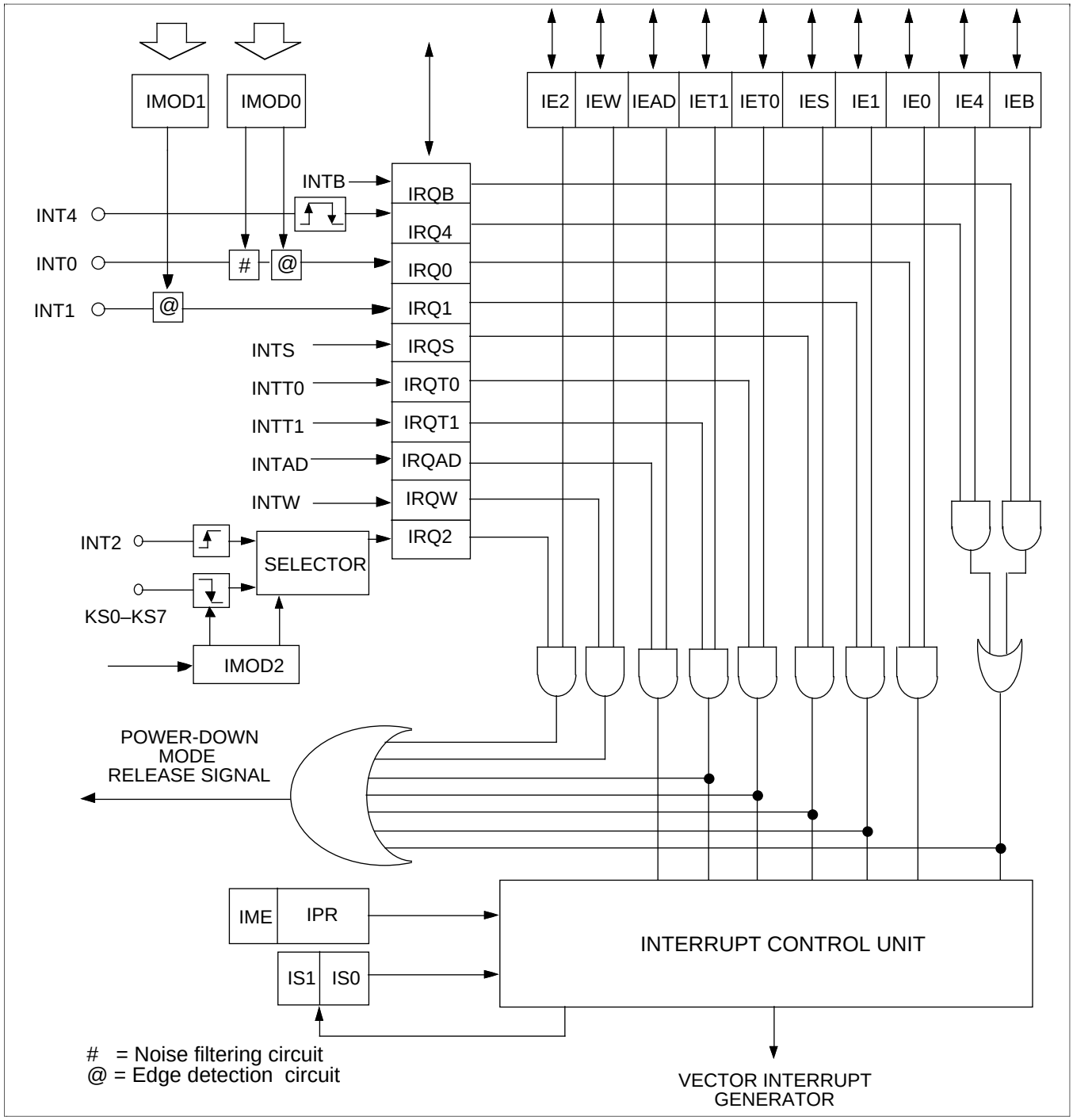


Figure 18. Interrupt Control Circuit Diagram

Table 5. Interrupt Request Flag Conditions and Priorities

Interrupt Source	Internal / External	Condition for IRQx Flag Setting	Interrupt Priority	Request Flag Name
INTB	I	Reference time interval signal from basic timer	1	IRQB
INT4	E	Both rising and falling edges detected at INT4	1	IRQ4
INT0	E	Rising or falling edge detected at INT0 pin	2	IRQ0
INT1	E	Rising or falling edge detected at INT1 pin	3	IRQ1
INTS	I	Completion signal for serial transmit-and-receive or receive-only operation	4	IRQS
INTT0	I	Signals for TCNT0 and TREF0 registers match	5	IRQT0
INTT1	I	Signals for TCNT1 and TREF1 registers match	6	IRQT1
INTAD	I	Analog-to-digital conversion is completed	7	IRQAD
INT2 *	E	Rising edge detected at INT2 or else a falling edge is detected at any of the KS0–KS7 pins	–	IRQ2
INTW	I	Time interval of 0.5 s or 3.19 ms	–	IRQW

* The quasi-interrupt INT2 is only used for testing incoming signals.

INTERRUPT ENABLE FLAGS

IEx flags, when set to "1", enable specific interrupt requests to be serviced. When the interrupt request flag is set to "1", an interrupt will not be serviced until its corresponding IEx flag is also enabled. The IPR register contains a global disable bit, IME, which disables all interrupt at once.

Table 6. Interrupt Enable and Request Flags

Address	Bit 3	Bit 2	Bit 1	Bit 0
FB8H	IE4	IRQ4	IEB	IRQB
FBAH	0	0	IEW	IRQW
FBBH	IEAD	IRQAD	IET1	IRQT1
FBCH	0	0	IET0	IRQT0
FBDH	0	0	IES	IRQS
FBEH	IE1	IRQ1	IE0	IRQ0
FBFH	0	0	IE2	IRQ2

NOTES:
1. IEx refers to all interrupt enable flags.
2. IRQx refers to all interrupt request flags.
3. IEx = "0" is interrupt disable mode.
4. IEx = "1" is interrupt enable mode.

INTERRUPT PRIORITY

Each interrupt source can also be individually programmed to high levels by modifying the IPR register. When IS1 = 0 and IS0 = 1, a low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt.

If you clear the interrupt status flags (IS1 and IS0) to "0" in a interrupt service routine, a high-priority interrupt can be interrupted by low-priority interrupt (multi-level interrupt). Before the IPR can be modified by 4-bit write instructions, all interrupts must first be disabled by a DI instruction.

When all interrupts are low priority (the lower three bits of the IPR register are "0"), the interrupt requested first will have high priority. Therefore, the first-requested interrupt cannot be superseded by any other interrupt.

If two or more interrupt requests are received simultaneously, the priority level is determined according to the standard interrupt priorities, where the default priority is assigned by hardware when the lower three IPR bits = "0".

In this case, the higher-priority interrupt request is serviced and the other interrupt is inhibited. Then, when the high-priority interrupt is returned from its service routine by an IRET instruction, the inhibited service routine is started.

Table 7. Interrupt Priority Register Settings

IPR.2	IPR.1	IPR.0	Result of IPR Bit Setting
0	0	0	Process all interrupt requests at low priority
0	0	1	INTB and INT4
0	1	0	INT0
0	1	1	INT1
1	0	0	INTS
1	0	1	INTT0
1	1	0	INTT1
1	1	1	INTAD

Table 8. Default Priorities

Source	Default Priority
INTB, INT4	1
INT0	2
INT1	3
INTS	4
INTT0	5
INTT1	6
INTAD	7

☞ PROGRAMMING TIP — Setting the INT Interrupt Priority

Set the INT1 interrupt to high priority:

```
BITS    EMB
SMB     15
DI              ;   IPR.3 (IME) ← 0
LD      A,#3H
LD      IPR,A
EI              ;   IPR.3 (IME) ← 1
```

EXTERNAL INTERRUPTS

The external interrupt 0 and 1 mode registers (IMOD0 and IMOD1) are used to control the triggering edge of the input signal at the INT0 and INT1 pins.

When a sampling clock rate of fxx/64 is used for INT0, an interrupt request flag must be cleared before 16 machine cycles have elapsed. Since the INT0 pin has a clock-driven noise filtering circuit built into it, please take the following precautions when you use it:

— To trigger an interrupt, the input signal width at INT0 must be at least two times wider than the pulse width of the clock selected by IMOD0. This is true even when the INT0 pin is used for general-purpose input.

— Since the INT0 input sampling clock does not operate during Stop or Idle mode, you cannot use INT0 to release power-down mode.

EXTERNAL INTERRUPTS (Continued)

When modifying the IMOD0 and IMOD1 registers, it is possible to accidentally set an interrupt request flag. To avoid unwanted interrupts, take these precautions when writing your programs:

1. Disable all interrupts with a DI instruction.
2. Modify the IMOD0 or IMOD1 register.
3. Clear all relevant interrupt request flags.
4. Enable the interrupt by setting the appropriate IEx flag.
5. Enable all interrupts with an EI instruction.

The external interrupt 2 (INT2) mode register (IMOD2) is used to select INT2 and KS pins as interrupt input. If a rising edge is detected at the INT2 pin, or when a falling edge is detected at any one of the KS0–KS7 pins, the IRQ2 flag is set to "1". This generates an interrupt request and a release signal for power-down mode.

To generate a key interrupt on a falling edge at KS0-KS7, all KS0-KS7 pins must be configured to input mode. KS4-KS7, in particular, must always be set to input mode.

If one or more of the pins which are configured as key Interrupt (KS0–KS7) are in Low input or Low output state, the key Interrupt can not be occured.

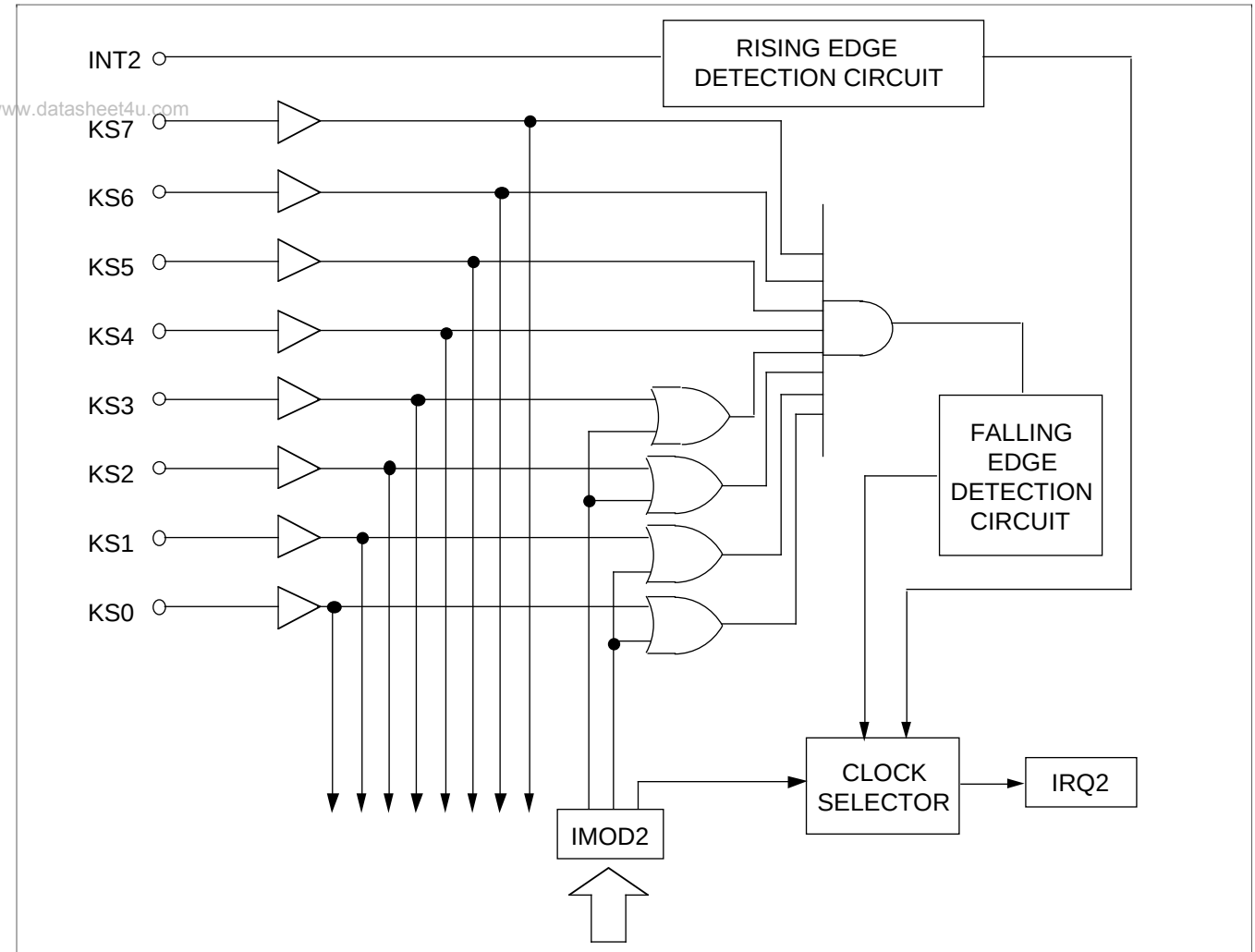
Table 9. IMOD0 and IMOD1 Register Organization (4-Bit W)

IMOD0.3	0	IMOD0.1	IMOD0.0	Effect of IMOD0 Settings
0				Select CPU clock for sampling
1				Select fxx/64 sampling clock
	0	0	0	Rising edge detection
	0	0	1	Falling edge detection
	0	1	0	Both rising and falling edge detection
	0	1	1	IRQ0 flag cannot be set to "1"

0	0	0	IMOD1.0	Effect of IMOD1 Settings
0	0	0	0	Rising edge detection
0	0	0	1	Falling edge detection

Table 10. IMOD2 Register Bit Settings (4-Bit W)

0	0	IMOD2.1	IMOD2.0	Effect of IMOD2 Settings
0	0	0	0	Select rising edge at INT2 pin
0	0	0	1	Select falling edge at KS4–KS7
0	0	1	0	Select falling edge at KS2–KS7
0	0	1	1	Select falling edge at KS0–KS7



NOTE: To generate a key interrupt on a falling edge at KS0–KS7, all KS0–KS7 pins must be configured to input mode. KS4–KS7, in particular, must always be configured to input mode.

Figure 18-1. Circuit diagram for INT2 and KS0-KS7

OSCILLATOR CIRCUITS

The KS57C2408A/2416A microcontroller has two oscillator circuits: a main system clock circuit, and a subsystem clock circuit. The main system clock frequencies can be divided by 4, 8, or 64 by manipulating PCON bits 1 and 0.

The system clock mode control register, SCMOD, lets you select the main system clock (fx) or a subsystem clock (fxt) as the CPU clock and to start (or stop) main system clock oscillation.

The watch timer, buzzer and LCD display operate normally with a subsystem clock source, since they operate at very slow speeds and with very low power consumption (as low as 122 µs at 32.768 kHz).

NOTE

If a subsystem clock (fxt) is selected as the system clock, the microcontroller's analog-to-digital converter block does not operate.

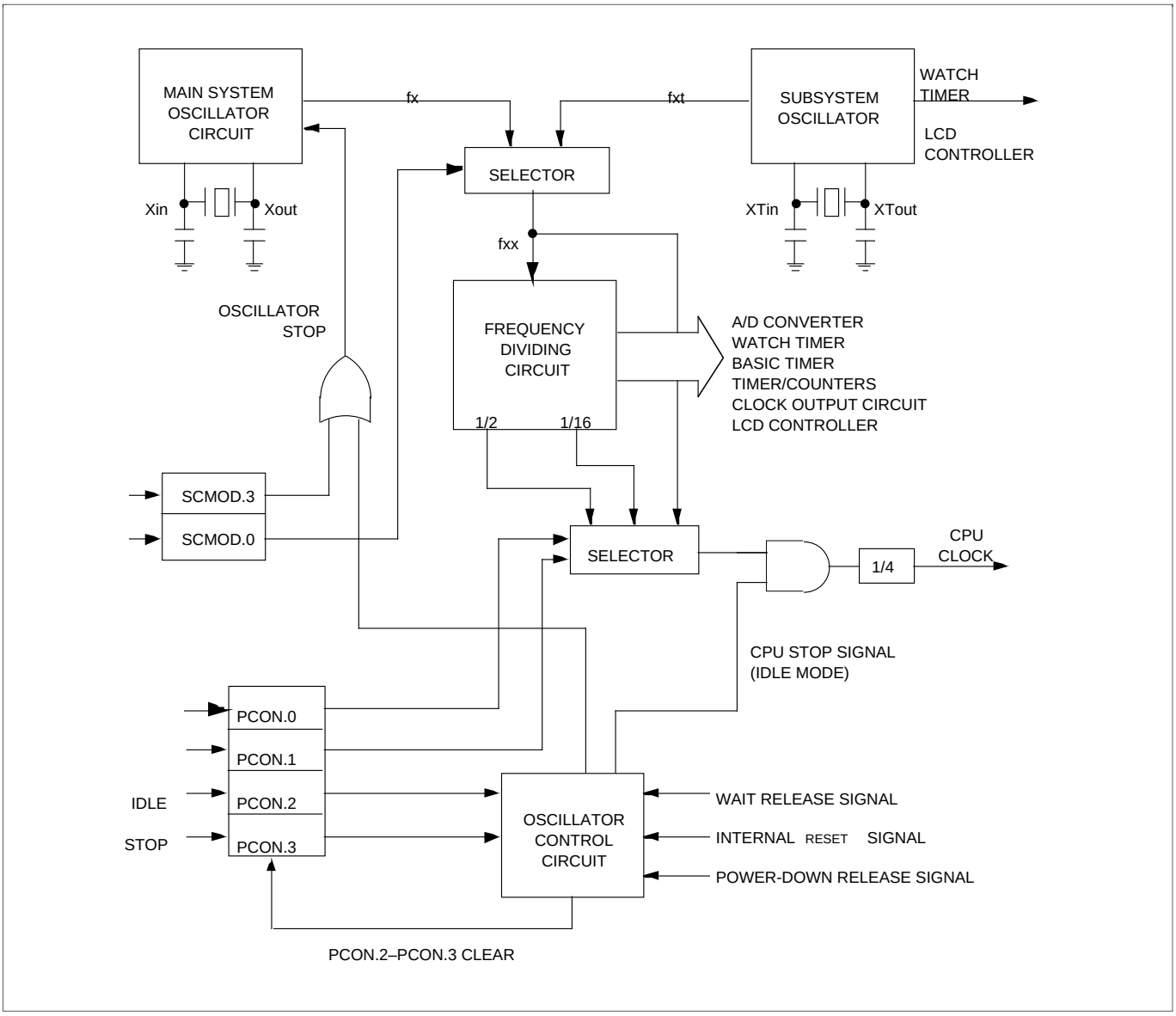


Figure 19. Oscillator Circuit Diagram

MAIN SYSTEM OSCILLATOR CIRCUITS

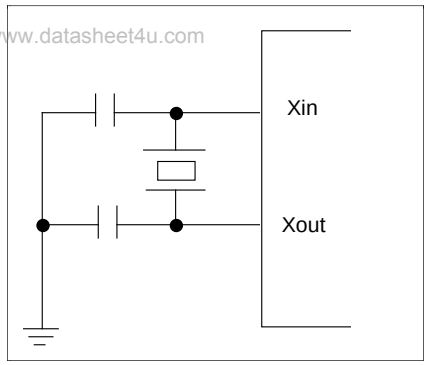


Figure 20. Crystal/Ceramic Oscillator (fx)

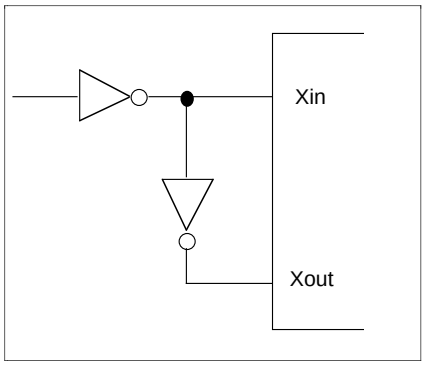


Figure 21. External Oscillator (fx)

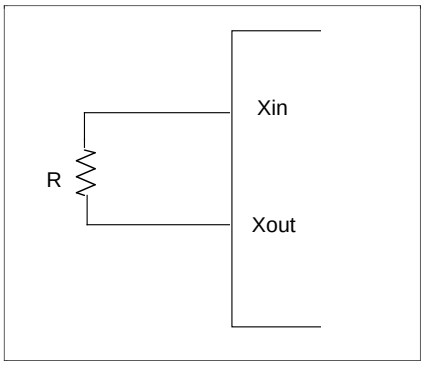


Figure 22. RC Oscillator (fx)

SUBSYSTEM OSCILLATOR CIRCUITS

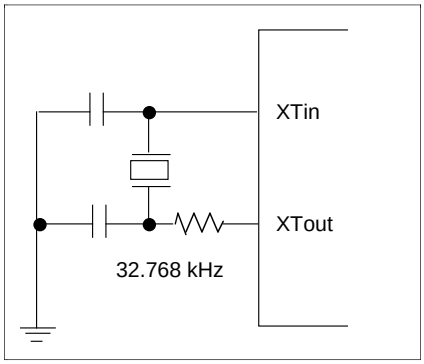


Figure 23. Crystal/Ceramic Oscillator (fxt)

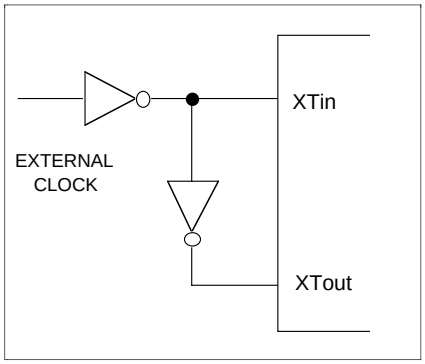


Figure 24. External Oscillator (fxt)

POWER CONTROL REGISTER (PCON)

The power control register, PCON, is used to select the CPU clock frequency and to control CPU operating and power-down modes.

PCON bits 3 and 2 are controlled by the STOP and IDLE instructions which engage the Idle and Stop power-down modes. Idle and Stop modes can be initiated by these instructions regardless of the current value of the enable memory bank flag (EMB).

Table 11. Power Control Register (PCON) Organization (4-Bit W)

PCON Bit Settings		Resulting CPU Operating Mode
PCON.3	PCON.2	
0	0	Normal CPU operating mode
0	1	Idle power-down mode
1	0	Stop power-down mode

PCON Bit Settings		Resulting CPU Clock Frequency	
PCON.1	PCON.0	If SCMOD.0 = "0"	If SCMOD.0 = "1"
0	0	fx/64	—
1	0	fx/8	—
1	1	fx/4	fxt/4

☞ **PROGRAMMING TIP — Setting the CPU Clock**

To set the CPU clock to 0.95 μs at 4.19 MHz:

```
BITS    EMB
SMB     15
LD      A,#3H
LD      PCON,A
```

INSTRUCTION CYCLE TIMES

The unit of time that equals one machine cycle varies depending on the main system clock is used, and on how the oscillator clock signal is divided (by 4, 8, or 64).

Table 12. Instruction Cycle Times for CPU Clock Rates

Selected CPU Clock	Resulting Frequency	Oscillation Source	Cycle Time (μs)
fx/64	65.5 kHz	fx=4.19 MHz	15.3
fx/8	524.0 kHz		1.91
fx/4	1.05 MHz		0.95
fxt/4	8.19 kHz	fxt=32.768 kHz	122.0

SYSTEM CLOCK MODE REGISTER (SCMOD)

The system clock mode register, SCMOD, is used to select the CPU clock and to control main system clock oscillation. Only its least significant and most significant bits can be manipulated by 1-bit write instructions. Bits 2 and 1 in the SCMOD register are always logic zero.

Subsystem clock oscillation cannot, of course, be stopped internally. Also, if you have selected fx as the CPU clock, setting SCMOD.3 to "1" will not stop main system clock oscillation. This can only be done by a STOP instruction.

Table 13. System Clock Mode Register (SCMOD) Organization

SCMOD Register Bit Settings		Resulting Clock Selection	
SCMOD.3	SCMOD.0	CPU Clock	fx Oscillation
0	0	fx	On
0	1	fxt	On
1	1	fxt	Off

SWITCHING THE CPU CLOCK

Together, bit settings in the power control register, PCON, and the system clock mode register, SCMOD, determine whether a main system or a subsystem clock is selected as the CPU clock. This makes it possible to switch dynamically between main and subsystem clocks and to modify operating frequencies.

NOTE

A clock switch operation does not go into effect immediately when you make the SCMOD and PCON register modifications — the previously selected clock continues to run for a certain number of machine cycles.

For example, you are using the default CPU clock (normal operating mode and a main system clock of fx/64) and you want to switch from the fx clock to a subsystem clock and to stop the main system clock. To do this, you first need to set SCMOD.0 to "1". This switches the clock from fx to fxt but allows main system clock oscillation to continue. Before the switch actually goes into effect, a certain number of machine cycles must elapse. After this time interval, you can disable main system clock oscillation by setting SCMOD.3 to "1".

This same 'stepped' approach must be taken to switch from a subsystem clock to the main system clock: first, clear SCMOD.3 to "0" to enable main system clock oscillation. Then, after a certain number of machine cycles have elapsed, select the main system clock by clearing all SCMOD values to logic zero.

Following a RESET , CPU operation starts with the lowest main system clock frequency of 15.3 μs at 4.19MHz after the standard oscillation stabilization interval of 31.3 ms has elapsed. Table 14 details the number of machine cycles that must elapse before a CPU clock switch modification goes into effect.

Table 14. Elapsed Machine Cycles During CPU Clock Switch

BEFORE	AFTER	SCMOD.0 = 0						SCMOD.0 = 1
		PCON.1 = 0	PCON.0 = 0	PCON.1 = 1	PCON.0 = 0	PCON.1 = 1	PCON.0 = 1	
SCMOD.0 = 0	PCON.1 = 0	N/A		1 MACHINE CYCLE		1 MACHINE CYCLE		N/A
	PCON.0 = 0							
	PCON.1 = 1	8 MACHINE CYCLES		N/A		8 MACHINE CYCLES		N/A
	PCON.0 = 0							
	PCON.1 = 1	16 MACHINE CYCLES		16 MACHINE CYCLES		N/A		fx / 4fxt
	PCON.0 = 1							
SCMOD.0 = 1		N/A		N/A		fx / 4fxt (M/C)		N/A

NOTES:
1. Even if oscillation is stopped by setting SCMOD.3 during main system clock operation, Stop mode is not entered.
2. Since the Xin input is connected internally to V_{SS} to avoid current leakage due to the crystal oscillator in Stop mode, do not set SCMOD.3 to "1" when an external clock is used as the main system clock.
3. When the system clock is switched to the subsystem clock, it is necessary to disable any interrupts which may occur during the time intervals shown in Table 14.
4. 'N/A' means 'not available'.

☞ **PROGRAMMING TIP — Switching Between Main System and Subsystem Clock**

1. Switch from the main system clock to the subsystem clock:


```
MA2SUB  BITS   SCMOD.0     ;  Switches to subsystem clock
        CALL   DLY80       ;  Delay 80 machine cycles
        BITS   SCMOD.3     ;  Stop the main system clock
        RET
DLY80   LD     A,#0FH
DEL1    NOP
        NOP
        DECS   A
        JR     DEL1
        RET
```

2. Switch from the subsystem clock to the main system clock:

```
SUB2MA  BITR   SCMOD.3     ;  Start main system clock oscillation
        CALL   DLY80       ;  Delay 80 machine cycles
        BITR   SCMOD.0     ;  Switch to main system clock
        RET
```

CLOCK OUTPUT MODE REGISTER (CLMOD)

The clock output circuit is used to output clock pulses to the CLO pin. The clock output mode register, CLMOD, is used to enable or disable clock output to the CLO pin and to select the CPU clock source and frequency.

To output a frequency, the clock output pin CLO/P3.2 must be set to output mode and the latch for the pin must be cleared to "0". Bit 2 in the CLMOD register must always be "0".

Table 15. Clock Output Mode Register (CLMOD) Organization

CLMOD Bit Settings		Resulting Clock Output	
CLMOD.1	**CLMOD.0**	**Clock Source**	**Frequency**
0	0	CPU clock (fx/4, fx/8, fx/64, fxt/4)	1.05 MHz, 524 kHz, 65.5 kHz, 8.19 kHz
0	1	fxx/8	524 kHz, 4.096 kHz
1	0	fxx/16	262 kHz, 2.048 kHz
1	1	fxx/64	65.5 kHz, 0.512 kHz

CLMOD.3	Result of CLMOD.3 Setting
0	Clock output is disabled
1	Clock output is enabled

NOTE: Frequencies assume that fx is 4.19 MHz and fxt is 32.768 kHz.

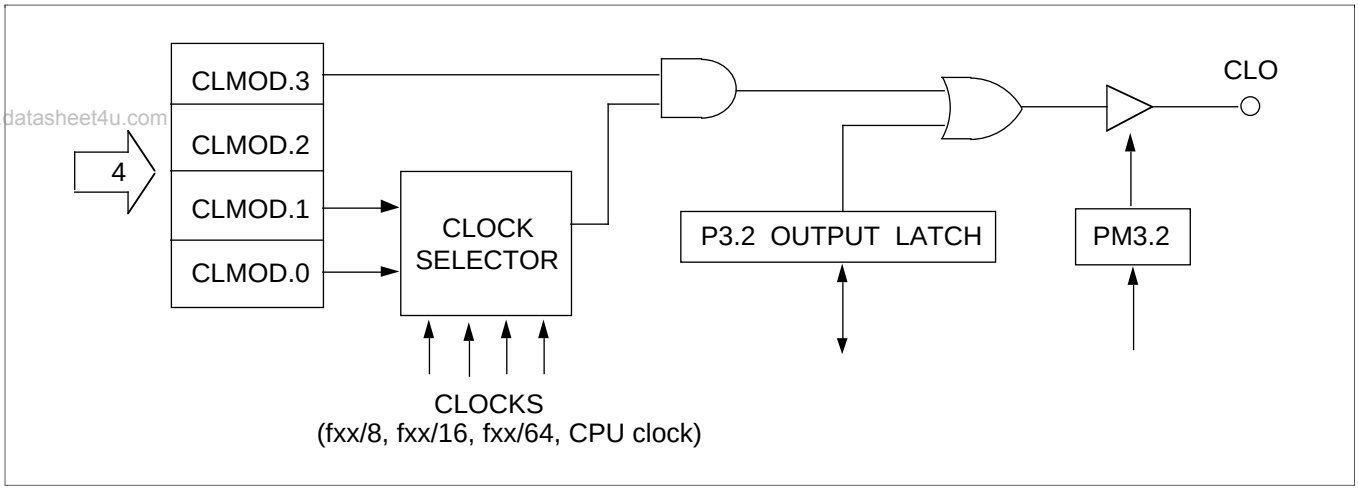


Figure 25. CLO Output Pin Circuit Diagram

☞ PROGRAMMING TIP — CPU Clock Output to the CLO Pin

To output the CPU clock to the CLO pin:

```
BITS    EMB             ;   Or BITR EMB
SMB     15
LD      EA,#40H
LD      PMG2,EA         ;   P3.2 ← Output mode
BITR    P3.2            ;   Clear P3.2 output latch
LD      A,#9H
LD      CLMOD,A
```

POWER-DOWN

The KS57C2408A/2416A microcontroller has two power-down modes to reduce power consumption: Idle and Stop. In Idle mode, the CPU clock stops while peripherals and the oscillator continue to operate normally.

In Stop mode, system clock oscillation is halted (assuming it is currently operating), and peripheral hardware components are powered-down. The effect of Stop mode on specific peripheral component (CPU, basic timer, serial I/O, timer/ counters 0 and 1, watch timer, and LCD controller) and on external interrupt requests, is detailed in Table 16.

Table 16. Hardware Operation During Power-Down Modes

Operation	Stop Mode (STOP)	Idle Mode (IDLE)
System clock status	Can be changed only if the main system clock is used	Can be changed if the main system clock or subsystem clock is used
Clock oscillator	Main system clock oscillation stops	CPU clock oscillation stops (main and subsystem clock oscillation continues)
Basic timer	Basic timer stops	Basic timer operates (with IRQB set at each reference interval)
Serial interface	Operates only if external SCK input is selected as the serial I/O clock	Operates if a clock other than the CPU clock is selected as the serial I/O clock
Timer/counter 0	Operates only if TCL0 is selected as the counter clock	Timer/counter 0 is operational
Timer/counter 1	Operates only if TCL1 is selected as the counter clock	Timer/counter 1 is operational
Watch timer	Operates only if subsystem clock (fxt) is selected as the counter clock	Watch timer is operational
LCD controller	Operates only if a subsystem clock is selected as LCDCK	LCD controller is operational
External interrupts	INT1, INT2, and INT4 are acknowledged; INT0 is not serviced	INT1, INT2, and INT4 are acknowledged; INT0 is not serviced
CPU	All CPU operations are disabled	All CPU operations are disabled
Mode release signal	Interrupt request signals (except INT0) are enabled by an interrupt enable flag or by RESET input	Interrupt request signals (except INT0 and INTAD) are enabled by an interrupt enable flag or by RESET input
A/D converter	A/D converter is disabled	A/D converter is disabled

☞ PROGRAMMING TIP — Reducing Power Consumption for Key Input Interrupt Processing

The following code shows real-time clock and interrupt processing for key inputs to reduce power consumption. In this example, the system clock source is switched from the main system clock to a subsystem clock and the LCD display is turned on:

```
KEYCLK  DI
        CALL    MA2SUB      ;  Main system  clock → subsystem clock switch subroutine
        SMB     15
        LD      EA,#00H
        LD      P4,EA       ;  All key strobe outputs to low level
        LD      A,#3H
        LD      IMOD2,A     ;  Select KS0–KS7 enable
        SMB     0
        BITR    IRQW
        BITR    IRQ2
        BITS    IEW
        BITS    IE2
CLKS1   CALL    WATDIS      ;  Execute clock and display changing subroutine
        BTSTZ   IRQ2
        JR      CIDLE
        CALL    SUB2MA      ;  Subsystem clock  → main system clock switch subroutine
        EI
        RET
CIDLE   IDLE                ;  Engage idle mode
        NOP
        NOP
        JPS     CLKS1
```

RECOMMENDED CONNECTIONS FOR UNUSED PINS

To reduce overall power consumption, please configure unused pins according to the guidelines described in Table 17.

Table 17. Unused Pin Connections for Reduced Power Consumption

Pin/Share Pin Names	Recommended Connection
P0.0 / SCK P0.1 / SO P0.2 / SI P0.3 / BTCO	Input mode: Connect to V_{DD} Output mode: Do not connect
P1.0 / INT0 – P1.2 / INT2	Connect to V_{DD}
P1.3 / INT4	Connect to V_{SS}
P2.0 / TCL0 P2.1 / TCL1 P2.2 P2.3 P3.0 / TCLO0 P3.1 / TCLO1 P3.2 / CLO P3.3 / BUZ P4.0–P4.3 P5.0–P5.3 P6.0 / KS0 – P6.3 / KS3 P7.0 / KS4 – P7.3 / KS7	Input mode: Connect to V_{DD} Output mode: Do not connect
P9.0 / AD0 – P9.3 / AD3 P10.0 / AD4 – P10.1 / AD5	Connect to V_{SS}
SEG0–SEG23 SEG24 / P8.0 – SEG31 / P8.7 COM0–COM3	Do not connect
V_{LC0}–V_{LC2}	Connect to V_{SS}
BIAS	If all of the V_{LC0}–V_{LC2} pins are unused, connect BIAS to V_{SS}
XT_{in}	Connect XT_{in} to V_{SS} or V_{DD}
XT_{out}	Do not connect
TEST	Connect to V_{SS}

RESET

Table 18 provides detailed information about hardware register values after a RESET occurs during power-down mode or during normal operation.

Table 18. Hardware Register Values After RESET

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
Program counter (PC)	Lower five bits of address 0000H are transferred to PC12–8, and the contents of 0001H to PC7–0.	Lower five bits of address 0000H are transferred to PC12–8, and the contents of 0001H to PC7–0.
Program Status Word (PSW)		
Carry flag (C)	Retained	Undefined
Skip flag (SC0–SC2)	0	0
Interrupt status flags (IS0, IS1)	0	0
Bank enable flags (EMB, ERB)	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.	Bit 6 of address 0000H in program memory is transferred to the ERB flag, and bit 7 of the address to the EMB flag.
Stack pointer (SP)	Undefined	Undefined
Data Memory (RAM)		
Registers E, A, L, H, X, W, Z, Y	Values retained (note1)	Undefined
General-purpose registers	Values retained	Undefined
Bank selection registers (SMB, SRB)	0, 0	0, 0
BSC register (BSC0–BSC3)	0	0
Oscillator Circuits		
Power control register (PCON)	0	0
Output mode register (CLMOD)	0	0
System clock control reg (SCMOD)	0	0
Interrupts		
Interrupt request flags (IRQx)	0	0
Interrupt enable flags (IEx)	0	0
Interrupt priority flag (IPR)	0	0
Interrupt master enable flag (IME)	0	0
INT0 mode register (IMOD0)	0	0
INT1 mode register (IMOD1)	0	0
INT2 mode register (IMOD2)	0	0

Note1: The values of the 0F8H-0FDH are not retained when a RESET signal is input.

Table 18. Hardware Register Values After RESET (Continued)

Hardware Component or Subcomponent	If RESET Occurs During Power-Down Mode	If RESET Occurs During Normal Operation
I/O Ports		
Output buffers	Off	Off
Output latches	0	0
Port mode flags (PM)	0	0
Pull-up resistor mode reg (PUMOD)	0	0
Basic Timer		
Count register (BCNT)	Undefined	Undefined
Mode register (BMOD)	0	0
Basic timer output enable flag (BOE)	0	0
TC0, TC1		
Count registers (TCNT0/1)	0	0
Reference registers (TREF0/1)	FFH, FFFFH	FFH, FFFFH
Mode registers (TMOD0/1)	0	0
T/C output enable flags (TOE0/1)	0	0
Watch Timer		
Watch timer mode register (WMOD)	0	0
LCD Controller/Driver		
LCD mode register (LMOD)	0	0
LCD control register (LCON)	0	0
Display data memory	Values retained	Undefined
Output buffers	Off	Off
A/D Converter		
A/D mode register (ADMOD)	0	0
A/D data register	0	0
Serial I/O Interface		
SIO mode register (SMOD)	0	0
SIO interface buffer (SBUF)	Values retained	Undefined

I/O PORTS

The KS57C2408A/2416A microcontroller has eleven I/O ports. There are 10 input pins, 12 output pins, 20 configurable I/O pins, and 8 n-channel open-drain I/O pins, for a total of 50 I/O pins.

PORT MODE FLAGS (PM FLAGS)

Port mode flags (PM) are used to configure ports 0 and 2–7 to input or output mode by setting or clearing the corresponding I/O buffer. If a PM bit = "0", the corresponding I/O pin is set to input mode. If the PM bit = "1", the pin is set to output mode.

Table 19. Port Mode Group Flags (8-Bit W)

PM Group ID	Address	Bit 3	Bit 2	Bit 1	Bit 0
PMG1	FE8H	PM0.3	PM0.2	PM0.1	PM0.0
	FE9H	PM7	"0"	PM5	PM4
PMG2	FEAH	PM2.3	PM2.2	PM2.1	PM2.0
	FEBH	PM3.3	PM3.2	PM3.1	PM3.0
PMG3	FECH	PM6.3	PM6.2	PM6.1	PM6.0
	FEDH	"0"	"0"	"0"	"0"

NOTE: If a PM bit = "0", the corresponding I/O pin is set to input mode. If bit = "1", the pin is set to output mode. All flags are cleared to "0" by RESET .

☞ **PROGRAMMING TIP — Configuring I/O Ports as Input or Output**

The following instructions configure P0.3 and P2 to output and the remaining ports to input:

```
BITS    EMB
SMB     15
LD      EA,#08H
LD      PMG1,EA         ;   P0.3 ← output, P0.0–0.2, P4, P5, P7 ← input
LD      EA,#0FH
LD      PMG2,EA         ;   P2.0–2.3 ← output, P3.0–3.3 ← input
LD      EA,#00H
LD      PMG3,EA         ;   P6.0–6.3 ← input
```

PULL-UP RESISTOR MODE REGISTERS

The pull-up resistor mode register (PUMOD) is used to assign internal pull-up resistors to specific I/O ports. When a PUMOD bit = "1", a pull-up resistor is assigned to the corresponding I/O port: PUMOD.3 for port 3, PUMOD.2 for port 2, and so on. I/O ports 4 and 5 are an exception, as these port pins may only be assigned internal pull-up resistors via mask option. PUMOD bits 4 and 5 should always be cleared to logic zero.

When a configurable I/O port pin is used as an output pin, its assigned pull-up resistor is automatically disabled, even though the pin's pull-up may be enabled by a corresponding PUMOD bit setting.

Table 20. Pull-Up Resistor Mode Register (PUMOD) Organization (8-Bit W)

Address	Bit 3	Bit 2	Bit 1	Bit 0
FDCH	PUMOD.3	PUMOD.2	PUMOD.1	PUMOD.0
FDDH	PUMOD.7	PUMOD.6	"0"	"0"

☞ PROGRAMMING TIP — Enabling and Disabling I/O Port Pull-Up Resistors

P6 and P7 enable pull-up resistors, P0–P3 disable pull-up resistors.

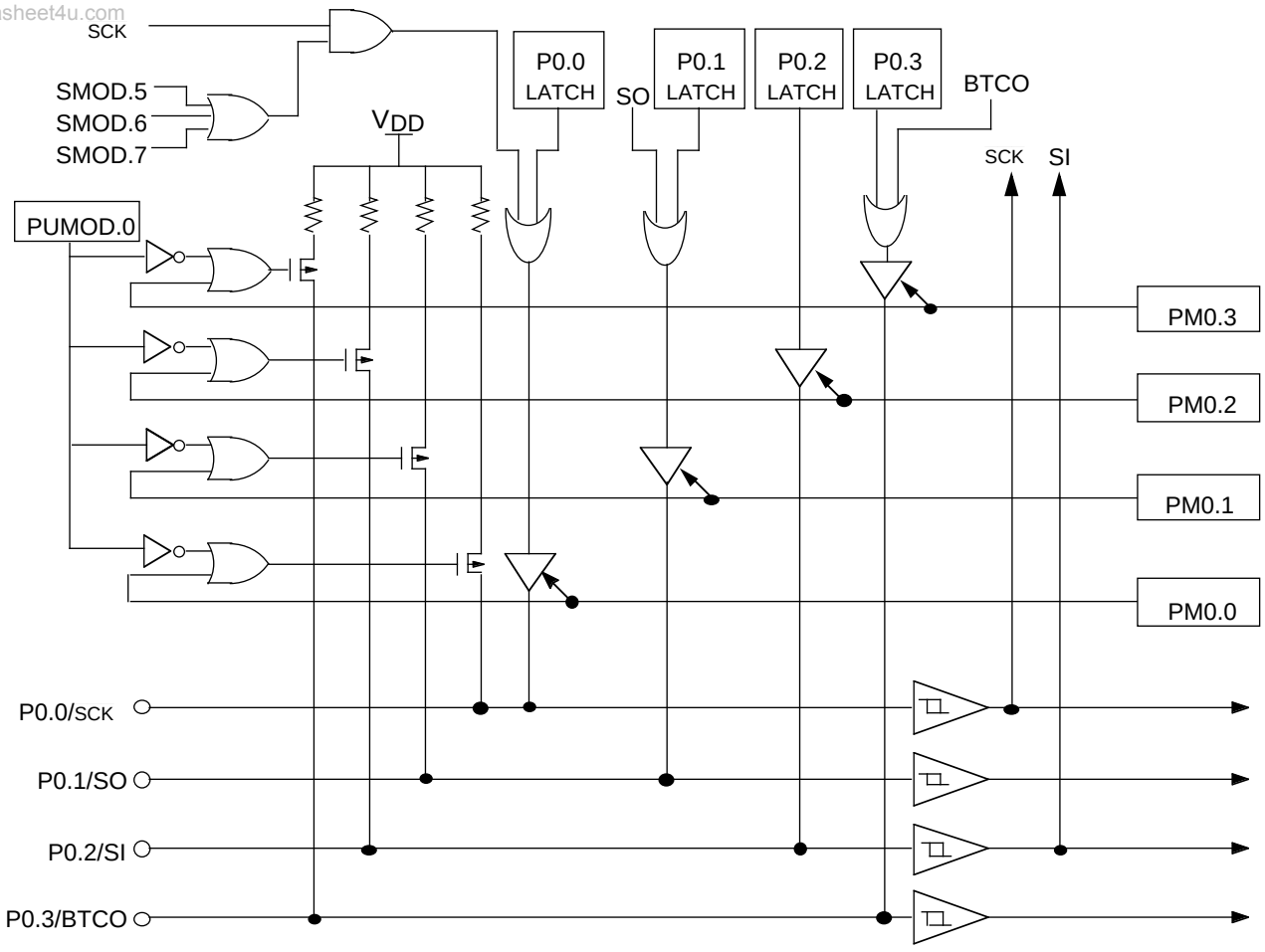
```
BITS    EMB
SMB     15
LD      EA,#0C0H
LD      PUMOD,EA        ;   P6 and P7 enable
```

PIN ADDRESSING FOR OUTPUT PORT 8

The addresses for the port 8 1-bit output pin buffers are located in bank 1 of data memory instead of bank 15. To address port 8 output pins, use the settings EMB = 1 and SMB = 1.

The LCD mode register, LMOD is used to control whether the pin address is used for LCD data output or for normal data output.

PORT 0 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 26. Port 0 Circuit Diagram

PORT 1 CIRCUIT DIAGRAM

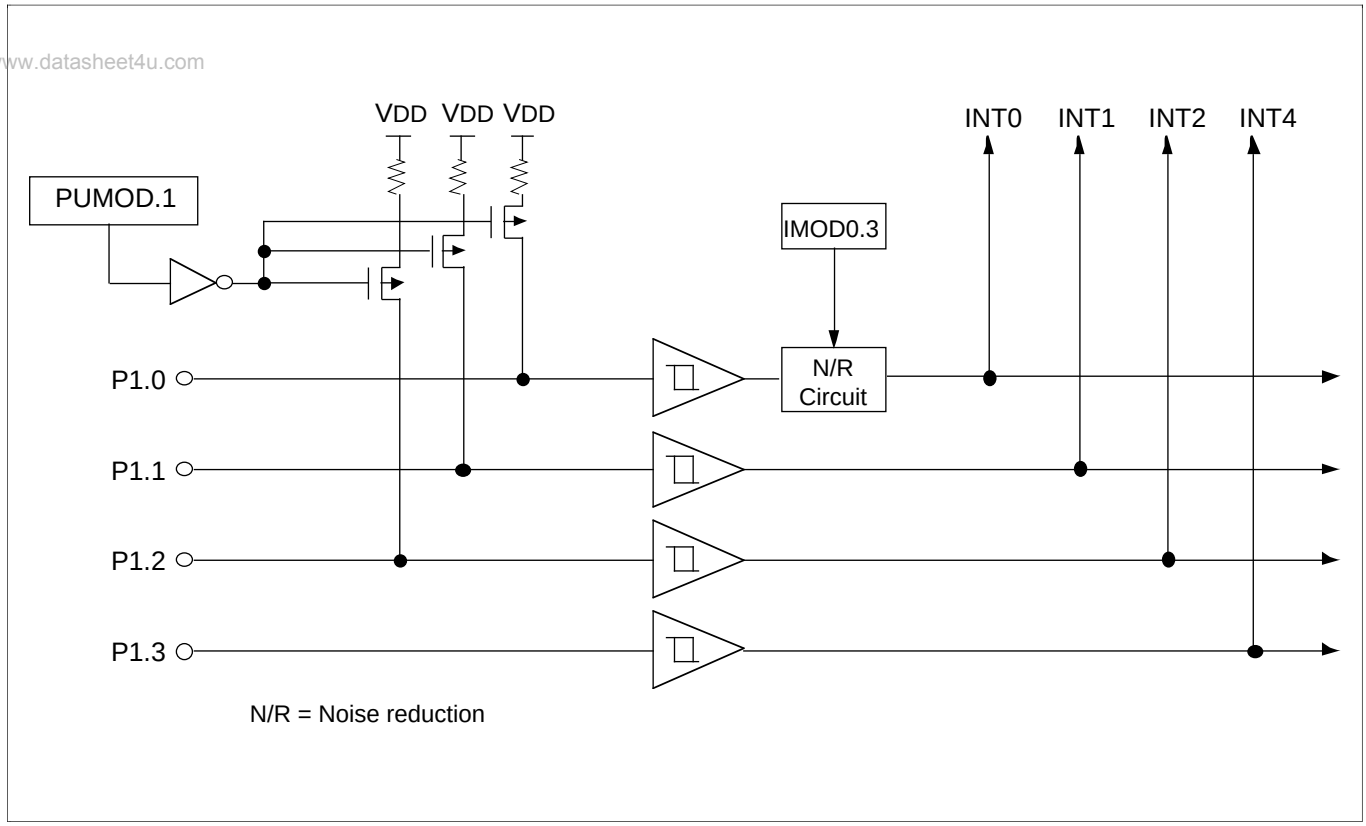
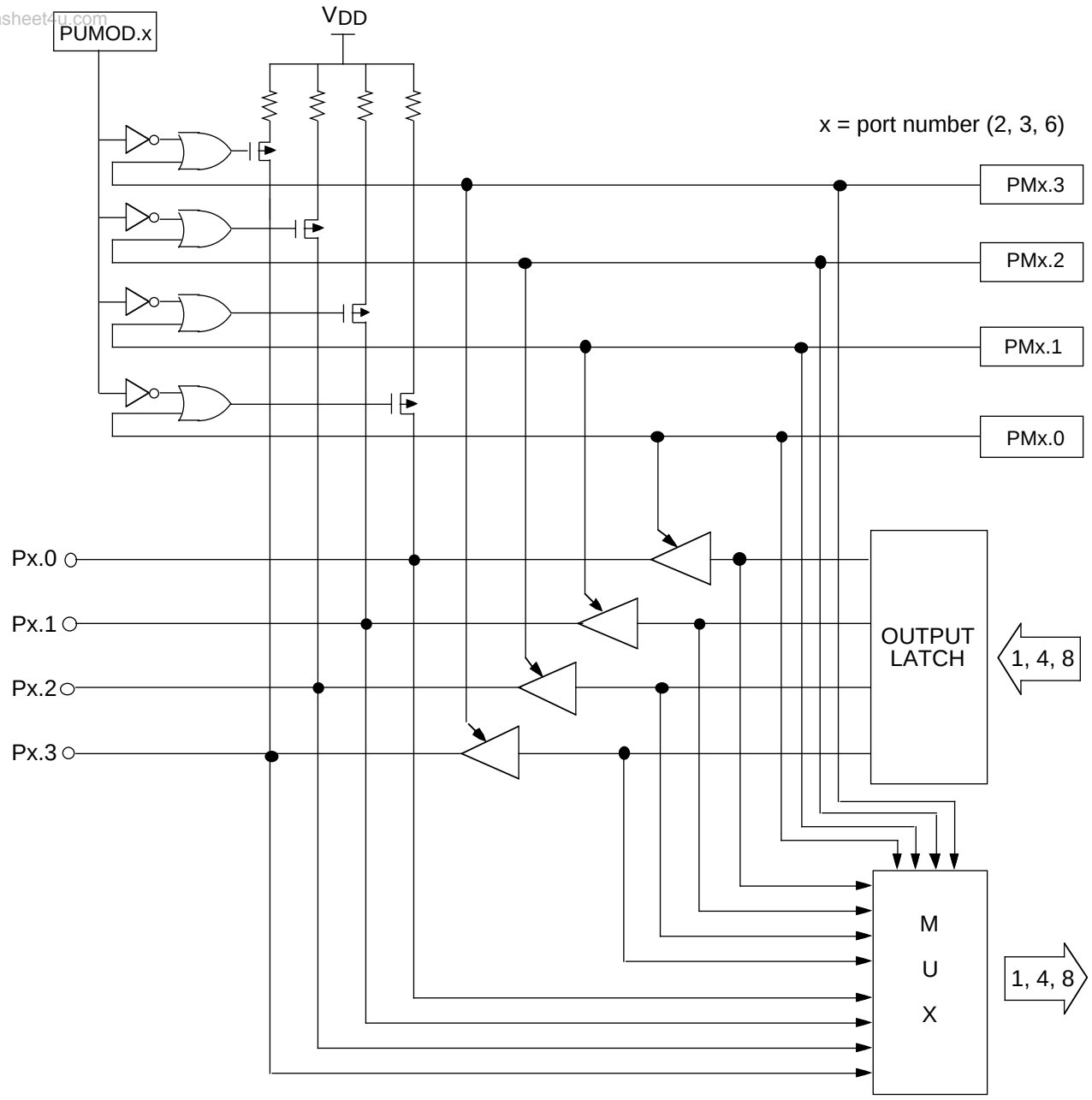


Figure 27. Port 1 Circuit Diagram

PORT 2, 3, 6 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD). The 8–bit access is impossible at port 2 and 3.

Figure 28. Port 2, 3, and 6 Circuit Diagram

PORT 4, 5 CIRCUIT DIAGRAM

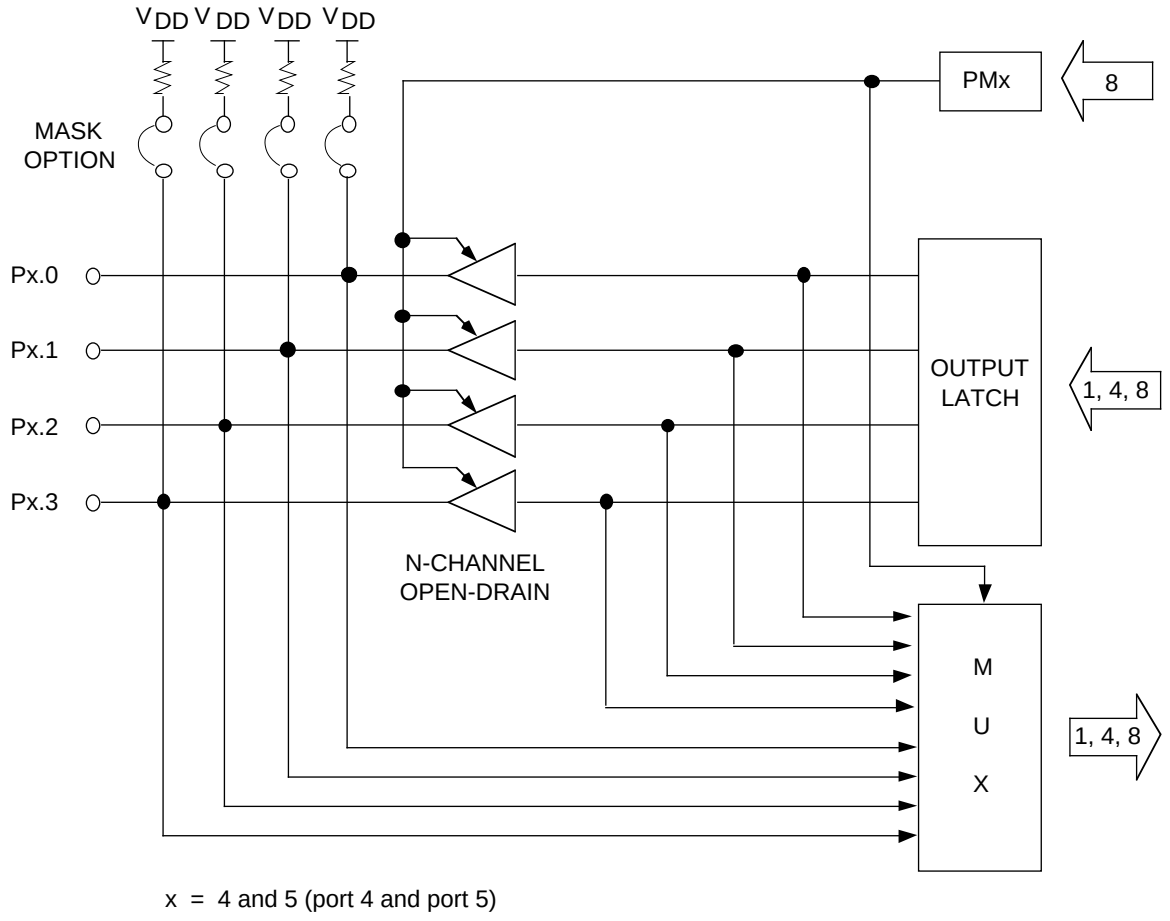
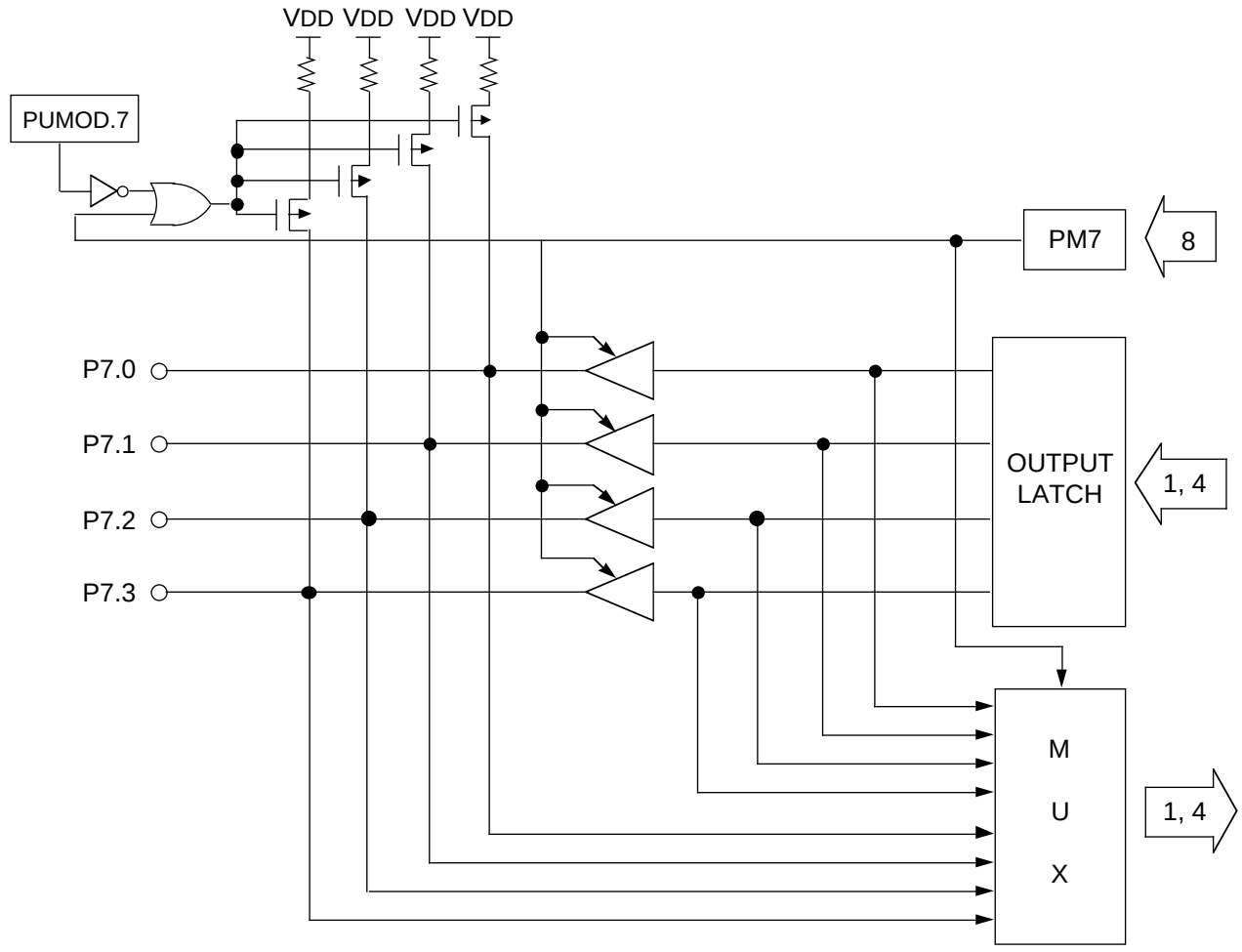


Figure 29. Port 4 and 5 Circuit Diagram

PORT 7 CIRCUIT DIAGRAM



NOTE: When a port pin acts as an output, its pull-up resistor is automatically disabled, even though the port's pull-up resistor is enabled by bit settings to the pull-up resistor mode register (PUMOD).

Figure 30. Port 7 Circuit Diagram

BASIC TIMER (BT)

The basic timer generates interrupt requests at precise intervals. You can use the basic timer as a "watchdog" timer for monitoring system events or use BT output to stabilize clock oscillation when Stop mode is released by an interrupt and following RESET .

Interval Timer Function

The measurement of elapsed time intervals is the basic timer's primary function. The standard interval is 256 BT clock pulses. To restart the basic timer, set bit 3 of the mode register BMOD to "1". The 8-bit counter register, BCNT, is incremented each time a clock signal is detected that corresponds to the frequency selected by BMOD. BCNT continues incrementing as it counts BT clocks until an overflow occurs. An overflow causes the BT interrupt request flag (IRQB) to be set to "1" to signal that the designated time interval has elapsed. An interrupt request is then generated, BCNT is cleared to "0", and counting continues from 00H.

Watchdog Timer Function

The basic timer can also be used as a "watchdog" timer to signal the occurrence of specific system events. Each time BCNT overflows, an overflow signal is sent to the basic timer clock output pin, BTCO. To enable BTCO output operation, clear the output latch for pin P0.3 to "0" and set the port mode flag for P0.3 (PM0.3) to "1".

Oscillation Stabilization Interval Control

Setting bits 2–0 of the BMOD register determines the time interval (also referred to as 'wait time') required to stabilize clock signal oscillation when power-down mode is released by an interrupt. When a RESET signal is generated , the standard stabilization interval for system clock oscillation following a RESET is 31.3ms at 4.19 MHz.

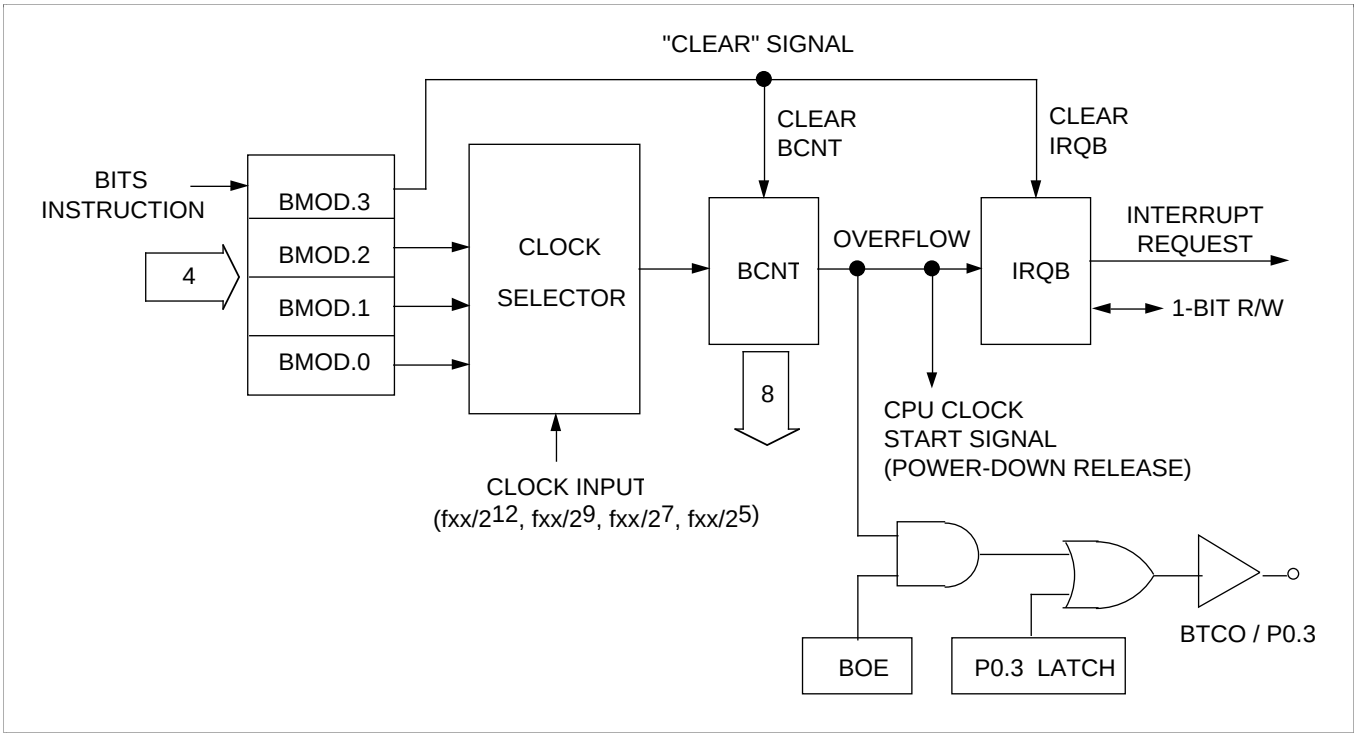


Figure 31. Basic Timer Circuit Diagram

BASIC TIMER MODE REGISTER (BMOD)

The basic timer mode register, BMOD, is used to select input frequency and oscillation stabilization time. The most significant bit of the BMOD register, BMOD.3, is used to start the basic timer again. When BMOD.3 is set to "1", the contents of the BT counter register (BCNT) and the BT interrupt request flag (IRQB) are both cleared to "0", and timer operation is restarted.

Table 21. Basic Timer Mode Register (BMOD) Organization

BMOD.3	Basic Timer Restart Bit
1	Restart basic timer; clear IRQB, BCNT, and BMOD.3 to "0"

BMOD.2	BMOD.1	BMOD.0	Basic Timer Input Clock	Oscillation Stabilization
0	0	0	fxx/2^{12} (1.02 kHz)	2^{20}/fxx (250 ms)
0	1	1	fxx/2^{9} (8.18 kHz)	2^{17}/fxx (31.3 ms)
1	0	1	fxx/2^{7} (32.7 kHz)	2^{15}/fxx (7.82 ms)
1	1	1	fxx/2^{5} (131 kHz)	2^{13}/fxx (1.95 ms)

NOTES:
1. Clock frequencies and stabilization intervals assume a system oscillator clock frequency (fxx) of 4.19 MHz.
2. fxx = selected system clock frequency.
3. Oscillation stabilization time is the time required to stabilize clock signal oscillation after stop mode is released. The data in the table column 'Oscillation Stabilization' can also be interpreted as "Interrupt Interval Time."
4. The standard stabilization time for system clock oscillation following a RESET is 31.3 ms at 4.19 MHz.

BASIC TIMER COUNTER (BCNT)

BCNT is an 8-bit counter register for the basic timer. When BCNT has incremented to hexadecimal 'FFH', it is cleared to '00H' and an overflow is generated. The overflow causes the interrupt request flag, IRQB, to be set to "1". When the interrupt request is generated, BCNT immediately resumes counting incoming clock signals.

NOTE

Always execute a BCNT read operation twice to eliminate the possibility of reading unstable data while the counter is incrementing. If, after two consecutive reads, the BCNT values match, you can select the latter value as valid data. Until the results of the consecutive reads match, however, the read operation must be repeated until the validation condition is met.

BASIC TIMER OUTPUT ENABLE FLAG (BOE)

The BOE flag value enables and disables basic timer output to the BTCO/P0.3. When BOE is "0", basic timer output to the BTCO pin is disabled; when it is "1", BT output to the BTCO pin is enabled.

F92H — 1-Bit R/W

TOE1	TOE0	**BOE**	0

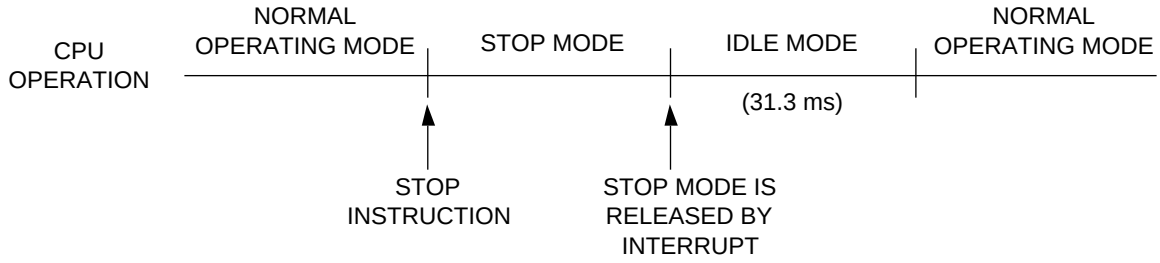
☞ PROGRAMMING TIP — Using the Basic Timer

1. To read the basic timer count register (BCNT):

```
        BITS    EMB
        SMB     15
BCNTR   LD      EA,BCNT
        LD      YZ,EA
        LD      EA,BCNT
        CPSE    EA,YZ
        JR      BCNTR
```

2. When Stop mode is released by an interrupt, set the oscillation stabilization interval to 31.3 ms:

```
        BITS    EMB
        SMB     15
        LD      A,#0BH
        LD      BMOD,A          ;   Wait time is 31.3 ms
        STOP                    ;   Set stop power-down mode
        NOP
        NOP
```



3. To set the basic timer interrupt interval time to 1.95 ms (at 4.19 MHz):

```
        BITS    EMB
        SMB     15
        LD      A,#0FH
        LD      BMOD,A
        EI
        BITS    IEB             ;   Basic timer interrupt enable flag is set to "1"
```

4. Clear BCNT and the IRQB flag and restart the basic timer:

```
        BITS    EMB
        SMB     15
        BITS    BMOD.3
```

8-BIT TIMER/COUNTER 0 (TC0)

Timer/counter 0 (TC0) is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals.

To indicate that an event has occurred, or that a specified time interval has elapsed, TC generates an interrupt request. By counting signal transitions and comparing the current counter value with the reference register value, TC can be used to measure specific time intervals.

Timer/counter 0 can supply a clock signal to the clock selector circuit of the serial I/O interface for data shifter and clock counter operations. (These internal SIO operations are controlled in turn by the SIO mode register, SMOD). This clock generation function lets you adjust data transmission rates across the serial interface.

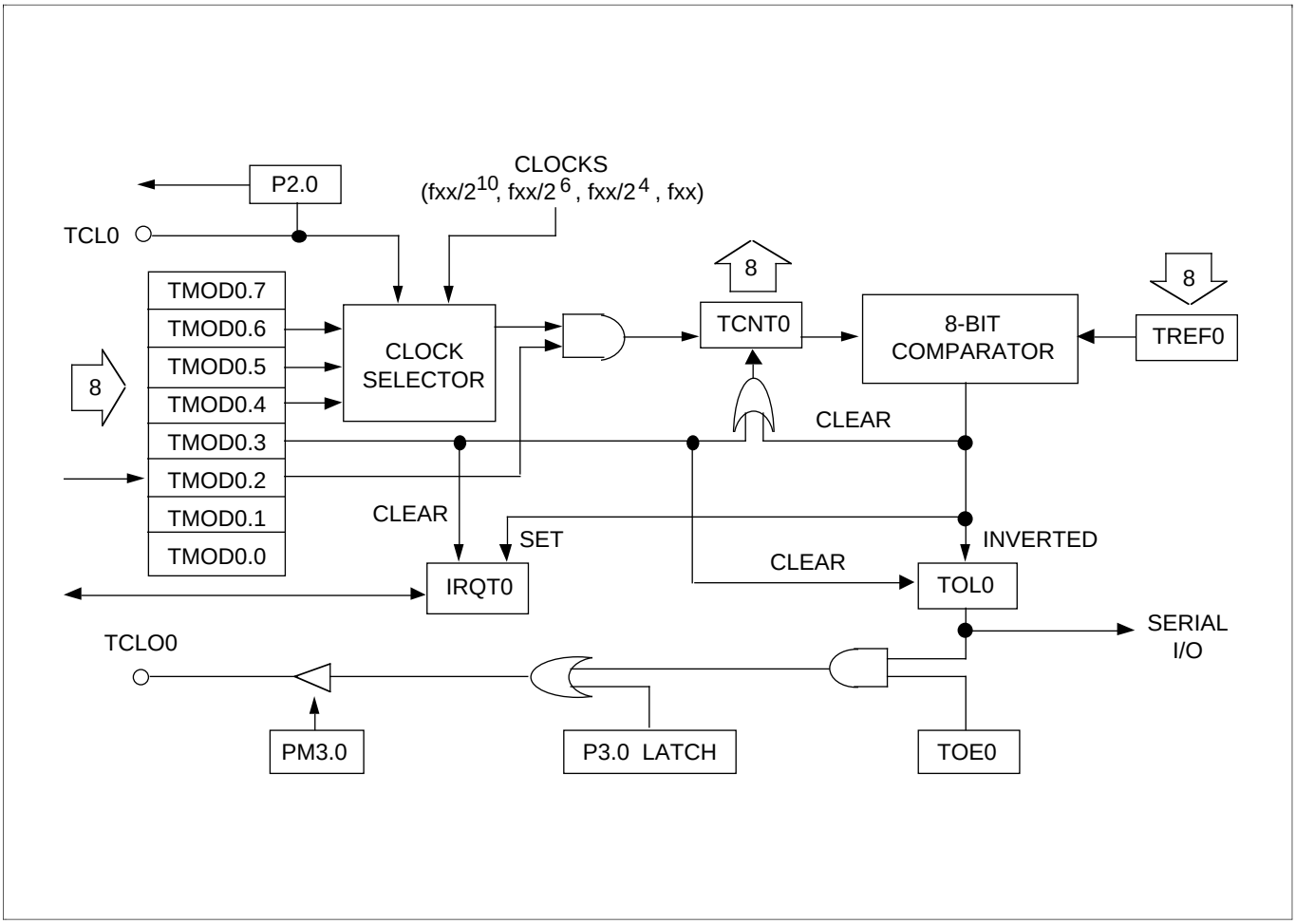


Figure 32. TC0 Circuit Diagram

PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 0 can be programmed to generate interrupt requests at various intervals based on the selected system clock frequency. Its 8-bit TC0 mode register TMOD0 is used to activate the timer/counter and to select the clock frequency. The reference register TREF0 stores the value for the number of clock pulses to be generated between interrupt requests.

The counter register, TCNT0, counts the incoming clock pulses, which are compared to the TREF0 value as TCNT0 is incremented. When there is a match (TREF0 = TCNT0), the TC0 interrupt request flag (IRQT0) is set to logic one, the status of TOL0 is inverted, and the interrupt is generated. The content of TCNT0 is then cleared to 00H and TC0 continues counting.

TC0 EVENT COUNTER FUNCTION

Timer/counter 0 can monitor or detect system 'events' by using the external clock input at the TCL0 pin as the counter source. With the exception of the different TMOD0.4–TMOD0.6 settings, the operation sequence for TC0's event counter function is identical to its programmable timer/counter function. To activate the TC0 event counter function, P2.0/TCL0 must be set to input mode.

Using timer/counter 0, a modifiable clock frequency can be output to the TC0 clock output pin, TCLO0. To enable the output to the TCLO0/P3.0, the I/O mode flag for P3.0 (PM3.0) must be set to output mode and output latch value for P3.0 must be cleared to "0" after the timer output enable flag (TOE0) is set to "1".

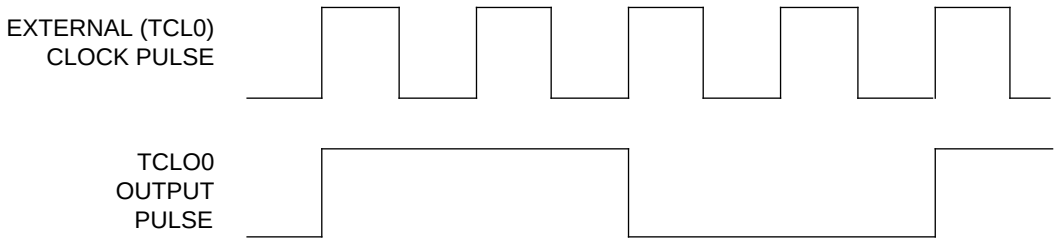
☞ PROGRAMMING TIP — TC0 Signal Output to the TCLO0 Pin

Output a 30 ms pulse width signal to the TCLO0 pin:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
LD      EA,#10H
LD      PMG2,EA         ;   P3.0 ← output mode
BITR    P3.0            ;   P3.0 clear
BITS    TOE0
```

☞ PROGRAMMING TIP — External TCL0 Clock Output to the TCLO0 Pin

Output external TCL0 clock pulse to the TCLO0 pin (divided by four):




```
BITS    EMB
SMB     15
LD      EA,#01H
LD      TREF0,EA
LD      EA,#0CH
LD      TMOD0,EA
LD      EA,#10H
LD      PMG2,EA         ;   P3.0 ← output mode
BITR    P3.0            ;   P3.0 clear
BITS    TOE0
```

TC0 MODE REGISTER (TMOD0)

TMOD0 is the 8-bit mode control register for timer/counter 0. When TMOD0.3 is set to "1", the contents of TCNT0, IRQT0, and TOL0 are cleared, counting starts from 00H, and TMOD0.3 is automatically reset to "0" for normal TC0 operation. When TC0 operation stops (TMOD0.2 = "0"), the contents of the TC0 counter register TCNT0 are retained until TC0 is re-enabled.

Table 22. TC0 Mode Register (TMOD0) Organization

Bit Name	Setting	Resulting TC0 Function	Address
TMOD0.7	0	Always logic zero	F91H
TMOD0.6 TMOD0.5 TMOD0.4	0,1	Specify input clock edge and internal frequency	
TMOD0.3	1	Clear TCNT0, IRQT0, and TOL0; then resume counting. (This bit is automatically cleared to "0" when counting resumes.)	F90H
TMOD0.2	0	Disable timer/counter 0; retain TCNT0 contents	
	1	Enable timer/counter 0	
TMOD0.1	0	Always logic zero	
TMOD0.0	0	Always logic zero	

Table 23. TMOD0.6, TMOD0.5, and TMOD0.4 Bit Settings

TMOD0.6	TMOD0.5	TMOD0.4	Resulting Counter Source and Clock Frequency
0	0	0	External clock input (TCL0) on rising edges
0	0	1	External clock input (TCL0) on falling edges
1	0	0	fxx/2^{10} (4.09 kHz)
1	0	1	fxx /2^{6} (65.5 kHz)
1	1	0	fxx/2^{4} (262 kHz)
1	1	1	fxx = 4.19 MHz

NOTE: 'fxx' = selected system clock of 4.19 MHz.

☞ **PROGRAMMING TIP — Restarting TC0 Counting Operation**

1. Set TC0 timer interval to 4.09 kHz:

```
BITS    EMB
SMB     15
LD      EA,#4CH
LD      TMOD0,EA
EI
BITS    IET0
```

2. Clear TCNT0, IRQT0, and TOL0; then restart TC0 counting operation:

```
BITS    EMB
SMB     15
BITS    TMOD0.3
```

TC0 REFERENCE REGISTER (TREF0)

TREF0 is used to store a reference value to be compared to the incrementing TCNT0 register in order to identify an elapsed time interval.

Use the following formula to calculate the correct value to load to the TREF0 reference register:

TC0 timer interval =

$$(\text{TREF0 value} + 1) \times \frac{1}{\text{TMOD0frequencysetting}}$$

Assuming TREF0 value $\neq$ 0

TC0 OUTPUT ENABLE FLAG (TOE0)

The 1-bit timer/counter 0 output enable flag TOE0 controls output from timer/counter 0 to the TCLO0 pin.

F92H 1-Bit R/W

TOE1	**TOE0**	BOE	"0"

When you set the TOE0 flag to "1", the contents of TOL0 can be output to the TCLO0 pin.

☞ PROGRAMMING TIP — Setting a TC0 Timer Interval

To set a 30 ms timer interval for TC0, given fx = 4.19 MHz, follow these steps.

1. Select the timer/counter 0 mode register with a maximum setup time of 62.5 ms (assume that the TC0 counter clock = $fx/2^{10}$, and TREF0 is set to FFH):

2. Calculate the TREF0 value:

$$30\ ms = \frac{TREF0value+1}{4.09kHz}$$

$$TREF0 + 1 = \frac{30ms}{244\mu s} = 122.9 = 7AH$$

TREF0 value = 7AH – 1 = 79H

3. Load the value 79H to the TREF0 register:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF0,EA
LD      EA,#4CH
LD      TMOD0,EA
```

16-BIT TIMER/COUNTER (TC1)

Timer/counter 1 (TC1) is used to count system 'events' by identifying the transition (high-to-low or low-to-high) of incoming square wave signals.

To indicate that an event has occurred, or that a specified time interval has elapsed, TC1 generates an interrupt request. By counting signal transitions, it can be used to measure time intervals.

The TC1 circuit also has 16-bit comparator logic. TC1 has a reloadable counter that consists of two parts: a 16-bit reference register (TREF1) into which you can write data for use as a reference value, and a 16-bit counter register (TCNT1) whose contents are automatically incremented by counter logic.

The only functional differences between TC0 and TC1 are the size of the counter and reference value registers (8-bit versus 16-bit), and that only TC0 can generate a clock signal for the serial I/O interface.

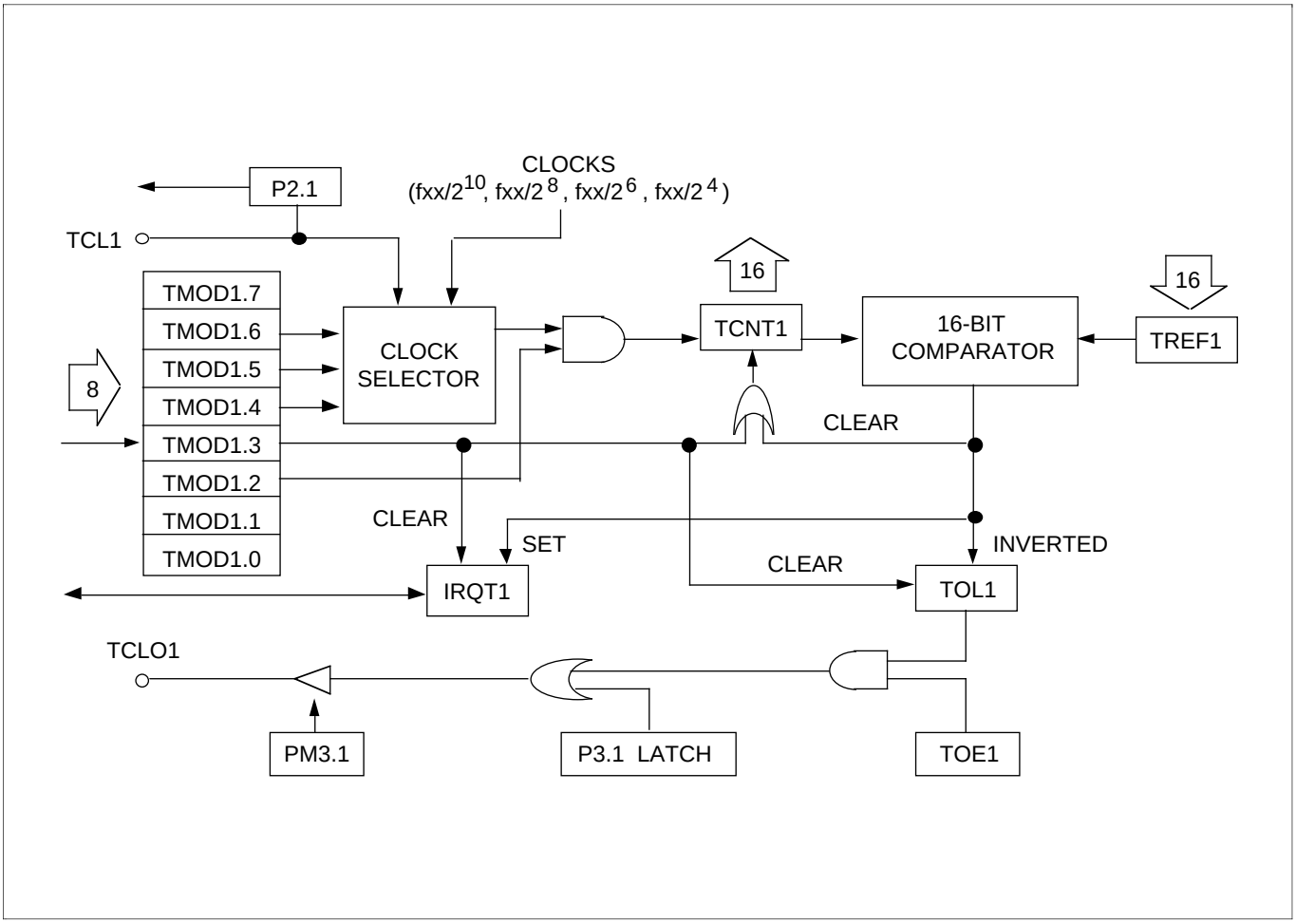


Figure 33. Timer/Counter 1 Circuit Diagram

PROGRAMMABLE TIMER/COUNTER FUNCTION

Timer/counter 1 can be programmed to generate interrupt requests at variable intervals, based on the system clock frequency you select. The 8-bit TC1 mode register, TMOD1, is used to activate the timer/counter and to select the clock frequency; the 16-bit reference register, TREF1, is used to store the value for the desired number of clock pulses between interrupt requests.

The 16-bit counter register, TCNT1, counts the incoming clock pulses, which are compared to the TREF1 value. When there is a match, the TC1 interrupt request flag (IRQT1) is set to logic one, the status of TOL1 is inverted, and the interrupt is output. The content of TCNT1 is then cleared to 0000H, and TC1 continues counting.

TC1 EVENT COUNTER FUNCTION

Timer/counter 1 can monitor system 'events' by using the external clock input at the TCL1 pin (I/O port 2.1) as the counter source. With the exception of the different TMOD1.4–TMOD1.6 settings, the operation sequence for TC1's event counter function is identical to its programmable timer/counter function. To activate the TC1 event counter function, P3.3/TCL1 must be set to input mode.

Using timer/counter 1, a modifiable clock frequency can be output to the TC1 clock output pin, TCLO1. To enable the output to the TCLO1/P3.1, P3.1 must be set to output mode and the latch for P3.1 must be cleared to "0" when timer output enable flag (TOE1) has been set to "1".

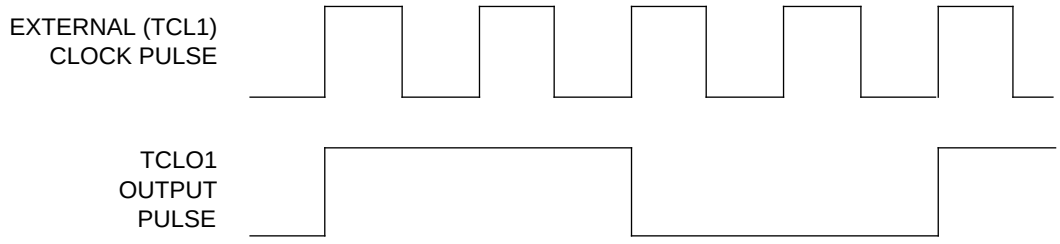
☞ PROGRAMMING TIP — TC1 Signal Output to the TCLO1 Pin

Output a 30 ms pulse width signal to the TCLO1 pin:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF1A,EA
LD      EA,#00H
LD      TREF1B,EA
LD      EA,#4CH
LD      TMOD1,EA
LD      EA,#02H
LD      PMG2,EA          ;   P3.1 ← output mode
BITR    P3.1             ;   P3.1 clear
BITS    TOE1
```

☞ PROGRAMMING TIP — External TCL1 Clock Output to the TCLO1 Pin

Output the external TCL1 clock source to the TCLO1 pin (divide by four):




```
BITS    EMB
SMB     15
LD      EA,#01H
LD      TREF1A,EA
LD      EA,#00H
LD      TREF1B,EA
LD      EA,#0CH
LD      TMOD1,EA
LD      EA,#02H
LD      PMG2,EA          ;   P3.1 ← output mode
BITR    P3.1             ;   P3.1 clear
BITS    TOE1
```

TC1 MODE REGISTER (TMOD1)

TMOD1 is the 8-bit mode register for timer/counter 1. When TMOD1.3 is set to "1", the contents of TCNT1, IRQT1, and TOL1 are cleared, counting starts from 0000H, and TMOD1.3 is automatically reset to "0" for normal TC1 operation. When TC1 operation stops (TMOD1.2 = "0"), the contents of the TC1 counter register, TCNT1, are retained until TC1 is re-enabled.

Table 24. TC1 Mode Register (TMOD1) Organization

Bit Name	Setting	Resulting TC1 Function	Address
TMOD1.7	0	Always logic zero	FA1H
TMOD1.6 TMOD1.5 TMOD1.4	0,1	Specify input clock edge and internal frequency	
TMOD1.3	1	Clear TCNT1, IRQT1, and TOL1 and resume counting immediately (This bit is automatically cleared to logic zero immediately after counting resumes.)	FA0H
TMOD1.2	0	Disable timer/counter 1; retain TCNT1 contents	
	1	Enable timer/counter 1	
TMOD1.1	0	Always logic zero	
TMOD1.0	0	Always logic zero	

Table 25. TMOD1.6, TMOD1.5, and TMOD1.4 Bit Settings

TMOD1.6	TMOD1.5	TMOD1.4	Resulting Counter Source and Clock Frequency
0	0	0	External clock input (TCL1) on rising edges
0	0	1	External clock input (TCL1) on falling edges
1	0	0	$fxx/2^{10}$ = 4.09 kHz
1	0	1	$fxx/2^{8}$ = 16.4 kHz
1	1	0	$fxx/2^{6}$ = 65.5 kHz
1	1	1	$fxx/2^{4}$ = 262 kHz

NOTE: 'fxx' = selected system clock of 4.19 MHz.

☞ **PROGRAMMING TIP — Restarting TC1 Counting Operation**

1. Set TC1 timer interval to 4.09 kHz:

```
BITS    EMB
SMB     15
LD      EA,#4CH
LD      TMOD1,EA
EI
BITS    IET1
```

2. Clear TCNT1, IRQT1, and TOL1; then restart TC1 counting operation:

```
SBITS   EMB
SMB     15
BITS    TMOD1.3
```

TC1 REFERENCE REGISTER (TREF1)

The TC1 reference register TREF1 is a 16-bit write-only register that is mapped to RAM locations FA8H–FA9H (TREF1A) and FAAH–FABH (TREF1B). It is addressable by 8-bit RAM control instructions.

Use the following formula to calculate the correct value to load to the TREF1 reference register:

TC1 timer interval =

$$(\text{TREF1 value} + 1) \times \frac{1}{\text{TMOD1frequencysetting}}$$

Assuming TREF1 value $\neq$ 0

TC1 OUTPUT ENABLE FLAG (TOE1)

The 1-bit timer/counter 1 output enable flag TOE1 controls output from timer/counter 1 to the TCLO1 pin.

F92H 1-Bit R/W

TOE1	TOE0	BOE	0

When you set the TOE1 flag to "1", the contents of TOL1 can be output to the TCLO1 pin.

☞ PROGRAMMING TIP — Setting a TC1 Timer Interval

To set a 30 ms timer interval for TC1, given fxx = 4.19 MHz, follow these steps.

1. Select the timer/counter 1 mode register with a maximum setup time of 16 seconds; assume the TC1 counter clock = $fxx/2^{10}$ and TREF1 is set to FFFFH.

2. Calculate the TREF1 value:

$$30\ ms = \frac{TREF1value+1}{4.09kHz}$$

$$TREF1 + 1 = \frac{30ms}{244\mu s} = 122.9 = 7AH$$

$$TREF1\ value = 7AH - 1 = 79H$$

3. Load the value 79H to the TREF1 register:

```
BITS    EMB
SMB     15
LD      EA,#79H
LD      TREF1A,EA
LD      EA,#00H
LD      TREF1B,EA
LD      EA,#4CH
LD      TMOD1,EA
```

WATCH TIMER

Watch timer functions include real-time and watch-time measurement and interval timing for the system clock. To start watch timer operation, set bit 2 of the watch timer mode register, WMOD.2, to "1". The watch timer starts, the interrupt request flag IRQW is automatically set to "1", and interrupt requests commence in 0.5-second intervals. Because the watch timer generates a quasi-interrupt instead of a vectored interrupt, the IRQW flag should be cleared to "0" by program software as soon as a requested interrupt service routine has executed.

The watch timer can generate a steady 2 kHz, 4 kHz, 8 kHz, or 16 kHz signal to the BUZ pin. To generate a BUZ signal, the output latch for I/O port 3.3 is cleared to "0" and the port 3.3 output mode flag (PM3.3) set to 'output' mode. By setting WMOD.1 to "1", the watch timer will function in high-speed mode, generating an interrupt every 3.91 ms. High-speed mode is useful for timing events for program debugging sequences.

The watch timer supplies the clock frequency for the LCD controller (f_{LCD}). Therefore, if the watch timer is disabled, the LCD controller does not operate.

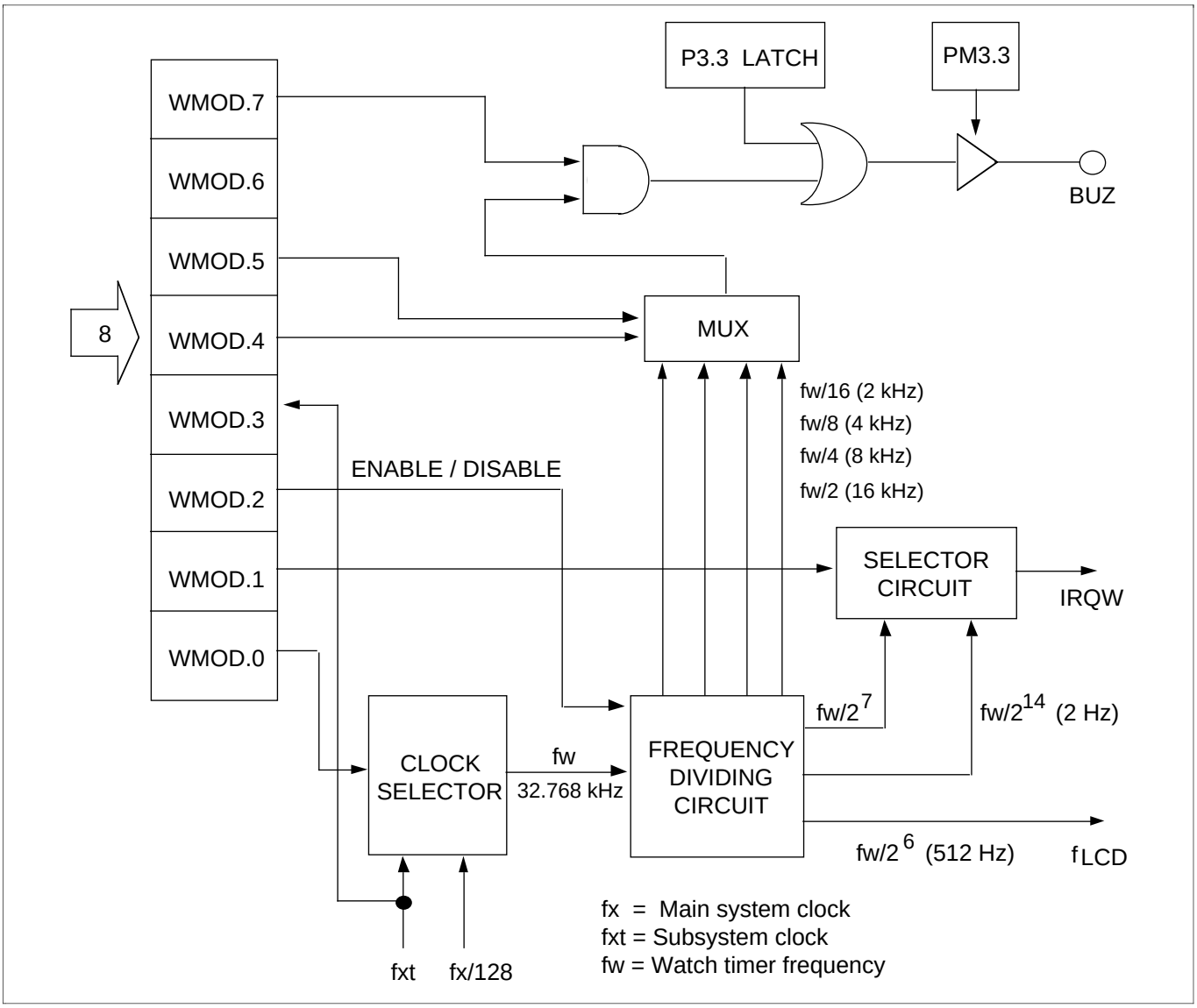


Figure 34. Watch Timer Circuit Diagram

WATCH TIMER MODE REGISTER (WMOD)

The watch timer mode register WMOD is used to select specific watch timer operations.

Table 26. Watch Timer Mode Register (WMOD) Organization (8-Bit W)

Bit Name	Values		Function	Address
WMOD.7	0		Disable buzzer (BUZ) signal output	F89H
	1		Enable buzzer (BUZ) signal output	
WMOD.6	0		Always logic zero	
WMOD.5 – .4	0	0	2 kHz buzzer (BUZ) signal output	
	0	1	4 kHz buzzer (BUZ) signal output	
	1	0	8 kHz buzzer (BUZ) signal output	
	1	1	16 kHz buzzer (BUZ) signal output	
WMOD.3	0		Input level to XT_{in} pin is low (read-only bit)	F88H
	1		Input level to XT_{in} pin is high (read-only bit)	
WMOD.2	0		Disable watch timer; clear frequency dividing circuits	
	1		Enable watch timer	
WMOD.1	0		Normal mode; sets IRQW to 0.5 s	
	1		High-speed mode; sets IRQW to 3.91 ms	
WMOD.0	0		Select (fx/128) as the watch timer clock (fw)	
	1		Select subsystem clock as watch timer clock (fw)	

NOTE: Main system clock frequency (fx) is assumed to be 4.19 MHz; subsystem clock (fxx) is assumed to be 32.768 kHz.

☞ PROGRAMMING TIP — Using the Watch Timer

1. Select a subsystem clock as the LCD display clock, a 0.5 second interrupt, and 2 kHz buzzer enable:

```
BITS    EMB
SMB     15
LD      EA,#80H
LD      PMG2,EA         ;   P3.3 ← output mode
BITR    P3.3
LD      EA,#85H
LD      WMOD,EA
BITS    IEW
```

2. Sample real-time clock processing method:

```
CLOCK   BTSTZ   IRQW    ;   0.5 second check
        RET             ;   No, return
        •               ;   Yes, 0.5 second interrupt generation
        •
        •               ;   Increment HOUR, MINUTE, SECOND
```

LCD CONTROLLER/DRIVER

The KS57C2408A/2416A microcontroller can directly drive an up-to-12-digit (96-segment) LCD panel. Data written to the LCD display RAM can be transferred to the segment signal pins automatically without program control.

When a subsystem clock is selected as the LCD clock source, the LCD display is enabled even during Stop and Idle modes.

LCD RAM ADDRESS AREA

RAM addresses 1E8H–1FFH are used as LCD data memory. These locations can be addressed by 1-bit or 4-bit instructions. When the bit value of a display segment is "1", the LCD display is turned on; when the bit value is "0", the display is turned off.

Display RAM data are sent out through segment pins SEG0–SEG23 using a direct memory access (DMA) method that is synchronized with the f_{LCD} signal. RAM addresses in this location that are not used for LCD display can be allocated to general-purpose use.

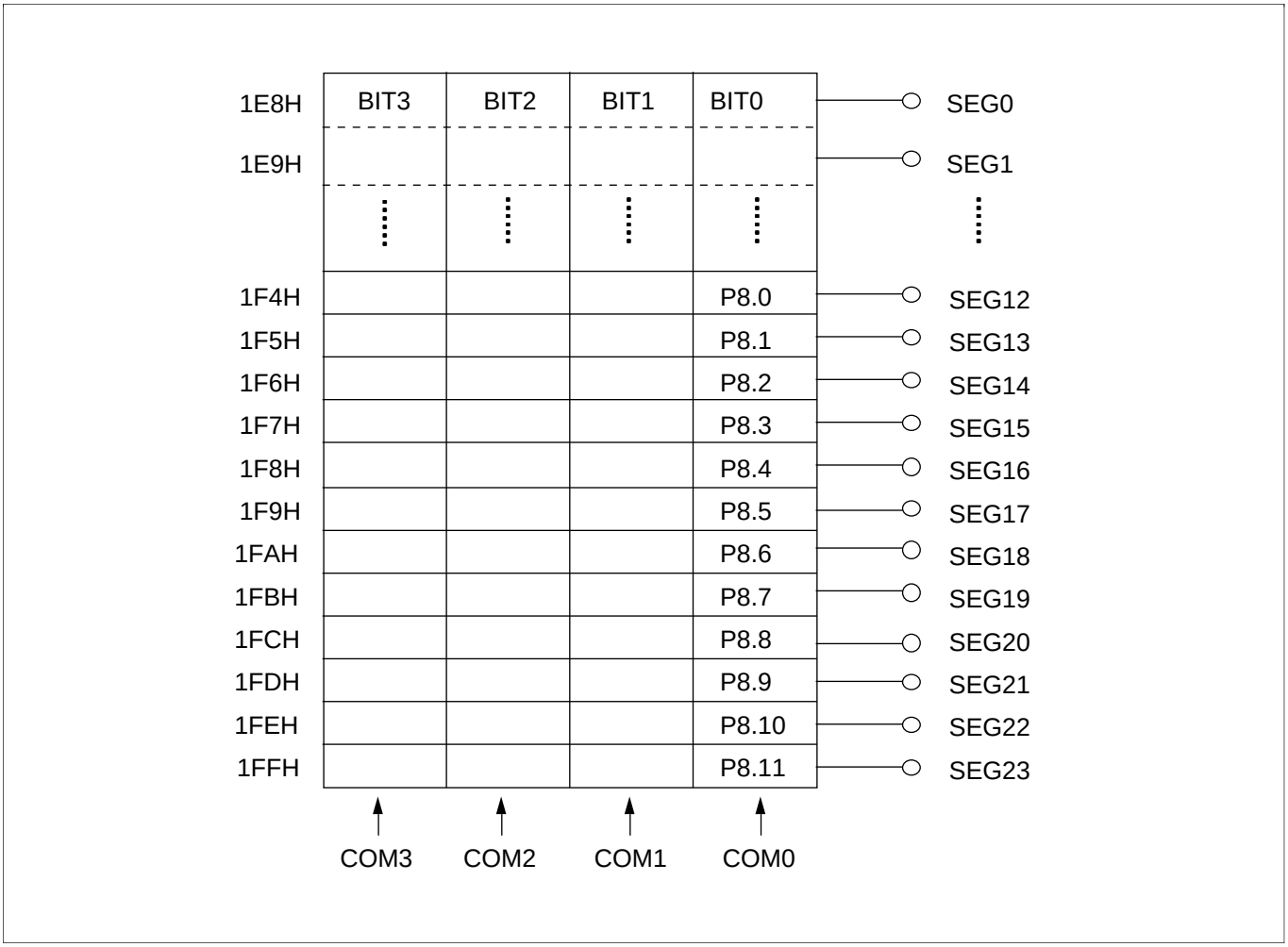


Figure 35. LCD Display Data RAM Organization

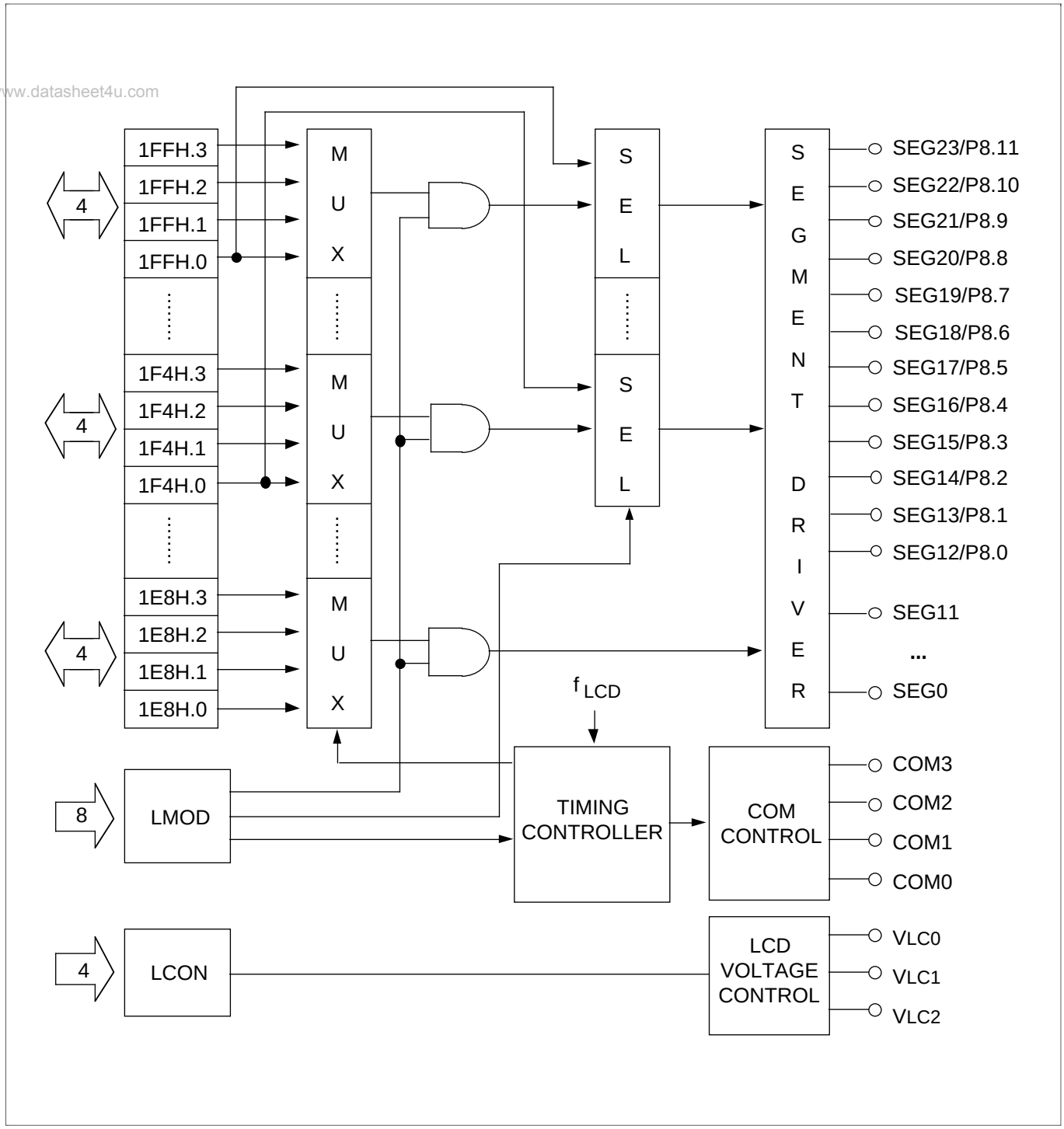


Figure 36. LCD Circuit Diagram

LCD CONTROL REGISTER (LCON)

The LCON register is used to turn the LCD display on and off and to control the flow of current to dividing resistors in the LCD circuit. When LCON.0 is "0", the LCD display is turned off and the current to the dividing resistors is cut off, regardless of the current LMOD.3 value.

Table 27. LCD Control Register (LCON) Organization (4-Bit W)

LCON Bit	Setting	Description
LCON.3	0	This bit is used for internal testing only; always logic zero.
LCON.2	0	Always logic zero.
LCON.1	0	Always logic zero.
LCON.0	0	LCD output low; turn display off, cut off current to dividing resistors, and output port 8 latch contents.
	1	If LMOD.3 = "0": LCD output low; turn display off; output port 8 latch contents; If LMOD.3 = "1": COM and SEG output in display mode; turn display on.

Table 28. Relationship of LCON.0 and LMOD.3 Bit Settings

LCON.0	LMOD.3	COM0-COM3	SEG0-SEG23	P8.0-P8.11
0	x	Output low; LCD display off	Output low; LCD display off	Output latch contents; cut off current to dividing resistors
1	0	Output low; LCD display off	Output low; LCD display off	Output latch contents; LCD display off
	1	COM output corresponds to display mode	SEG output corresponds to display mode	Output latch contents; LCD display on

NOTE: 'x' means 'don't care.'

Table 29. LCD Clock Signal (LCDCK) Frame Frequency

LCDCK Frequency	Static	1/2 Duty	1/3 Duty	1/4 Duty
$fw/2^9$ (64 Hz)	64	32	21	16
$fw/2^8$ (128 Hz)	128	64	43	32
$fw/2^7$ (256 Hz)	256	128	85	64
$fw/2^6$ (512 Hz)	512	256	171	128

NOTES:
1. 'fw' is the watch timer clock frequency of 32.768 kHz.
2. The watch timer clock frequency for LCDCK is shown in parentheses in column one.

LCD MODE REGISTER (LMOD)

The LCD mode register LMOD is used to control LCD controller. Because the LCD clock (LCDCK) is generated by dividing the watch timer clock (fw), the watch timer must be enabled when the LCD display is turned on. The LCD display can continue to operate during Idle and Stop modes if a subsystem clock is used as the watch timer source.

Table 30. LCD Mode Control Register (LMOD) Organization

LMOD.7	LMOD.6	LCD Output Segments and 1-Bit Output Pins
0	0	Segments 12–15, 16–19, and 20–23
0	1	Segments 12–15 and 16–19; 1-bit output at P8.8–P8.11
1	0	Segments 12–15; 1-bit output at P8.4–P8.7 and P8.8–P8.11
1	1	1-bit output only at P8.0–P8.3, P8.4–P8.7, and P8.8–P8.11

LMOD.5	LMOD.4	LCD Clock (LCDCK) Frequency
0	0	32.768 kHz watch timer clock (fw)/2^9 = 64 Hz
0	1	fw/2^8 = 128 Hz
1	0	fw/2^7 = 256 Hz
1	1	fw/2^6 = 512 Hz

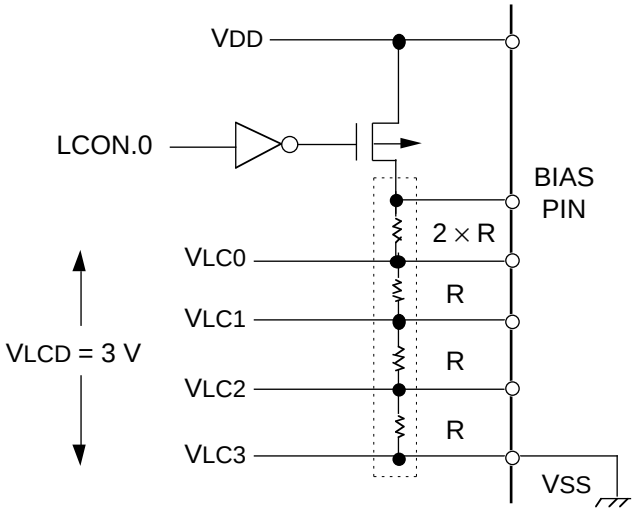
LMOD.3	LMOD.2	LMOD.1	LMOD.0	Duty and Bias Selection for LCD Display
0	x	x	x	LCD display off
1	0	0	0	1/4 duty, 1/3 bias
1	0	0	1	1/3 duty, 1/3 bias
1	0	1	0	1/2 duty, 1/2 bias
1	0	1	1	1/3 duty, 1/2 bias
1	1	0	0	Static

NOTE: 'x' means 'don't care.'

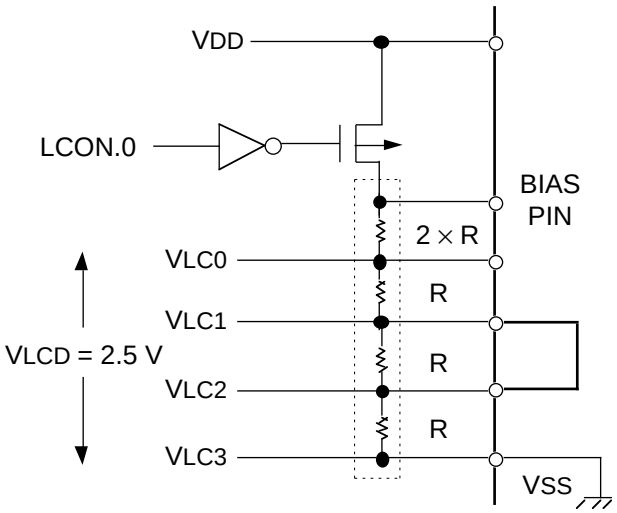
Table 31. Maximum Number of Display Digits Per Duty Cycle

LCD Duty	LCD Bias	COM Output Pins	Maximum Digit Display (× 8 Segment Pins)
Static	Static	COM0	3
1/2	1/2	COM0–COM1	6
1/3	1/2	COM0–COM2	9
1/3	1/3	COM0–COM2	9
1/4	1/3	COM0–COM3	12

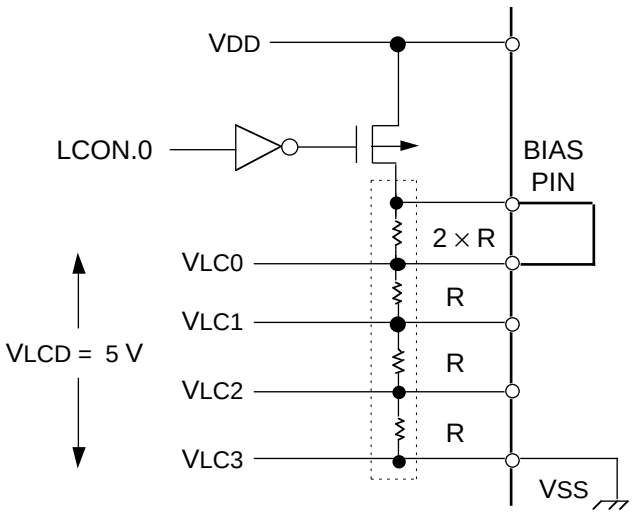
Static and 1/3 Bias (VLCD = 3 V at VDD = 5 V)



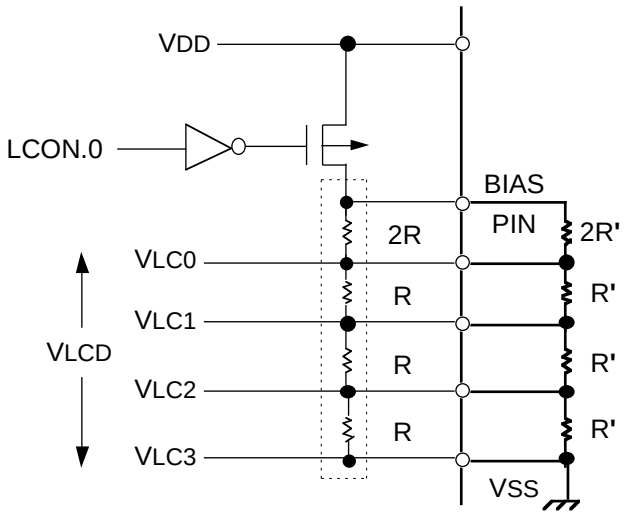
1/2 Bias (VLCD = 2.5 V at VDD = 5V)



Static and 1/3 Bias (VLCD = 5 V at VDD = 5V)



Voltage Dividing Resistor Adjustment



R = Optional voltage dividing resistor
R' = External resistor

Figure 37. Voltage Dividing Resistor Circuit Diagrams

LCD DRIVE VOLTAGE

The LCD display is turned on only when the voltage difference between the common and segment signals is greater than V_{LCD}. The LCD display is turned off when the difference between the common and segment signal voltages is less than V_{LCD}.

NOTE

The LCD panel display may deteriorate if a DC voltage is applied that lies between the common and segment signal voltage. Therefore, always drive the LCD panel with AC voltage.

LCD VOLTAGE DIVIDING RESISTORS

On-chip voltage dividing resistors for the LCD circuit can be configured by mask option selection. Using these optional internal voltage dividing resistors, you can drive either a 3-volt or a 5-volt LCD display using external biasing. Bias pins are connected externally to the V_{LCD} pin so that it can handle the different LCD drive voltages. To cut off the current supply to the voltage dividing resistors, clear LCON.0 when you turn the LCD display off.

COMMON (COM) SIGNALS

The common signal output pin selection (COM pin selection) varies according to the selected duty cycle.

Table 32. Common Signal Pins Used Per Duty Cycle

Display Mode	COM0 Pin	COM1 Pin	COM2 Pin	COM3 Pin
Static	Selected	N/C	N/C	N/C
1/2 duty	Selected	Selected	N/C	N/C
1/3 duty	Selected	Selected	Selected	N/C
1/4 duty	Selected	Selected	Selected	Selected

NOTE: 'NC' means that no connection is required.

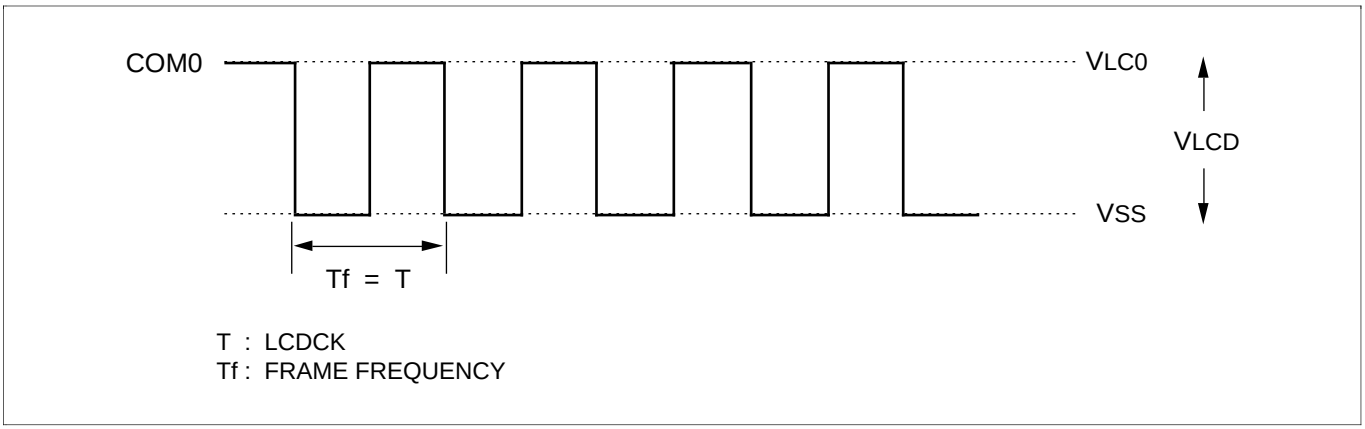


Figure 38. LCD Common Signal Waveform (Static)

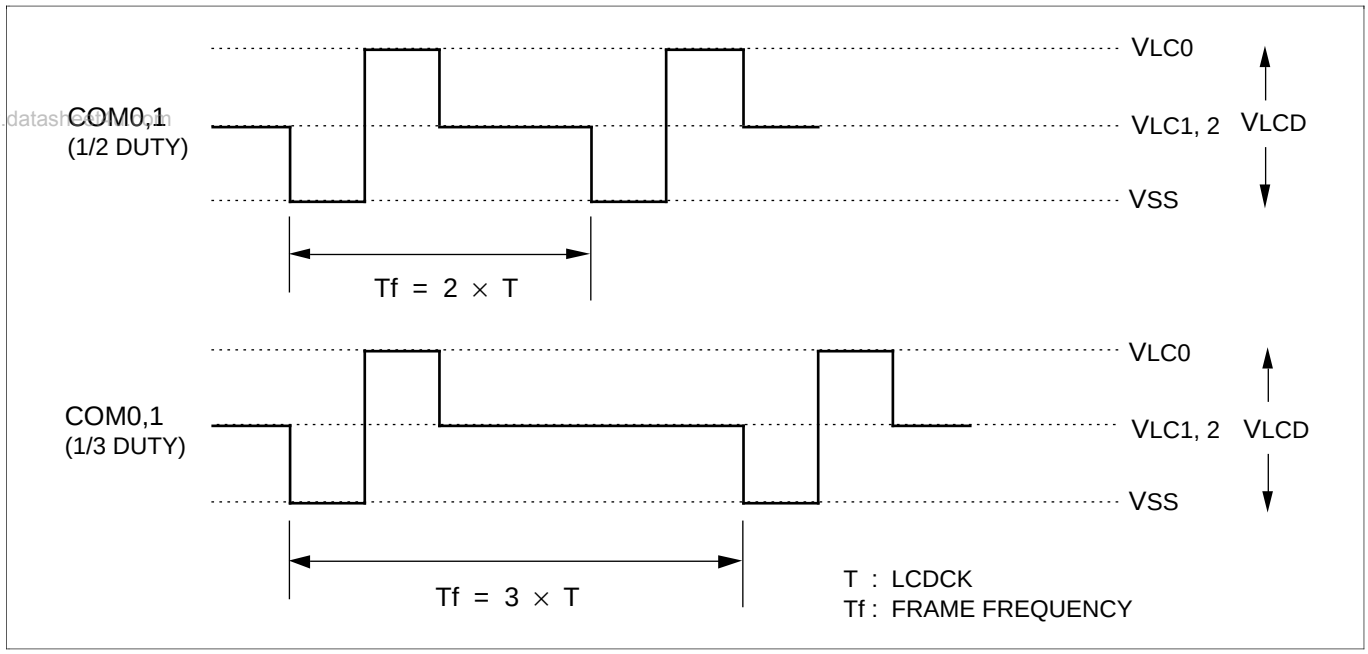


Figure 39. LCD Common Signal Waveforms at 1/2 Bias (1/2, 1/3 Duty)

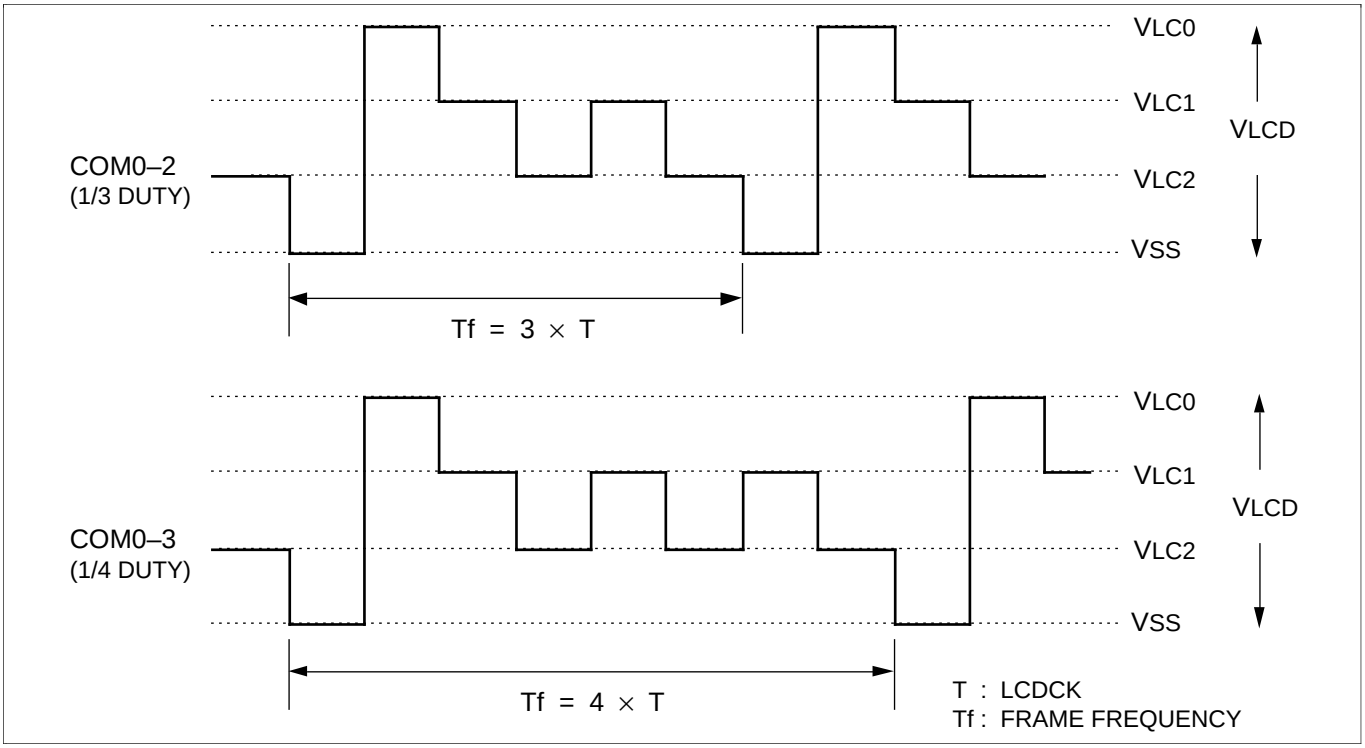


Figure 40. LCD Common Signal Waveforms at 1/3 Bias (1/3, 1/4 Duty)

SEGMENT (SEG) SIGNALS

The 24 LCD segment signal pins are connected to corresponding display RAM locations at 1E8H–1FFH. Bits 0–3 of the display RAM are synchronized with the common signal output pins COM0, COM1, COM2, and COM3.

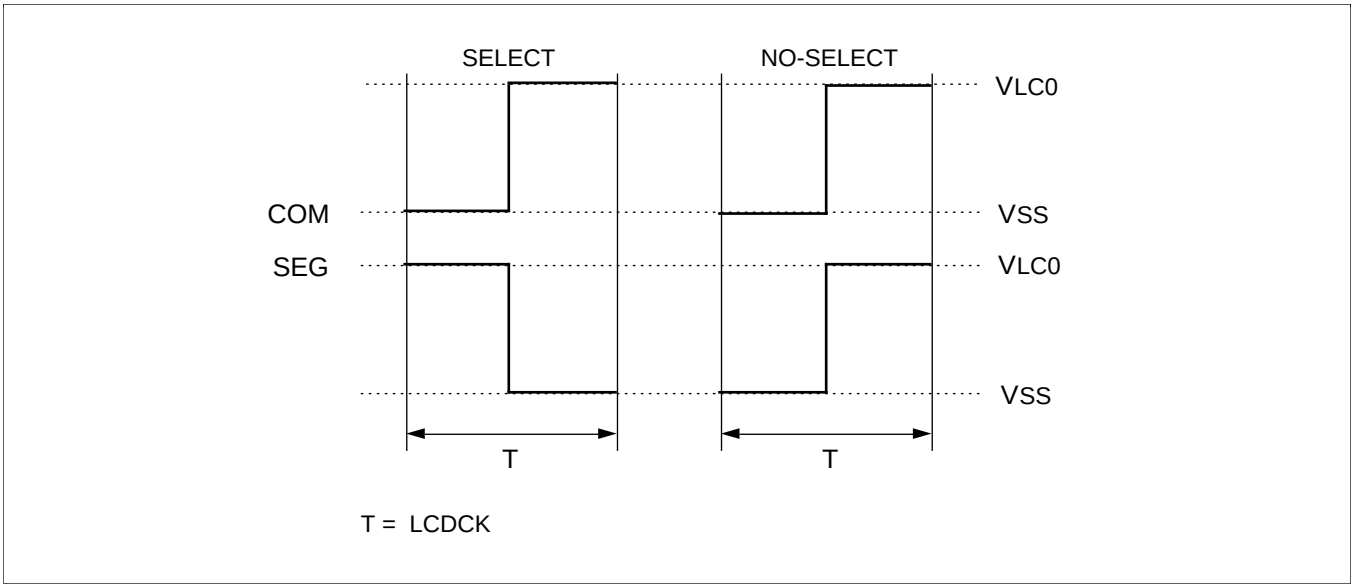


Figure 41. Select/No-Select Bias Signals in Static Display Mode

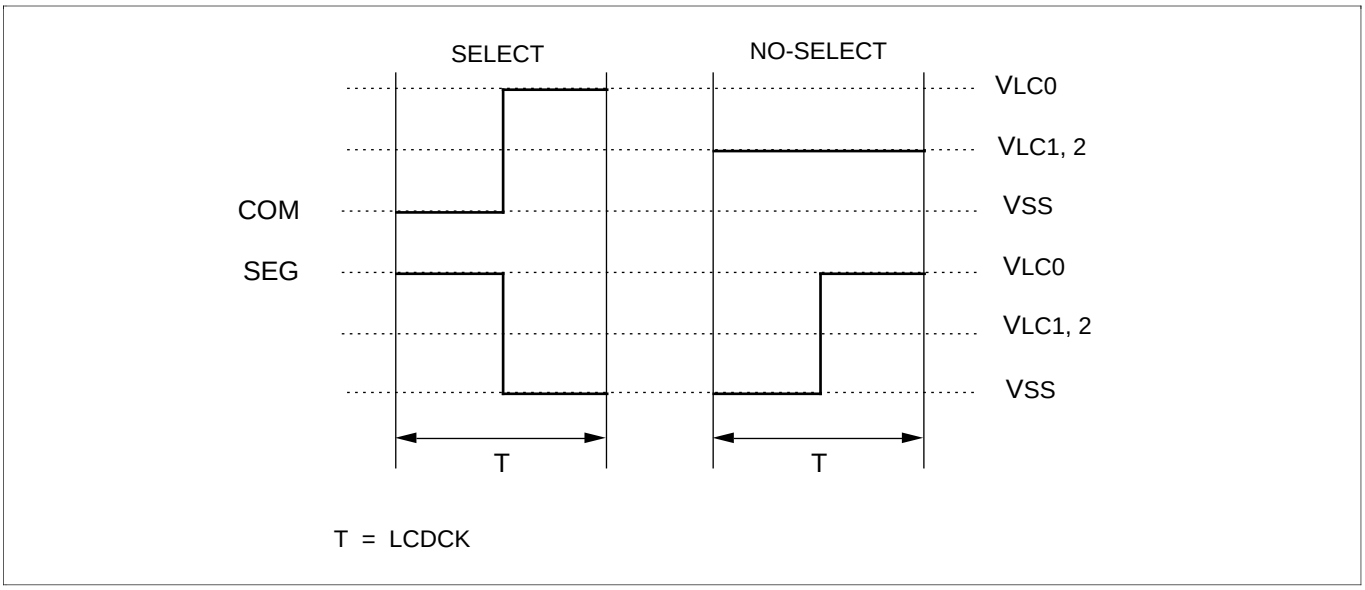


Figure 42. Select/No-Select Bias Signals in 1/2 Bias Display Mode

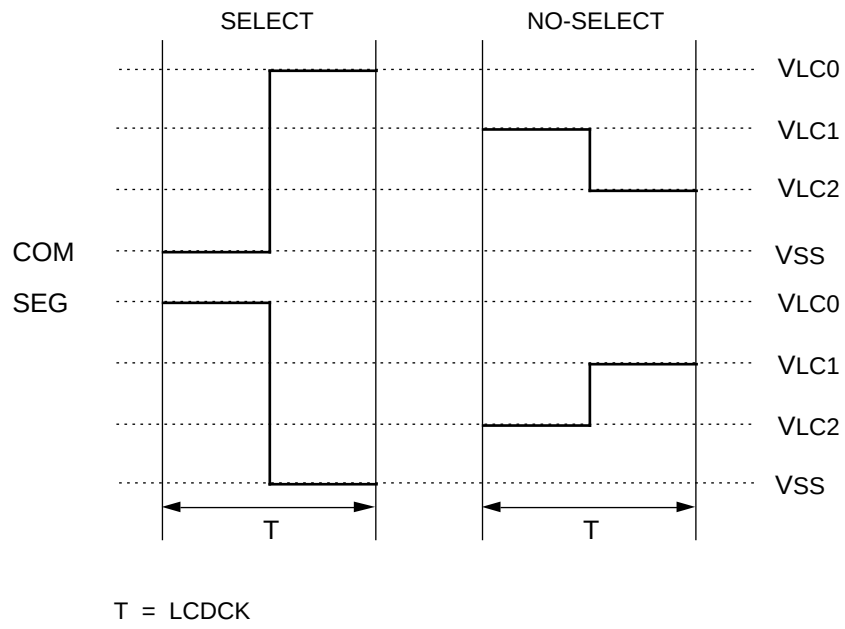


Figure 43. Select/No-Select Signals in 1/3 Bias Display Mode

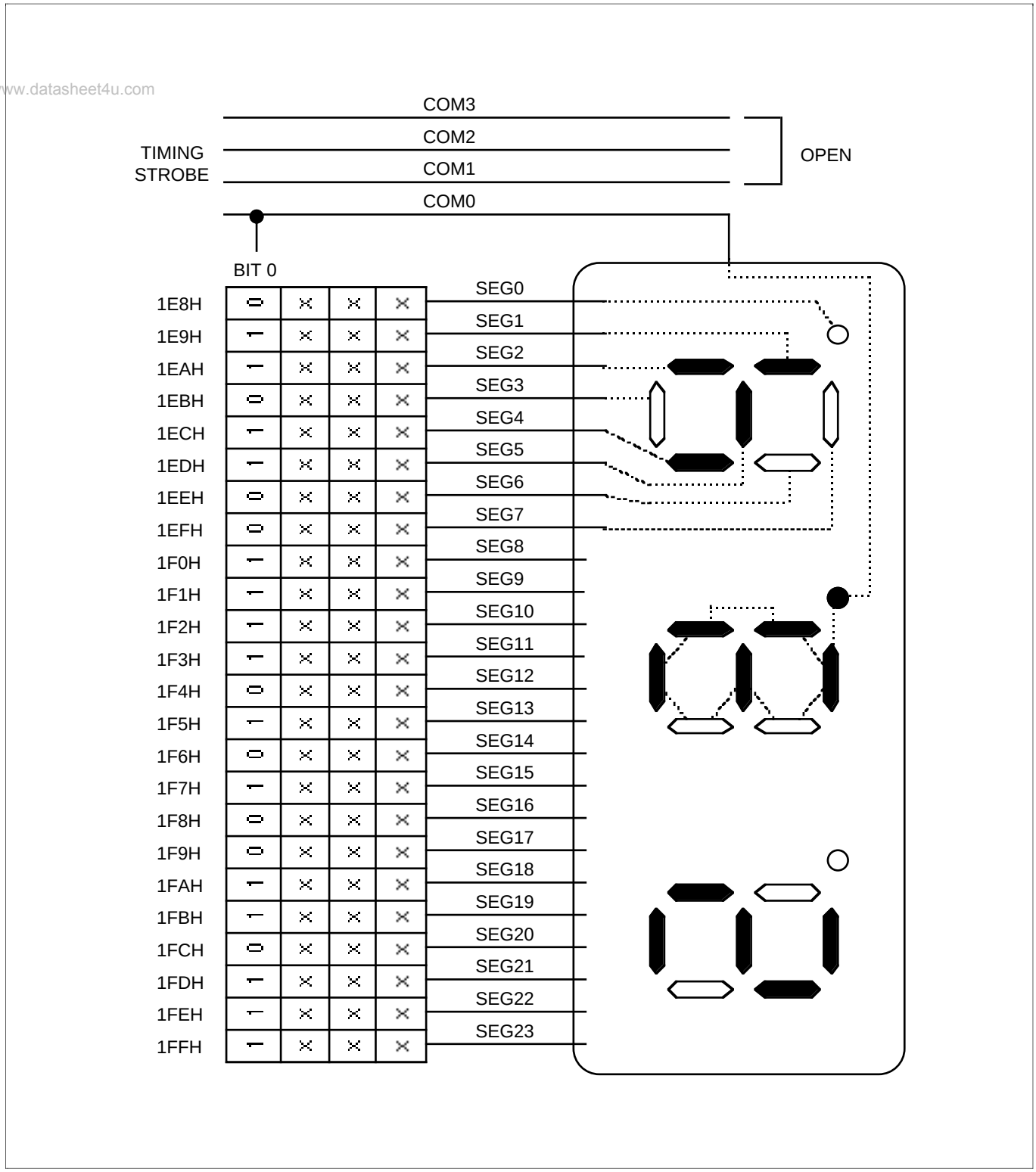


Figure 44. LCD Connection Example (Static)

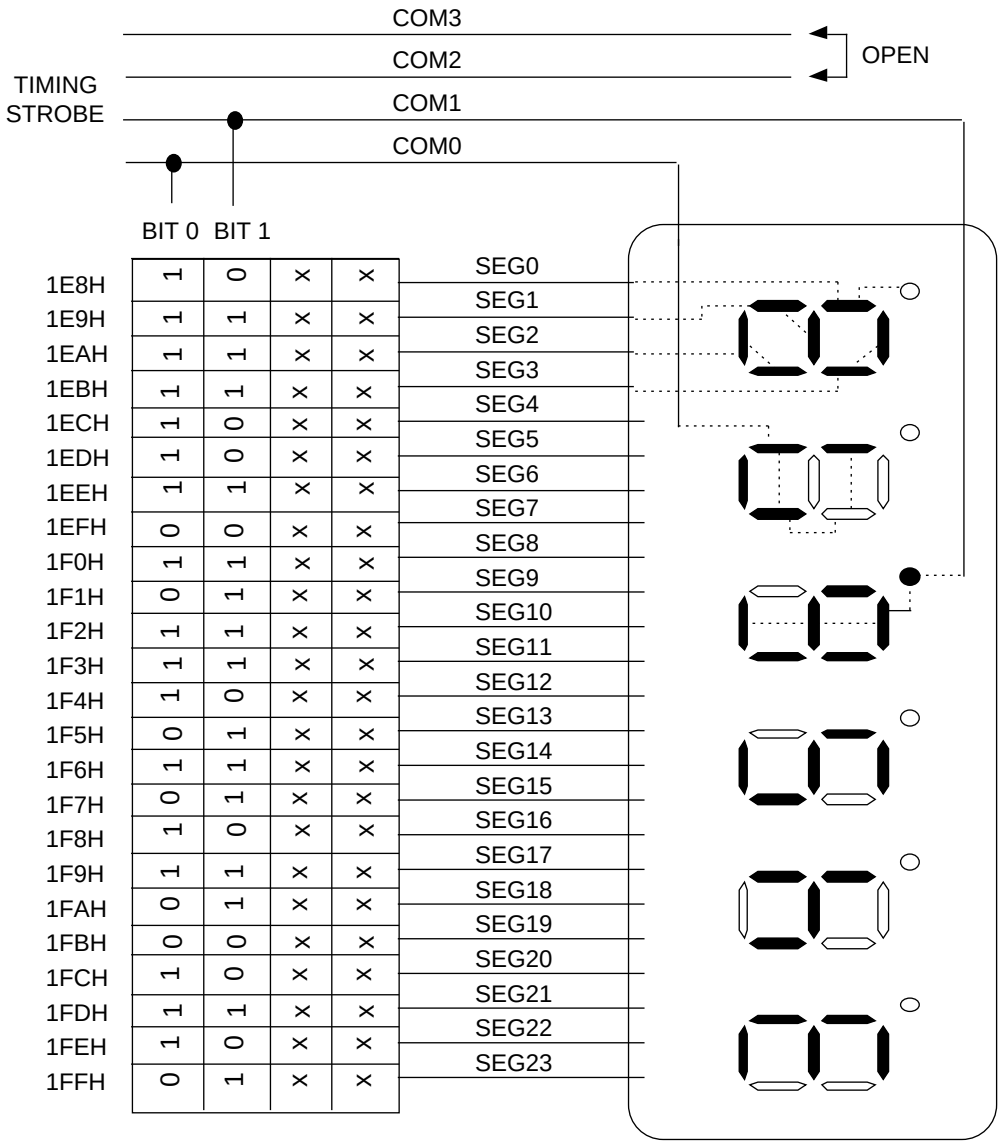


Figure 45. LCD Connection Example (1/2 Duty, 1/2 Bias)

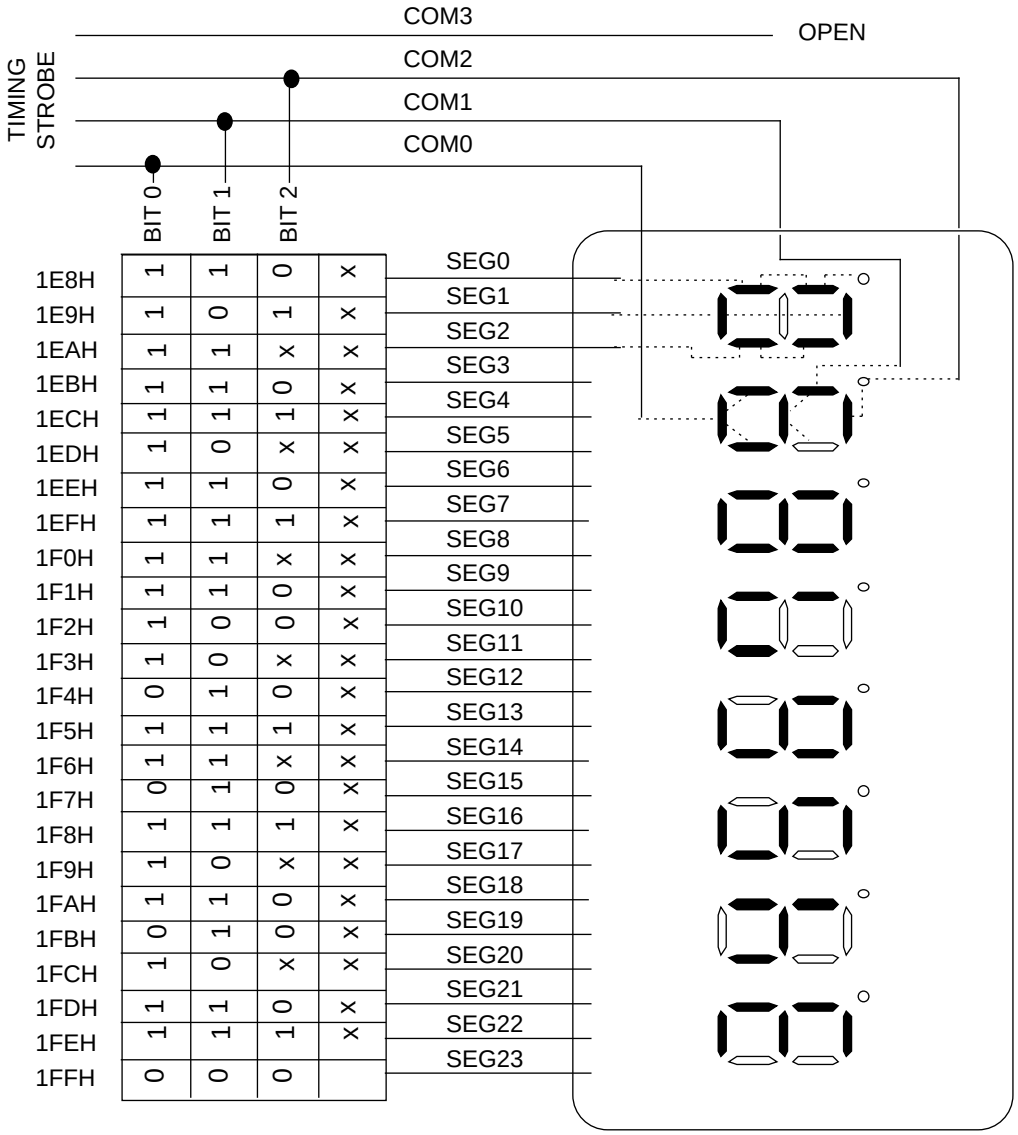


Figure 46. LCD Connection Example (1/3 Duty, 1/3 Bias)

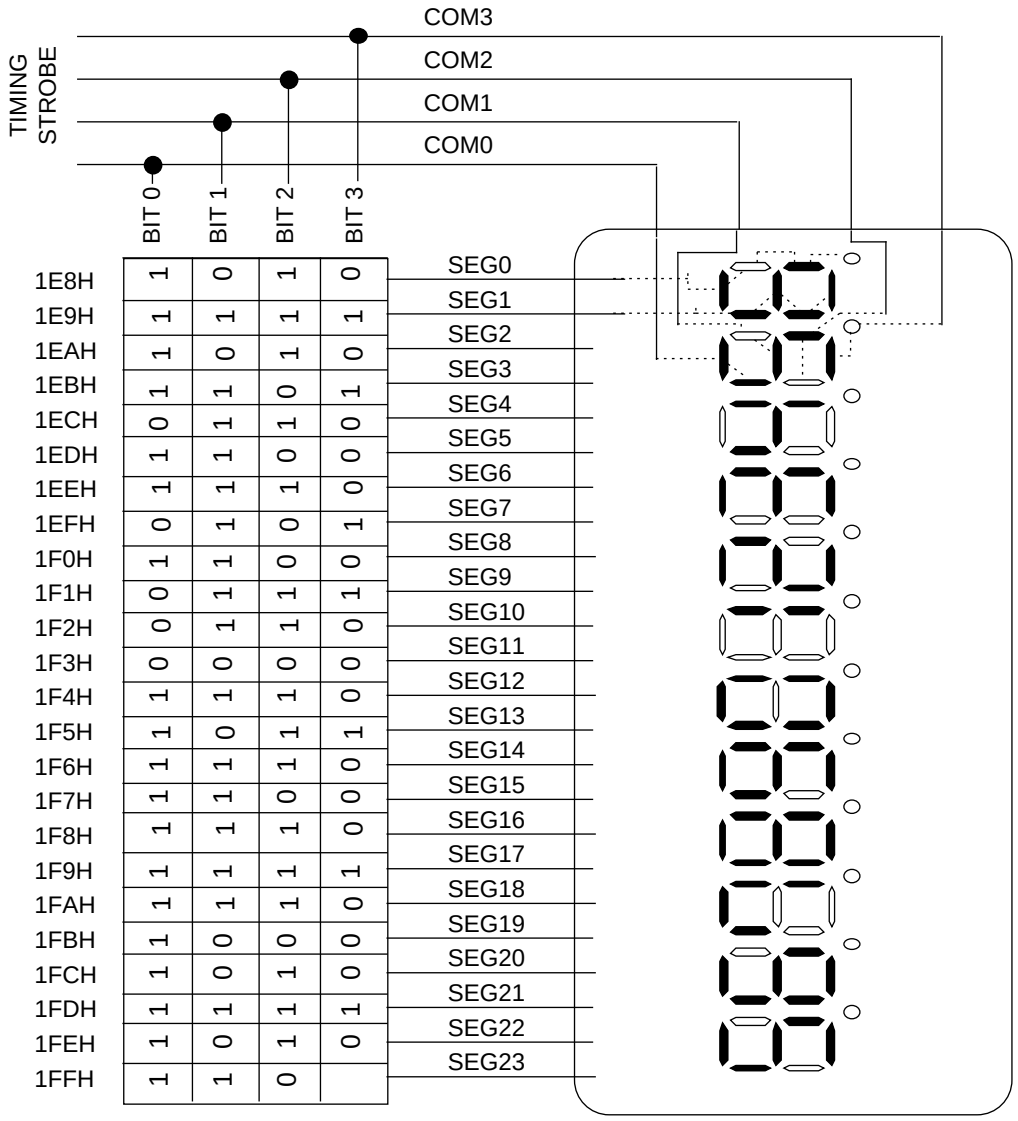


Figure 47. LCD Connection Example (1/4 Duty, 1/3 Bias)

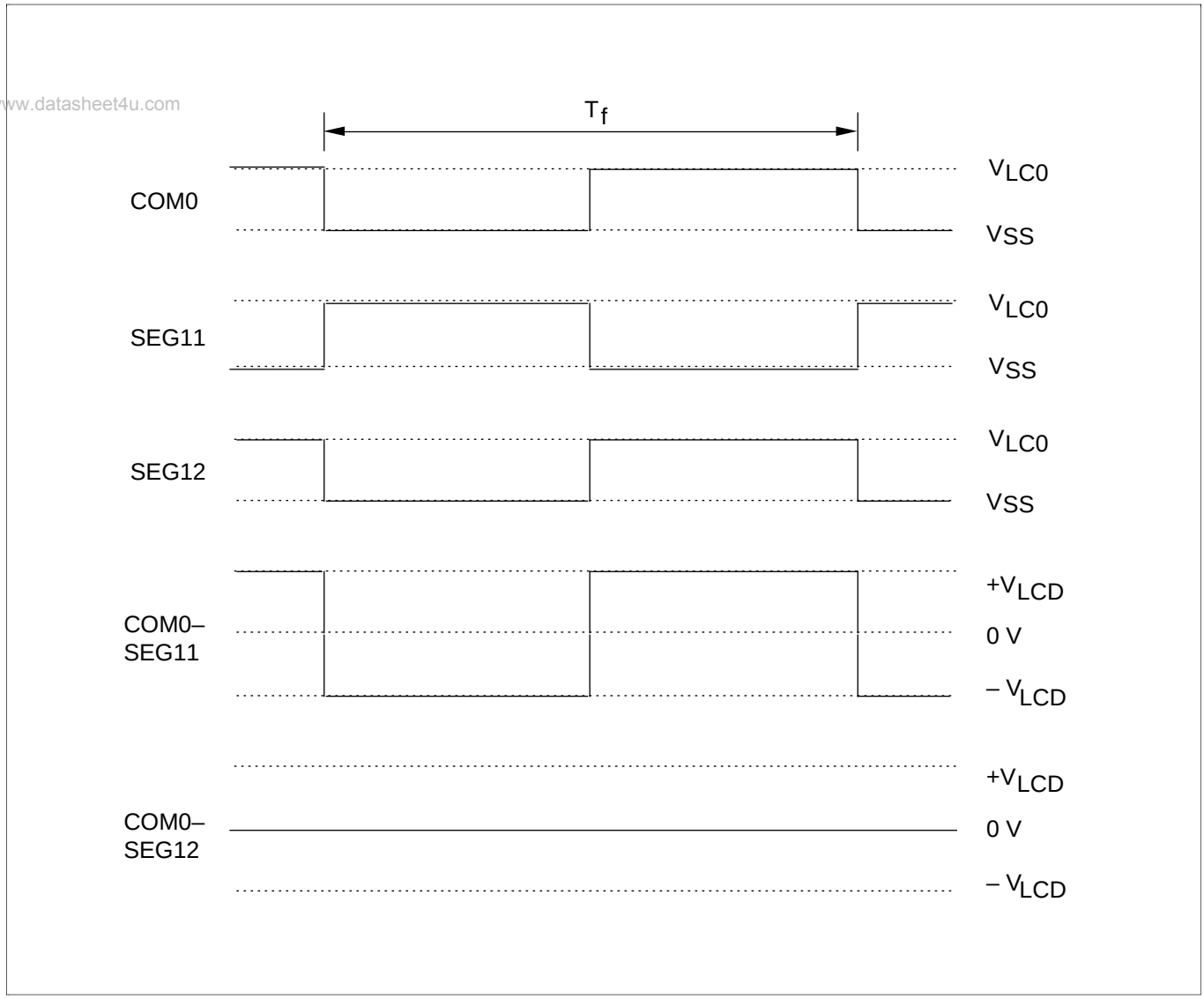


Figure 48. LCD Signal Waveforms in Static Mode

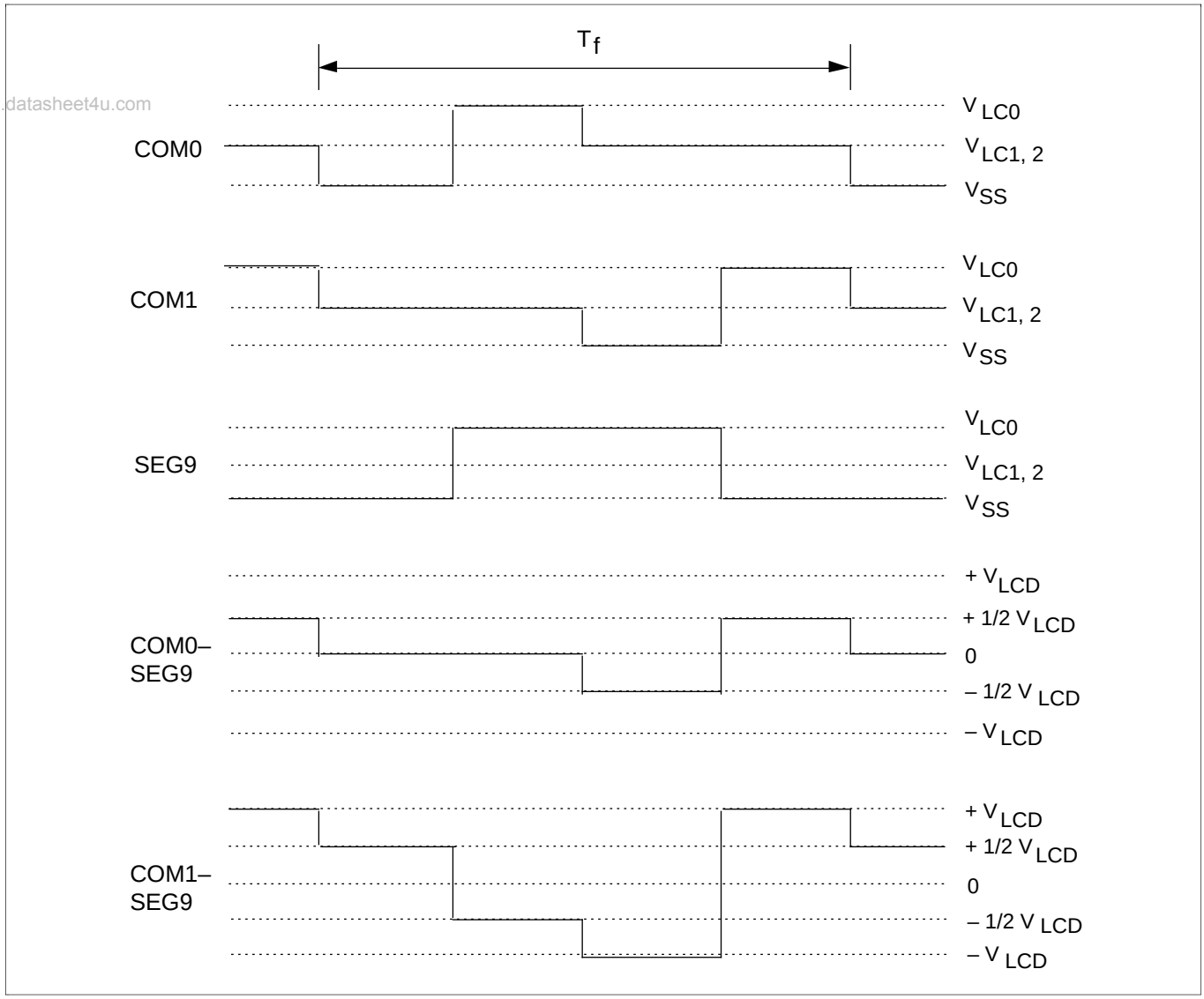


Figure 49. LCD Signal Waveforms at 1/2 Duty, 1/2 Bias

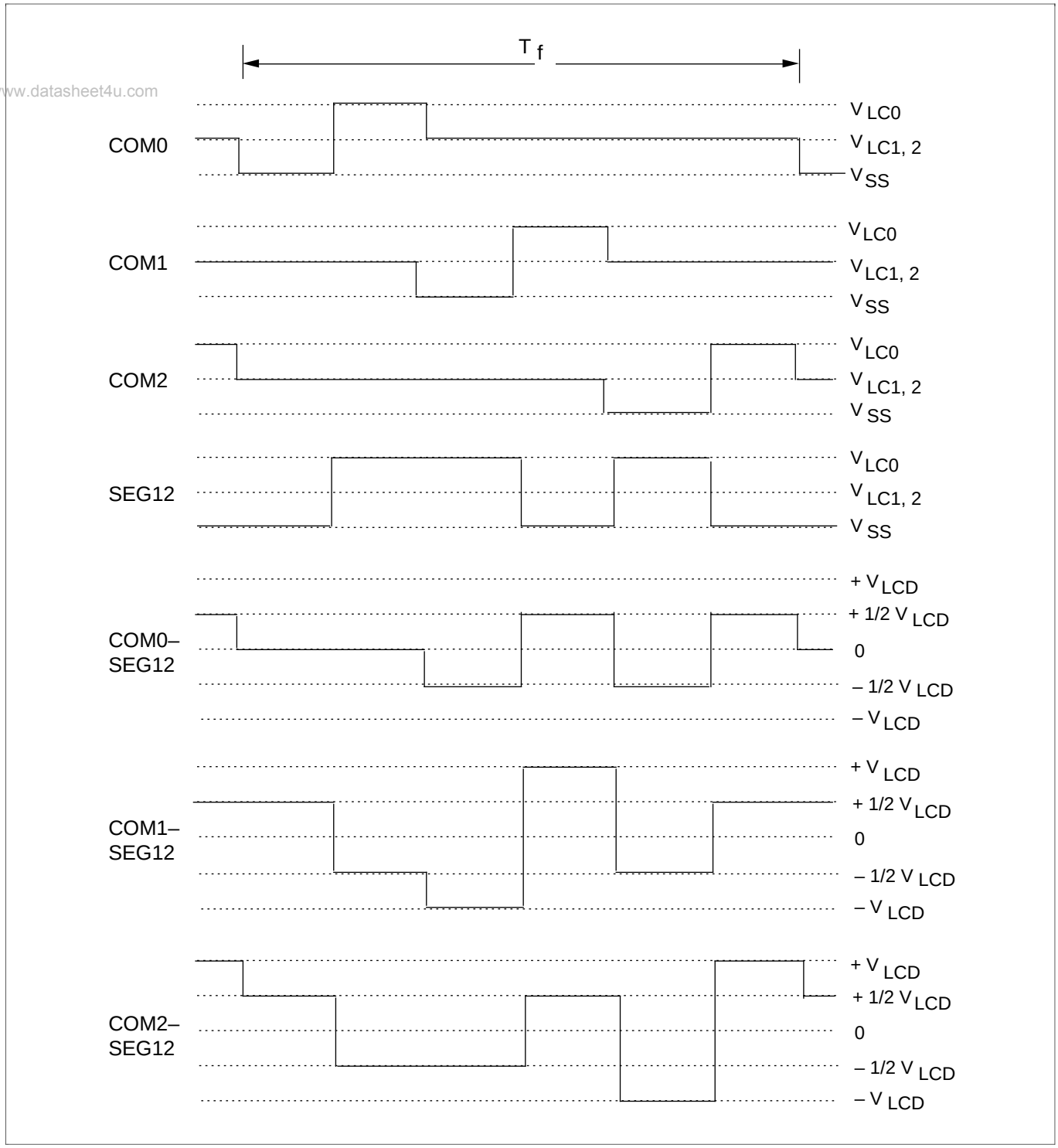


Figure 50. LCD Signal Waveforms at 1/3 Duty, 1/2 Bias

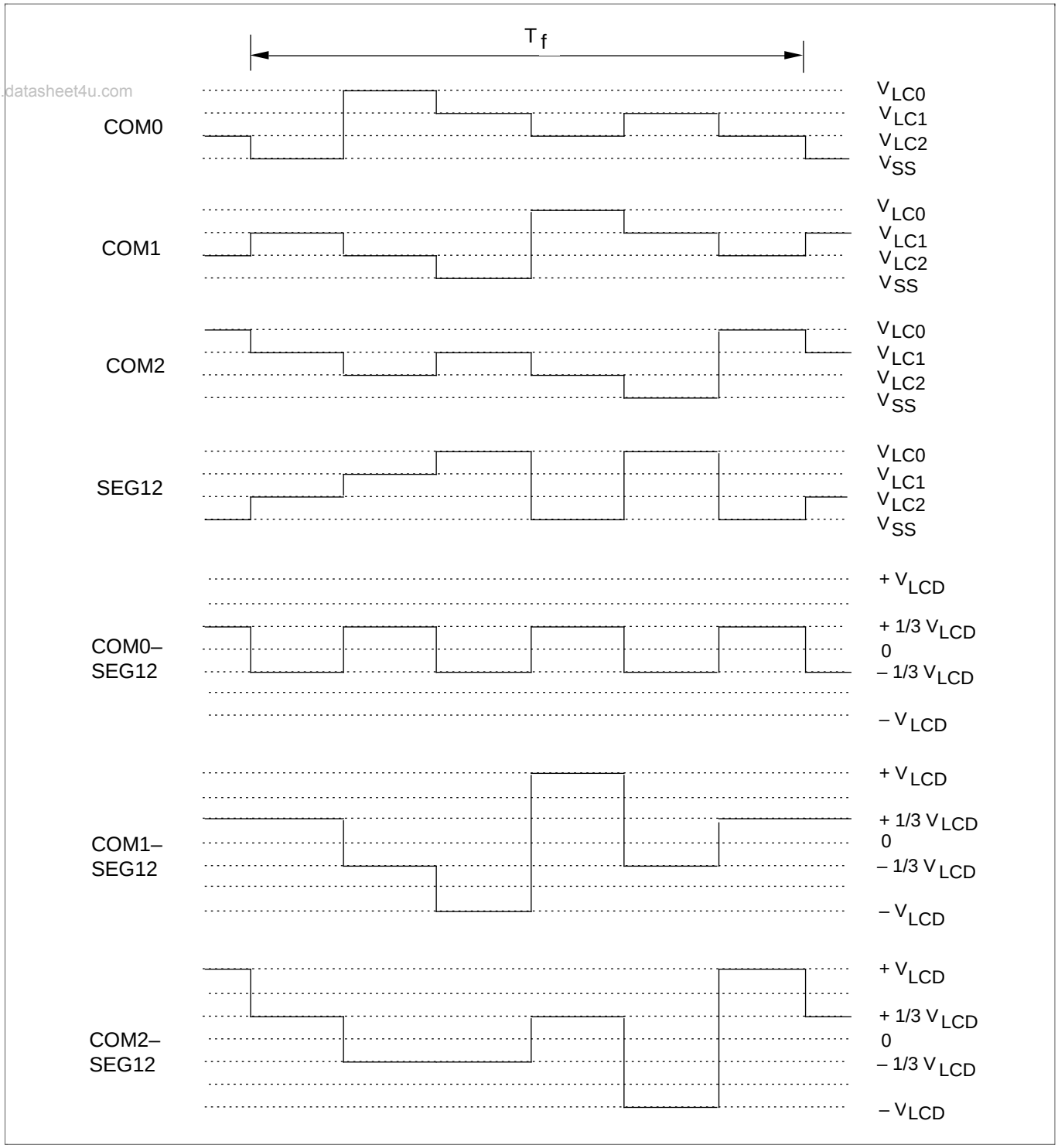


Figure 51. LCD Signal Waveforms at 1/3 Duty, 1/3 Bias

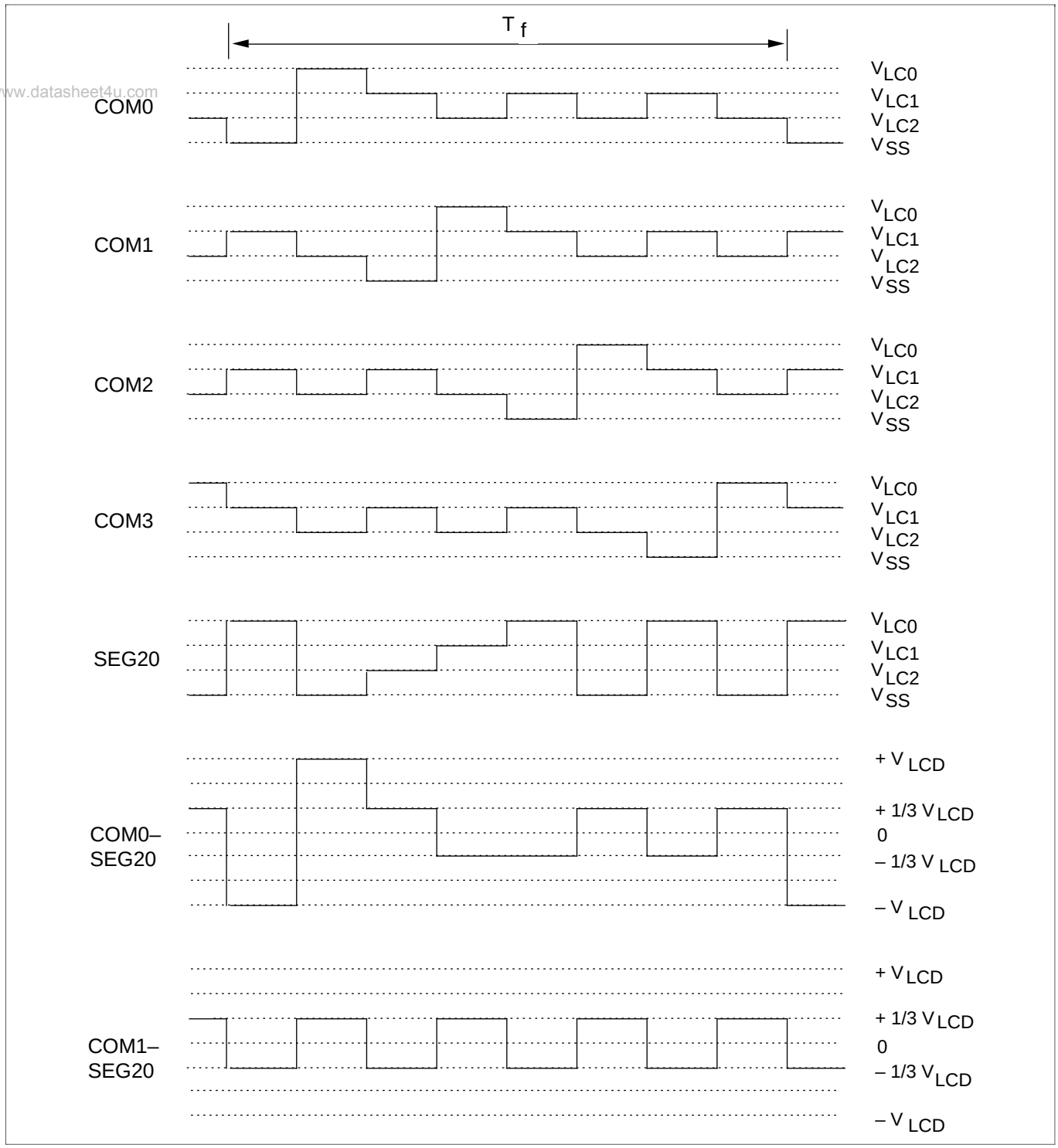
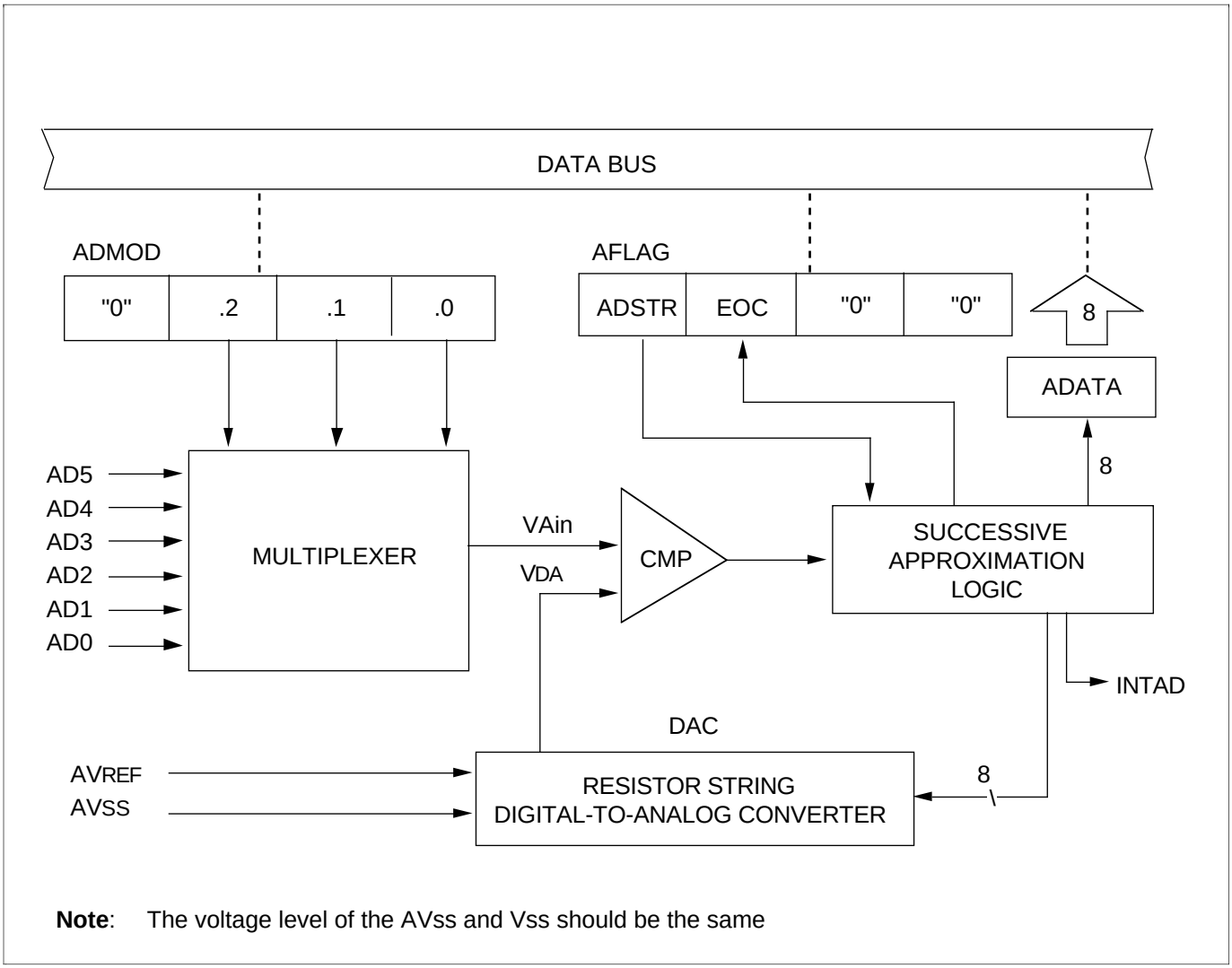


Figure 52. LCD Signal Waveforms at 1/4 Duty, 1/3 Bias

A/D CONVERTER

To operate the A/D converter, one of the six analog input channels is selected by writing the appropriate value to the A/D mode register, ADMOD.

To start the converter, the ADSTR flag in the control register AFLAG must be set to "1". Conversion speed is determined by the oscillator frequency and the CPU clock. When the A/D operation is complete, the EOC flag must be tested in order to verify that the conversion was successful. When the EOC value is "0", an interrupt request (INTAD) is issued. Then, when the interrupt request has been enabled, the converted digital values stored in the data register ADATA can be read.



Note: The voltage level of the AVss and Vss should be the same

Figure 53. A/D Converter Circuit Diagram

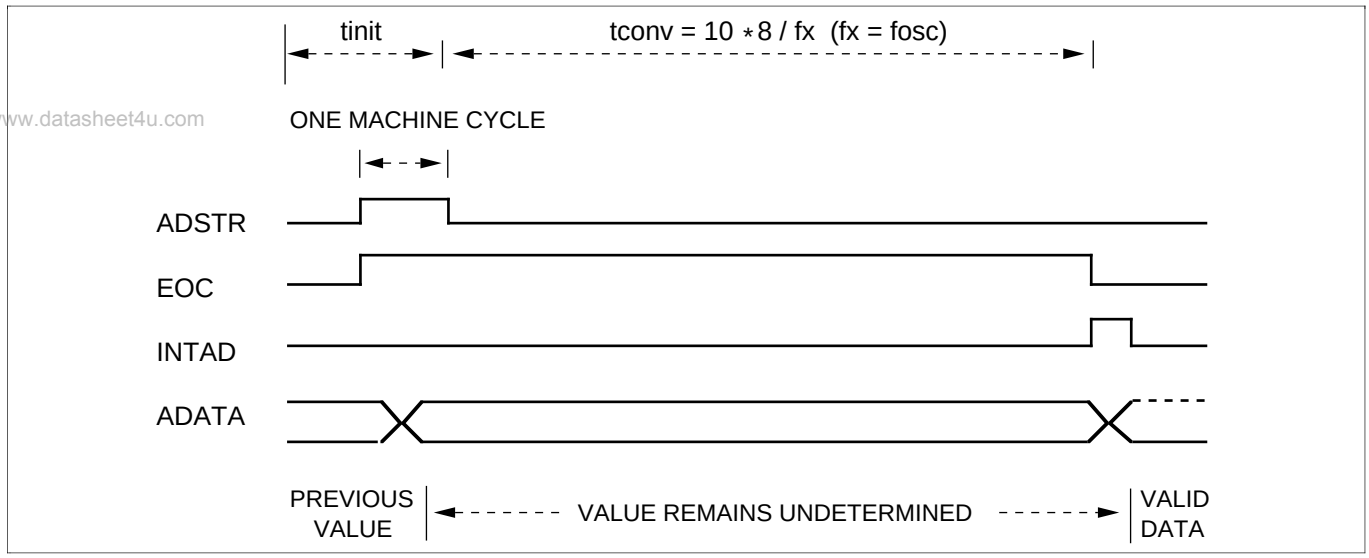


Figure 54. A/D Converter Timing Diagram

ADC DIGITAL-TO-ANALOG CONVERTER (DAC)

The 8-bit digital-to-analog converter (DAC) generates analog voltage reference values for the comparator. The DAC is a 256-step resistor string type digital-to-analog converter that uses successive approximation logic to convert digital input into the reference analog voltage, V_{DA}. The V_{DA} values are input from the DAC to the comparator where they are compared to the multiplexed external analog source voltage, VA_{in}. Since the DAC has 8-bit resolution, it generates the 256-step analog reference voltage.

ADC DATA REGISTER (ADATA)

The A/D converter data register, ADATA, is an 8-bit register in which digital data values are stored as an A/D conversion operation is completed. Digital values stored in ADATA are retained until another conversion operation is initiated. ADATA is addressable by 8-bit read instructions only.

ADC MODE REGISTER (ADMOD)

The analog-to-digital converter mode register ADMOD is used to select one of six analog channels as the analog data input source. Input channels AD0–AD5 (corresponding to I/O pins P9.0–P9.3 and P10.0–10.1) may be used either for analog input to the A/D converter, or as normal input ports.

Because only one of the six ports can be selected at one time as external source of analog data, the five remaining input ports are always available for other inputs. Bit 3 in the ADMOD register is always 0.

Table 33. A/D Converter Mode Register Settings (1, 4-Bit R/W)

ADMOD.2	ADMOD.1	ADMOD.0	Effect of ADMOD Bit Setting
0	0	0	Select input channel AD0 (pin P9.0)
0	0	1	Select input channel AD1 (pin P9.1)
0	1	0	Select input channel AD2 (pin P9.2)
0	1	1	Select input channel AD3 (pin P9.3)
1	0	0	Select input channel AD4 (pin P10.0)
1	0	1	Select input channel AD5 (pin P10.1)

ADC CONTROL REGISTER (AFLAG)

The A/D converter control register, AFLAG, contains the control flags used to start the A/D converter and to monitor its operational status.

FDBH

ADSTR	EOC	"0"	"0"

The ADSTR bit (bit 3) is the enable/disable flag for the A/D converter (ADSTR = A/D start). ADSTR is write-only and is 1-bit and 4-bit addressable.

The EOC bit (End Of Conversion) is a flag that can be read to determine the current status of an A/D conversion operation. EOC is 1-bit or 4-bit read-only addressable.

☞ PROGRAMMING TIP — Configuring A/D Converter Input Pins

In this A/D converter program sample, the AD0, AD1 and AD2 pins are used as A/D input pins and the P9.3 / AD3, P10.0 / AD4, and P10.1 / AD5 pins are used as normal input pins:

```
        BITR    EMB
        BITR    IEAD        ;   Disable INTAD interrupt
        DI                  ;   Disable all interrupts during A/D conversion
        LD      A,#0H
        LD      ADMOD,A     ;   AD0 pin select for A/D conversion
        BITS    ADSTR       ;   A/D conversion start
AD0CK   BTSF    EOC         ;   A/D conversion end check
        JR      AD0CK       ;   A/D conversion not completed
        LD      EA,ADATA    ;   A/D conversion end
        LD      AD0BUF,EA   ;   AD0BUF ← AD0 conversion data
        LD      A,#1H
        LD      ADMOD,A     ;   AD1 pin select for A/D conversion
        BITS    ADSTR       ;   A/D conversion start
AD1CK   BTSF    EOC         ;   A/D conversion end check
        JR      AD1CK       ;   A/D conversion not completed
        LD      EA,ADATA    ;   AD conversion end
        LD      AD1BUF,EA   ;   AD1BUF ← AD1 conversion data
        LD      A,#2H
        LD      ADMOD,A     ;   AD2 pin select for A/D conversion
        BITS    ADSTR       ;   AD conversion start
AD2CK   BTSF    EOC         ;   AD conversion end check
        JR      AD2CK       ;   AD conversion not completed
        LD      EA,ADATA    ;   AD conversion end
        LD      AD2BUF,EA   ;   AD2BUF ← AD2 conversion data
        EI                  ;   Interrupt enable
        BITS    EMB
        BTST    P9.3        ;   P9.3 / AD3 pin check
        JPS     AAA
        BTST    P10.0       ;   P10.0 / AD4 pin check
        JPS     BBB
        BTST    P10.1       ;   P10.0 / AD5 pin check
        JPS     CCC
```

RECOMMENDATION FOR A/D CONVERTER APPLICATION

The input voltage level at the AD0 - AD5 input pins must be greater than V_{SS} and less than V_{DD}. Although V_{IN} does satisfy the absolute maximum voltage requirement, conversion data may be undefined if the $V_{SS} < V_{IN} < V_{DD}$ condition is not met.

To ensure the accuracy of A/D conversion data, noise entering at the A/D input pins must be eliminated. Figure 49 shows the recommended circuit configuration.

On the figure, values of capacitors and resistors are as follows. In addition to, R1 is variable to control the

offset value.

NOTE: C1 = 10 μF, C2 = 100 to 1000 pF, C3 = 100 to 1000 pF, R1 = 50 to 100 Ω, R2 = 1K Ω.

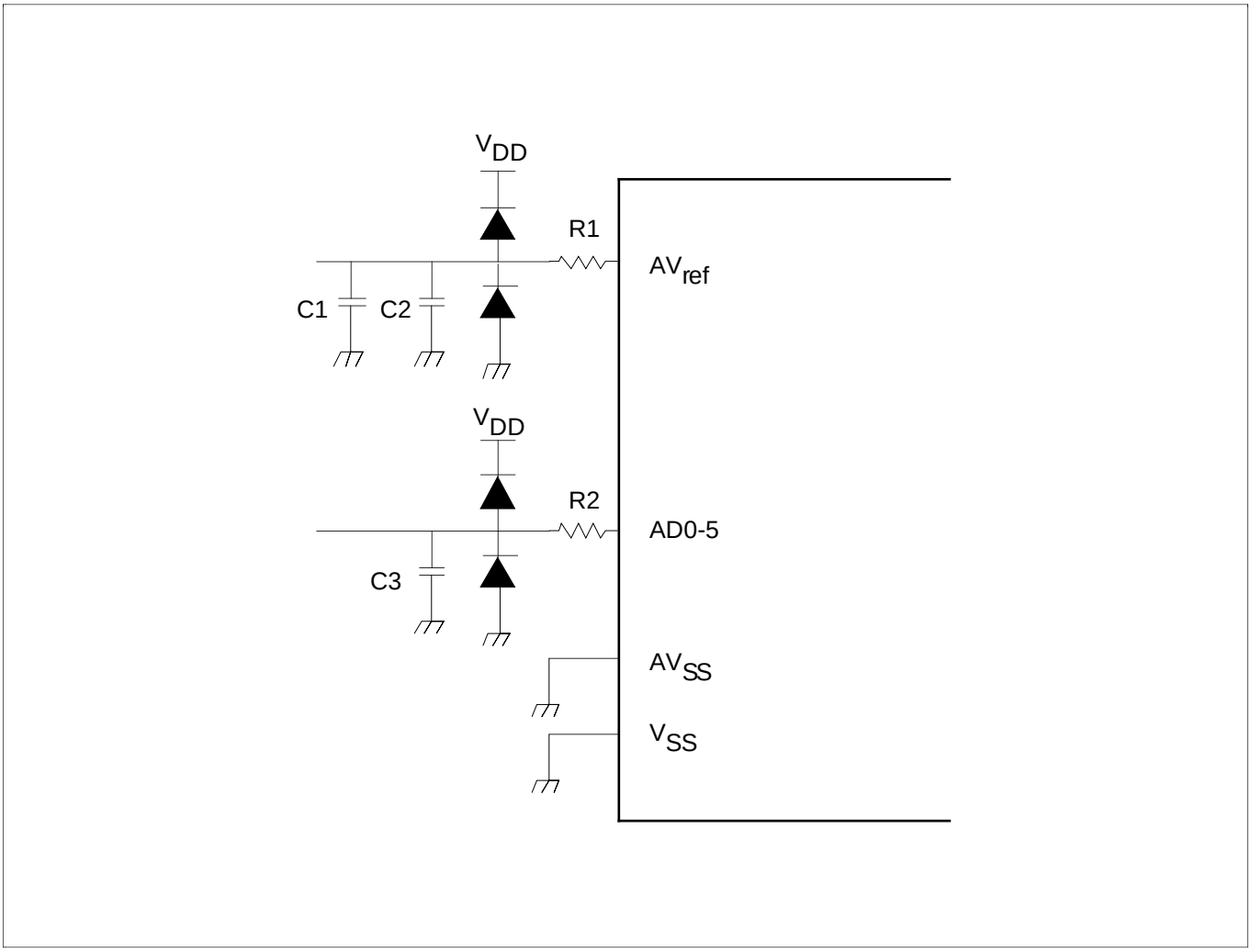


Figure 55. Recommendation for A/D Converter

SERIAL I/O INTERFACE

Using the serial I/O interface, you can exchange 8-bit data with an external device. The serial interface can run off an internal or an external clock source, or the TOL0 signal that is generated by the 8-bit timer/counter 0, TC0. If you use the TOL0 clock signal, you can modify its frequency to adjust the serial data transmission rate.

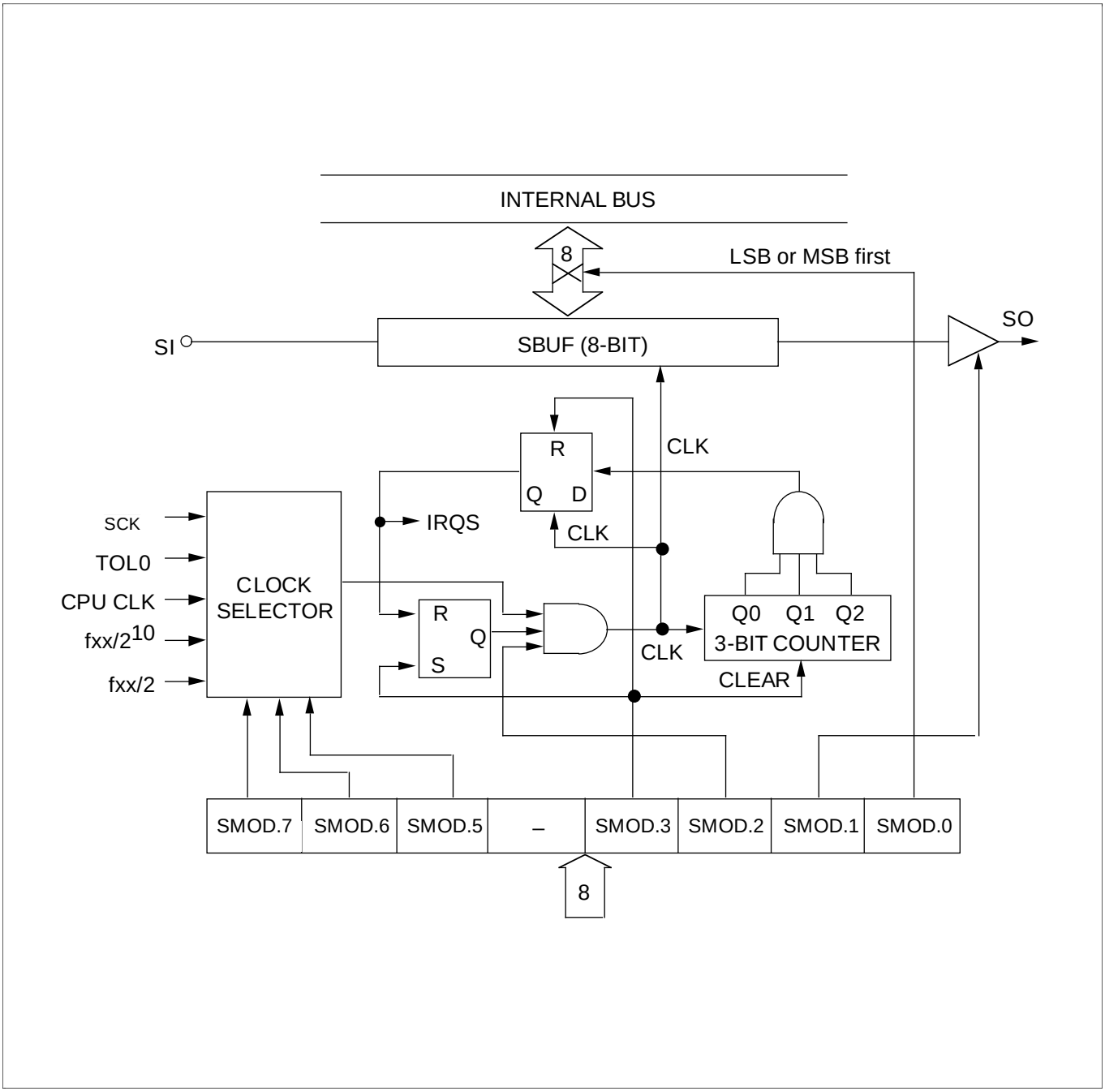


Figure 56. Serial I/O Interface Circuit Diagram

SERIAL I/O MODE REGISTER (SMOD)

The serial I/O mode register (SMOD) specifies the operation mode of the serial interface. SMOD register settings enable you to select either MSB-first or LSB-first serial transmission, and to operate in transmit-and-receive mode or receive-only mode.

When SMOD.3 is set to "1", the contents of the serial interface interrupt request flag, IRQS, and the 3-bit serial clock counter are cleared, and SIO operations are initiated. When the SIO transmission starts, SMOD.3 is cleared to "0".

SERIAL I/O BUFFER REGISTER (SBUF)

When the serial interface operates in transmit-and-receive mode (SMOD.1 = "1"), transmit data in the SIO buffer register are output to the SO pin at the rate of one bit for each falling edge of the SIO clock. Receive data is simultaneously input from the SI pin to SBUF at the rate of one bit for each rising edge of the SIO clock.

When receive-only mode is used, incoming data is input to the SIO buffer at the rate of one bit for each rising edge of the SIO clock. SBUF can be read or written using 8-bit RAM control instructions.

Table 34. SIO Mode Register (SMOD) Organization

SMOD.0	0	Most significant bit (MSB) is transmitted first
	1	Least significant bit (LSB) is transmitted first
SMOD.1	0	Receive-only mode
	1	Transmit-and-receive mode
SMOD.2	0	Disable the data shifter and clock counter; retain contents of IRQS flag when serial transmission is halted
	1	Enable the data shifter and clock counter; set IRQS flag to "1" when serial transmission is halted
SMOD.3	1	Clear IRQS flag and 3-bit clock counter to "0"; initiate transmission and then reset this bit to logic zero
SMOD.4	0	Bit not used; value is always "0"

SMOD.7	SMOD.6	SMOD.5	Clock Selection	R/W Status of SBUF
0	0	0	External clock at SCK pin	SBUF is enabled when SIO operation is halted or when SCK goes high.
0	0	1	Use TOL0 clock from TC0	
0	1	x	CPU clock: fxx/4, fxx/8, fxx/64	Enable SBUF read/write
1	0	0	4.09 kHz clock: $fxx/2^{10}$	SBUF is enabled when SIO operation is halted or when SCK goes high.
1	1	1	262 kHz clock: $fxx/2^4$	

NOTES:
1. 'fxx' = system clock; 'x' means 'don't care.'
2. kHz frequency ratings assume a system clock (fxx) running at 4.19 MHz.
3. The SIO clock selector circuit cannot select a $fxx/2^4$ clock if the CPU clock is fxx/64.

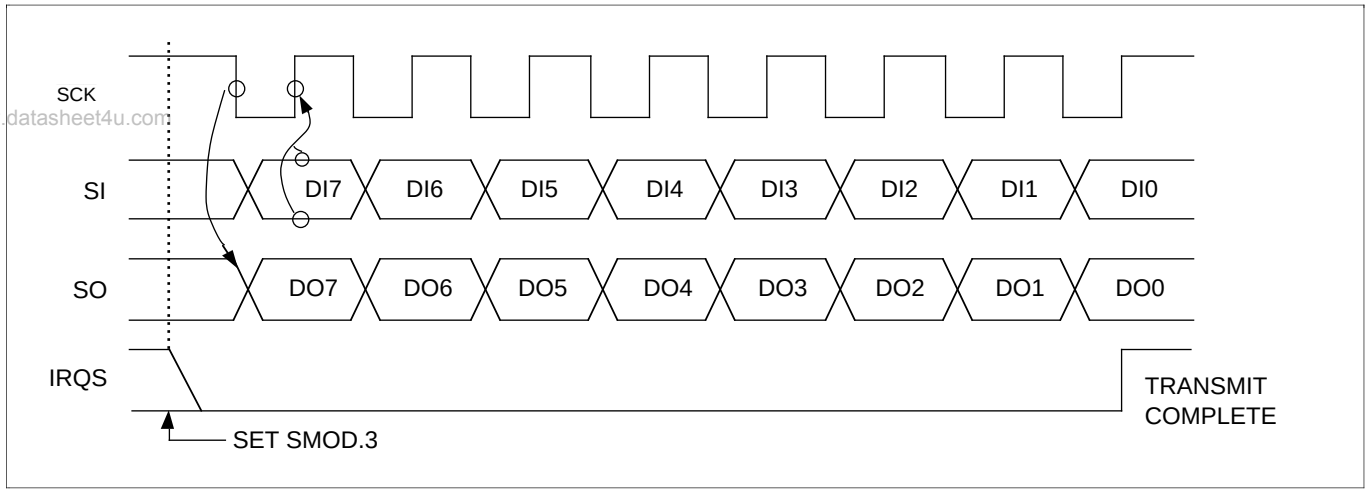


Figure 57. SIO Timing in Transmit/Receive Mode

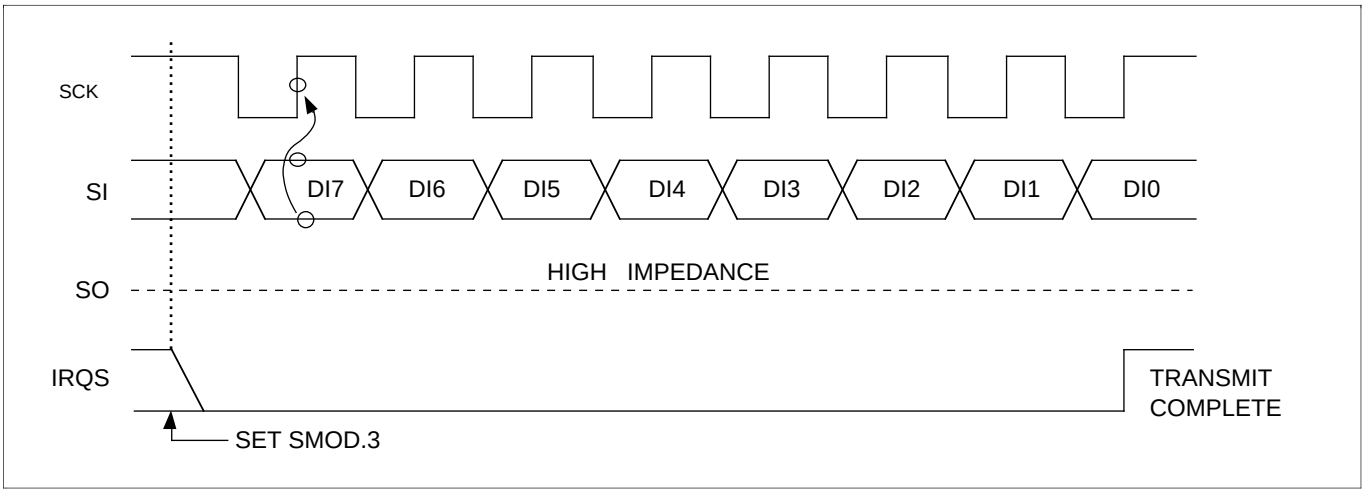
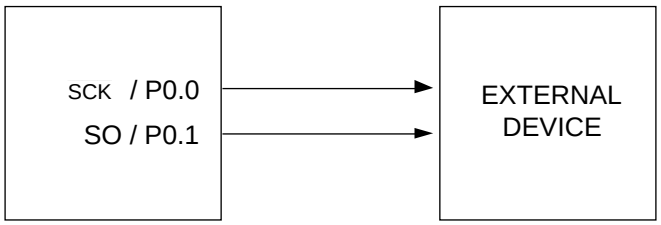


Figure 58. SIO Timing in Receive-Only Mode

☞ PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O

1. Transmit the data value 48H through the serial I/O interface using an internal clock frequency of fx/2^4 and in MSB-first mode:

```
        BITS    EMB
        SMB     15
        LD      EA,#03H
        LD      PMG1,EA         ;  P0.0 / SCK  and P0.1 / SO ← Output
        LD      EA,#48H         ;
        LD      SBUF,EA         ;
        LD      EA,#0EEH
        LD      SMOD,EA         ;  SIO data transfer
```



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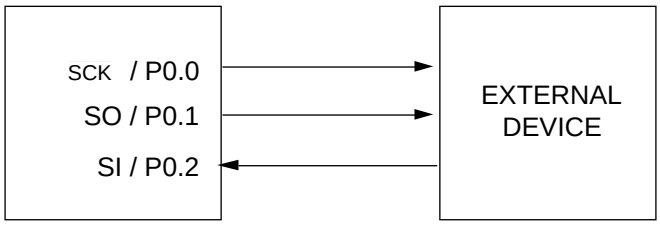
2. Use CPU clock to transfer and receive serial data at high speed:

```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ;  P0.0 / SCK  and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ;  TDATA address = Bank0(20H–7FH)
        LD      SBUF,EA
        LD      EA,#4FH
        LD      SMOD,EA         ;  SIO start
        BITR    IES             ;  SIO Interrupt Enable
STEST   BTSTZ   IRQS
        JR      STEST
        LD      EA,SBUF
        LD      RDATA,EA        ;  RDATA address = Bank0 (20H–7FH)
```

☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Continued)**

3. Transmit and receive an internal clock frequency of 4.09 kHz (at 4.19 MHz) in LSB-first mode:

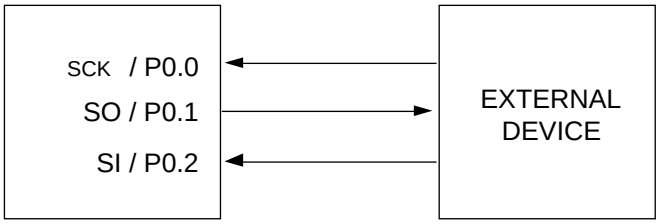

```
        BITR    EMB
        LD      EA,#03H
        LD      PMG1,EA         ; P0.0 / SCK and P0.1 / SO ← Output, P0.2 / SI ← Input
        LD      EA,TDATA        ; TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#8FH
        LD      SMOD,EA         ; SIO start
        EI
        BITS    IES             ; SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ; Store SMB, SRB
        PUSH    EA              ; Store EA
        BITR    EMB
        LD      EA,TDATA        ; EA ← Transmit data
                                ; TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ; Transmit data ↔ Receive data
        LD      RDATA,EA        ; RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ; SIO start
        POP     EA
        POP     SB
        IRET
```



☞ **PROGRAMMING TIP — Setting Transmit/Receive Modes for Serial I/O (Concluded)**

4. Transmit and receive an external clock in LSB-first mode:

```
        BITR    EMB
        LD      EA,#02H
        LD      PMG1,EA         ;  P0.1/ SO ← Output, P0.0/ SCK and P0.2/ SI← Input
        LD      EA,TDATA        ;  TDATA address = Bank0 (20H–7FH)
        LD      SBUF,EA
        LD      EA,#0FH
        LD      SMOD,EA         ;  SIO start
        EI
        BITS    IES             ;  SIO Interrupt Enable
        •
        •
        •
INTS    PUSH    SB              ;  Store SMB, SRB
        PUSH    EA              ;  Store EA
        BITR    EMB
        LD      EA,TDATA        ;  EA ← Transmit data
                                ;  TDATA address = Bank0 (20H–7FH)
        XCH     EA,SBUF         ;  Transmit data ↔ Receive data
        LD      RDATA,EA        ;  RDATA address = Bank0 (20H–7FH)
        BITS    SMOD.3          ;  SIO start
        POP     EA
        POP     SB
        IRET
```



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ELECTRICAL DATA

Table 35. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply voltage	V_{DD}		– 0.3 to + 7.0	V
Input voltage	V_{I1}	Applies to I/O ports 4 and 5 only. Pull-up resistors are individually assignable to pins at ports 4 and 5, or they can remain open-drain.	– 0.3 to V_{DD} + 0.3 (with pull-up resistor) – 0.3 to + 9.0 (open-drain)	V
	V_{I2}	All I/O ports except 4 and 5	– 0.3 to V_{DD} + 0.3	
Output voltage	V_O		– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output current low	I_{OL}	One I/O port active	+ 30 (peak value)	mA
			+ 15 *	
		Total value for ports 0, 2, 3, and 5	+ 100 (peak value)	
			+ 60 *	
		Total value for ports 4, 6, and 7	+ 100	
Operating temperature	T_A		– 40 to + 85	°C
Storage temperature	T_{STG}		– 65 to + 150	°C

* The values for output current low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 36. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7 V_{DD}	—	V_{DD}	V
	V_{IH2}	Ports 0–2, 6, 7, 9, 10, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}		V_{DD}	
		Ports 4 and 5 open-drain	0.7 V_{DD}		9	
	V_{IH4}	X_{in}, X_{out}, and XT_{in}	V_{DD} – 0.5		V_{DD}	
Input low voltage	V_{IL1}	Ports 3, 4, 5	—	—	0.3 V_{DD}	V
	V_{IL2}	Ports 0–2, 6, 7, 9, 10, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{in}, X_{out}, and XT_{in}			0.4	

Table 36. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 1 mA Ports 0, 2, 3, 6, 7, and BIAS	V_{DD} – 1.0	—	—	V
		I_{OH} = – 100 μA	V_{DD} – 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = – 100 μA; port 8 only	V_{DD} – 2.0			
		I_{OH} = – 30 μA	V_{DD} – 1.0			
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 4 and 5 only	—	0.4	2	V
		I_{OL} = 1.6 mA Ports 0, 2, 3, 6, and 7 only		—	0.4	
		I_{OL} = 400 μA Ports 0, 2, 3, 6, and 7 only			0.2	
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 μA; port 8 only			1	
		I_{OL} = 50 μA			1	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except ports 4 and 5, X_{IN}, X_{out}, and XT_{in}	—	—	3	μA
	I_{LIH2}	V_{IN} = V_{DD} X_{in}, X_{out}, XT_{in} only			20	
	I_{LIH3}	V_{IN} = 9 V Ports 4 and 5 are open-drain			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{in}, X_{out}, XT_{in} and RESET	—	—	– 3	μA
	I_{LIL2}	V_{IN} = 0 V X_{in}, X_{out}, XT_{in},only			– 20	
Output high leakage current	I_{LOH1}	V_{out} = V_{DD} All output pins except for port 4 and port 5	—	—	3	μA
	I_{LOH2}	Ports 4 and 5 are open-drain V_{out} = 9 V			20	
Output low leakage current	I_{LOL}	V_{out} = 0 V	—	—	– 3	μA

Table 36. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pull-up resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Port 0, 1 (not P1.3), 2, 3, 6, and 7	15	40	80	KΩ
		V_{DD} = 3 V ± 10%	30	—	200	
	R_{L2}	V_{out} = V_{DD} – 2 V V_{DD} = 5 V ± 10% Ports 4 and 5 only	15	40	70	
		V_{DD} = 3 V ± 10%	10	—	60	
	R_{L3}	V_{IN} = 0 V V_{DD} = 5 V ± 10% RESET	100	230	400	
		V_{DD} = 3 V ± 10%	200	490	800	
LCD voltage dividing resistor	R_{LCD}		50	100	140	KΩ
COM output impedance	R_{COM}	V_{DD} = 5 V ± 10%	—	3	6	KΩ
		V_{DD} = 3 V ± 10%		10	15	
SEG output impedance	R_{SEG}	V_{DD} = 5 V ± 10%	—	3	20	KΩ
		V_{DD} = 3 V ± 10%		10	60	

Table 36. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10% (3) 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	2.5	8	mA
		V_{DD} = 3 V ± 10% (4)		0.62	1.2	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% 4.19 MHz crystal oscillator C1 = C2 = 22 pF	—	0.6	1.8	
		V_{DD} = 3 V ± 10%		0.25	1.0	
	I_{DD3} (5)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		30	90	µA
	I_{DD4} (5)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		5	15	
	I_{DD5}	Stop mode; XT_{in} = 0 V V_{DD} = 5 V ± 10%		0.5	5	
		V_{DD} = 3 V ± 10%		0.1	3	

NOTES:
1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents and A/D converter.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, the power control register (PCON) must be set to 0011B.
4. For low-speed controller operation, the power control register (PCON) must be set to 0000B.
5. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.

Table 37. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95	—	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8	—	64	
		With subsystem clock (fxt)	114	122	125	
TCL0, TCL1 input frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0	—	1	MHz
		V_{DD} = 2.7 V to 4.5 V			275	kHz
TCL0, TCL1 input high, low width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48	—	—	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
SCK cycle time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External SCK source	800	—	—	ns
		Internal SCK source	950			
		V_{DD} = 2.7 V to 4.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK high, low width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External SCK source	400	—	—	ns
		Internal SCK source	$t_{KCY}/2 - 50$			
		V_{DD} = 2.7 V to 4.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 - 150$			
SI setup time to SCK high	t_{SIK}	External SCK source	100	—	—	ns
		Internal SCK source	150			
SI hold time to SCK high	t_{KSI}	External SCK source	400	—	—	ns
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External SCK source	—	—	300	ns
		Internal SCK source			250	
		V_{DD} = 2.7 V to 4.5 V External SCK source			1000	
		Internal SCK source			1000	

Table 37. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)	—	—	µs
		INT1, INT2, INT4, KS0–KS7	10			
RESET input low width	t_{RSL}	Input	10	—	—	µs

NOTES:
1. Unless otherwise specified, instruction cycle time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

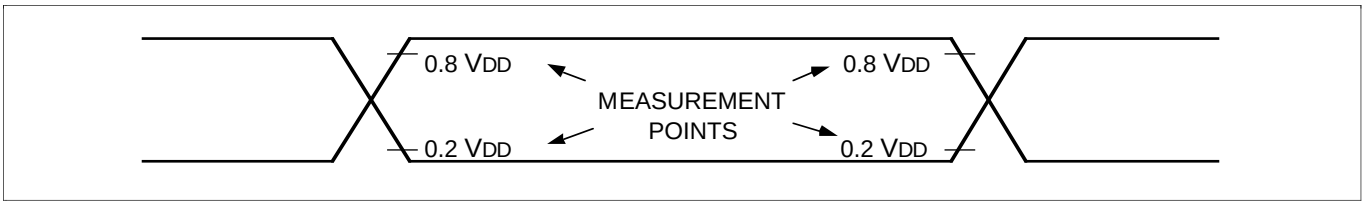

Figure 59. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

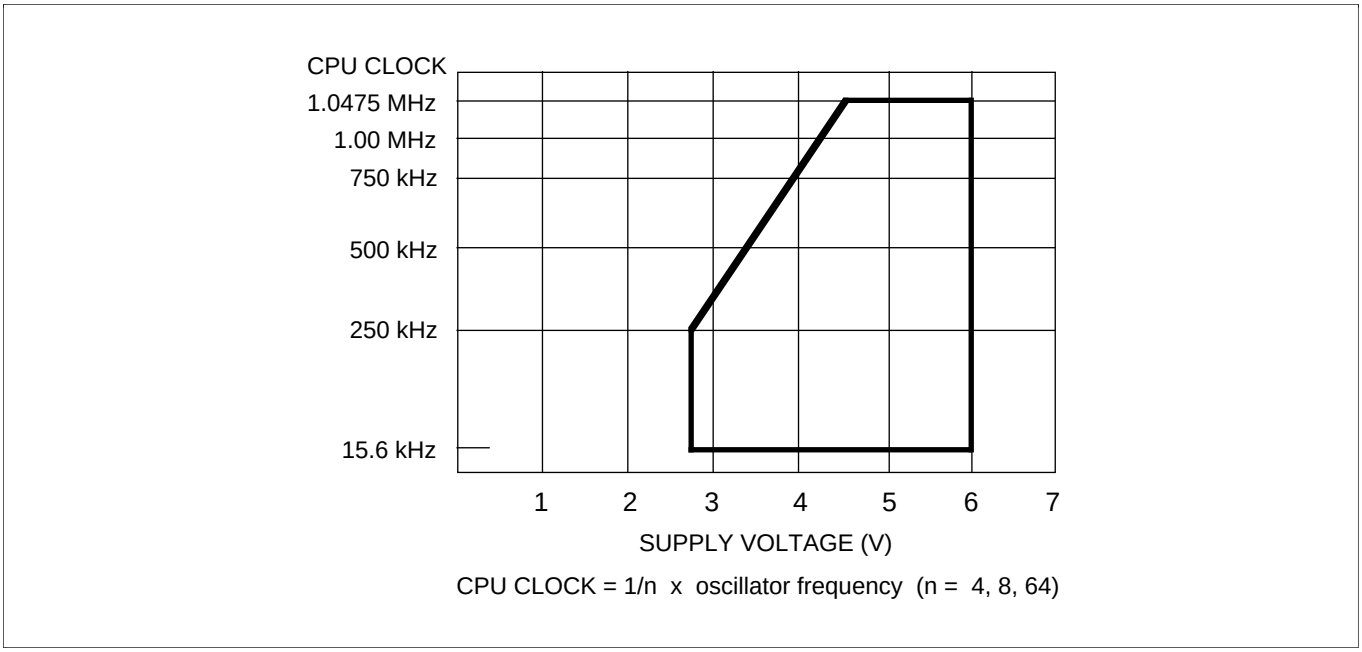

Figure 60. Standard Operating Voltage Range

Table 38. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are returned to V_{SS}	—	—	15	pF
Output capacitance	C_{OUT}		—	—	15	pF
I/O capacitance	C_{IO}		—	—	15	pF

Table 39. A/D Converter Electrical Characteristics

(T_A = – 10 °C to + 70 °C, V_{DD} = 3.5 V to 6.0 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution		—	8	8	8	bit
Absolute accuracy (1)		2.5 V < AV_{REF} < V_{DD}	—	—	± 1.5	LSB
Conversion time (2)	t_{CON}	—	—	—	100/fx (3)	µs
Analog input voltage	V_{IAN}	—	AV_{SS}	—	AV_{REF}	V
Analog input impedance	R_{AN}	—	—	1000	—	MΩ

NOTES:
1. Absolute accuracy does not include the quantization error (± 1/2 LSB).
2. Conversion time is the time required from the moment a conversion operation starts until it ends (EOC = 0).
3. 'fx' is the abbreviation for main system clock.

Table 40. Main System Clock Oscillator Frequencies

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Clock	Conditions	Min	Typ	Max	Unit
Ceramic	fx	—	0.4	—	4.5	MHz
Crystal	fx	—	0.4	4.19	4.5	MHz
Resistor-capacitor (RC)	fx	V_{DD} = 5 V	0.4	—	2	MHz
External clock	X_{in} input	—	0.4	—	4.5	MHz

NOTE: 'fx' is the main system clock.

Table 41. Main System Clock Oscillation Stabilization Times

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Conditions	Min	Typ	Max	Unit
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	4	ms
Crystal	V_{DD} = 4.5 V to 6.0 V	—	—	10	ms
	V_{DD} = 2.7 V to 4.5 V	—	—	30	ms
External clock	X_{in} input high and low level width (t_{XH}, t_{XL})	100	—	—	ns

NOTE: Oscillation stabilization time is the time required for the main system clock to return to normal oscillation frequency after a power-on occurs, or when stop mode is terminated.

Table 42. Subsystem Clock Oscillator Frequencies

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Clock	Conditions	Min	Typ	Max	Unit
Crystal	fxt	—	32	32.768	35	kHz
External clock	XT_{in} input (fxt)	—	32	—	100	kHz

NOTE: 'fxt' is the subsystem clock

Table 43. Subsystem Clock Oscillation Stabilization Time

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Conditions	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 6.0 V	—	1.0	2	s
	V_{DD} = 2.7 V to 4.5 V	—	—	10	s
External clock	XT_{in} input high and low level width (t_{XTH}, t_{XTL})	5	—	15	µs

NOTE: Oscillation stabilization time is the time required for the subsystem clock to return to normal oscillation frequency after a power-on occurs.

Table 44. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	2.0	—	7.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	—	0.1	10	µA
Release signal set time	t_{SREL}	Normal operation	0	—	—	µs
Oscillator stabilization wait time (Note1)	t_{WAIT}	Released by RESET	—	2^{17} / fx	—	ms
		Released by interrupt	—	(Note 2)	—	ms

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

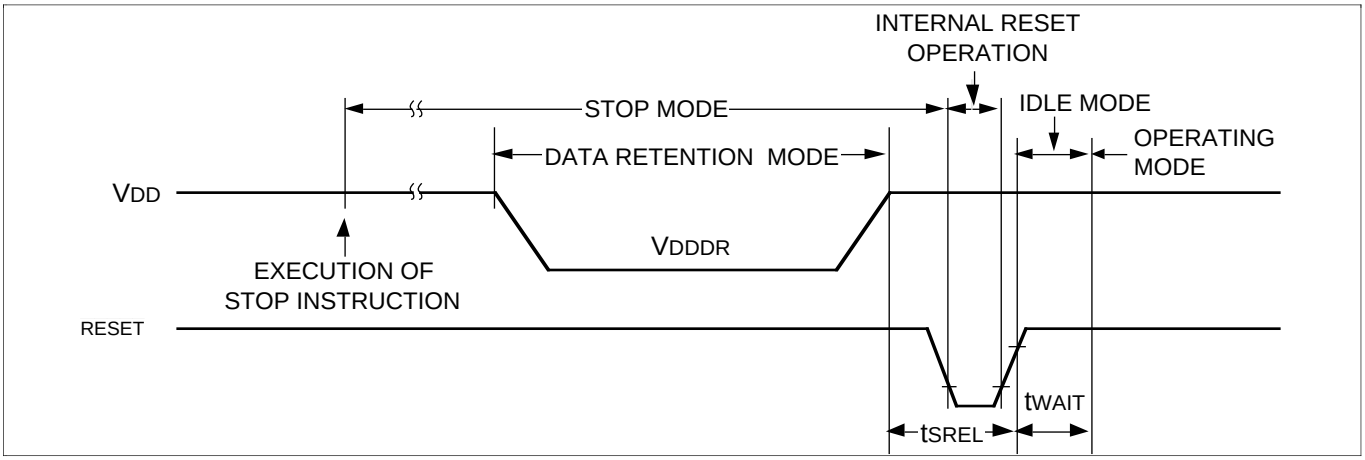

Figure 61. Stop Mode Release Timing When Initiated By RESET

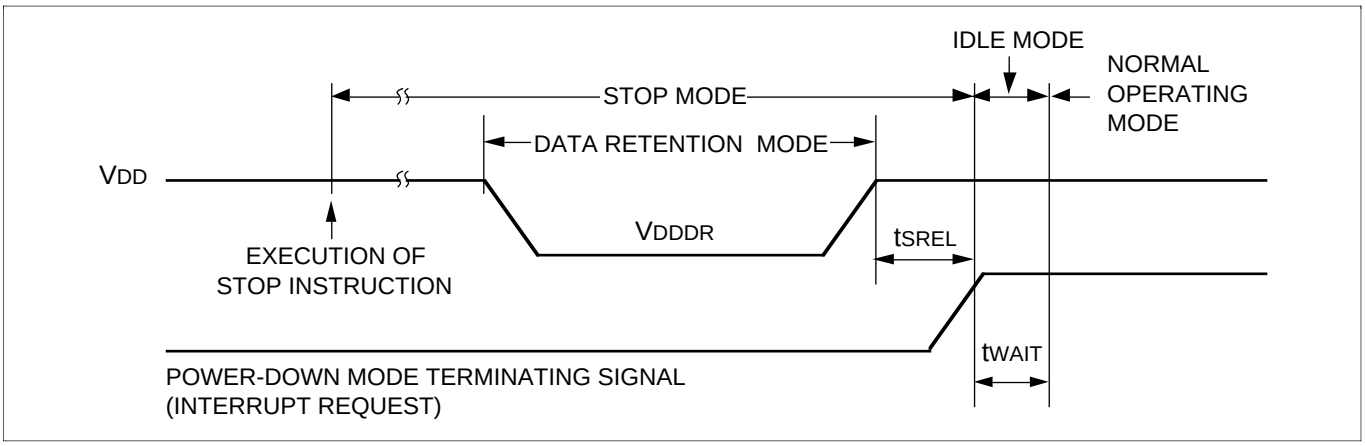

Figure 62. Stop Mode Release Timing When Initiated By Interrupt Request

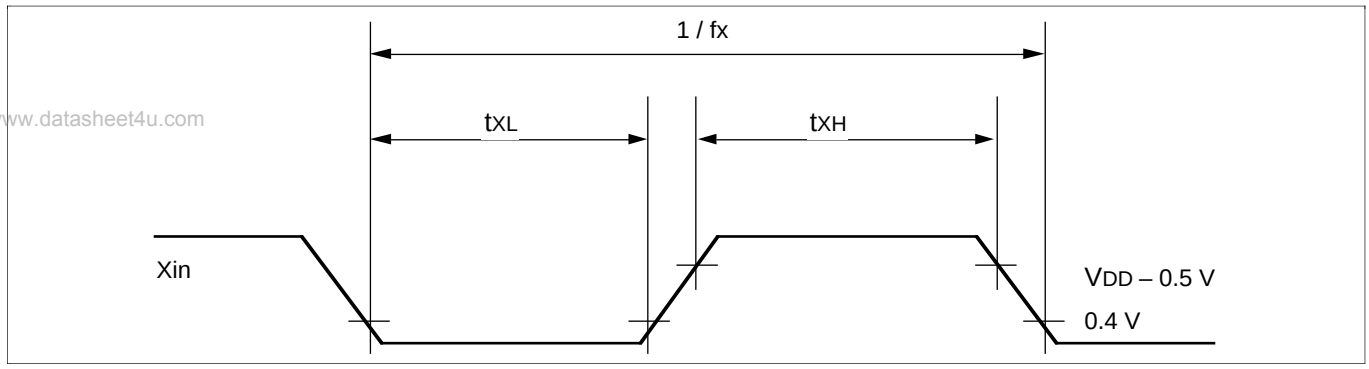

Figure 63. Clock Timing Measurement at X_{in}

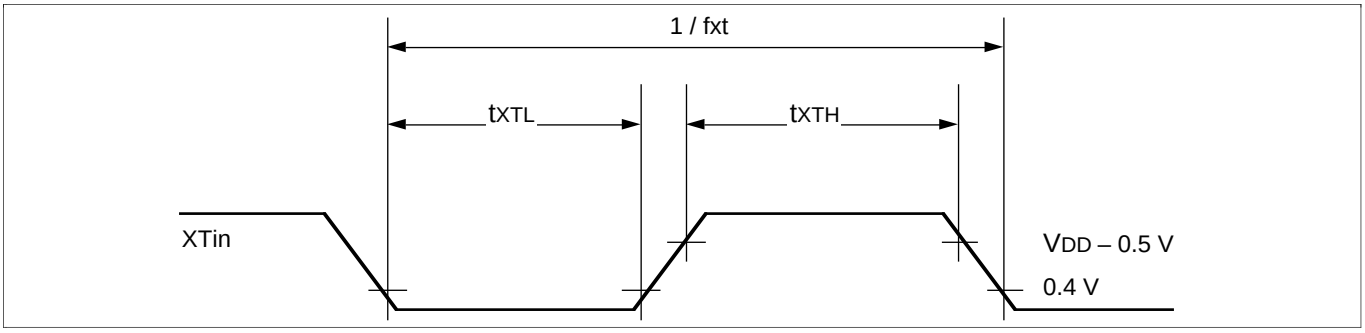

Figure 64. Clock Timing Measurement at XT_{in}

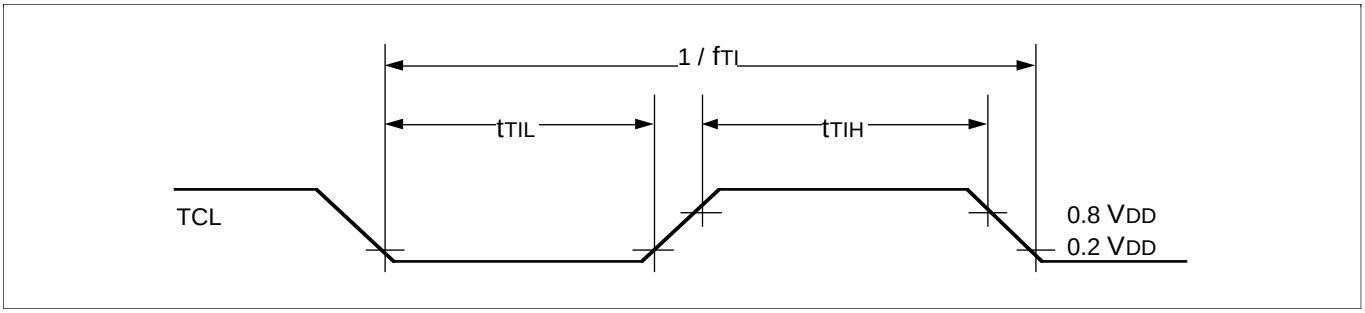

Figure 65. TCL Timing

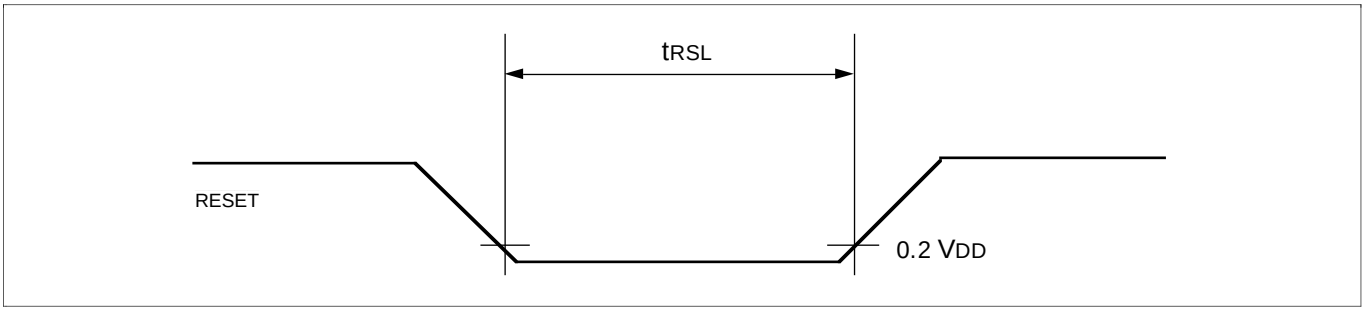

Figure 66. Input Timing for RESET Signal

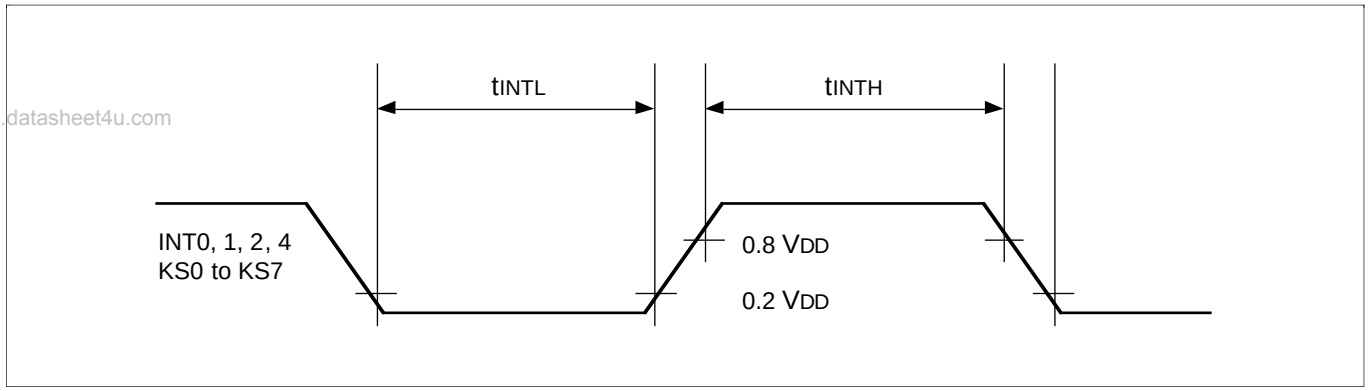

Figure 67. Input Timing for External Interrupts and Quasi-Interrupts

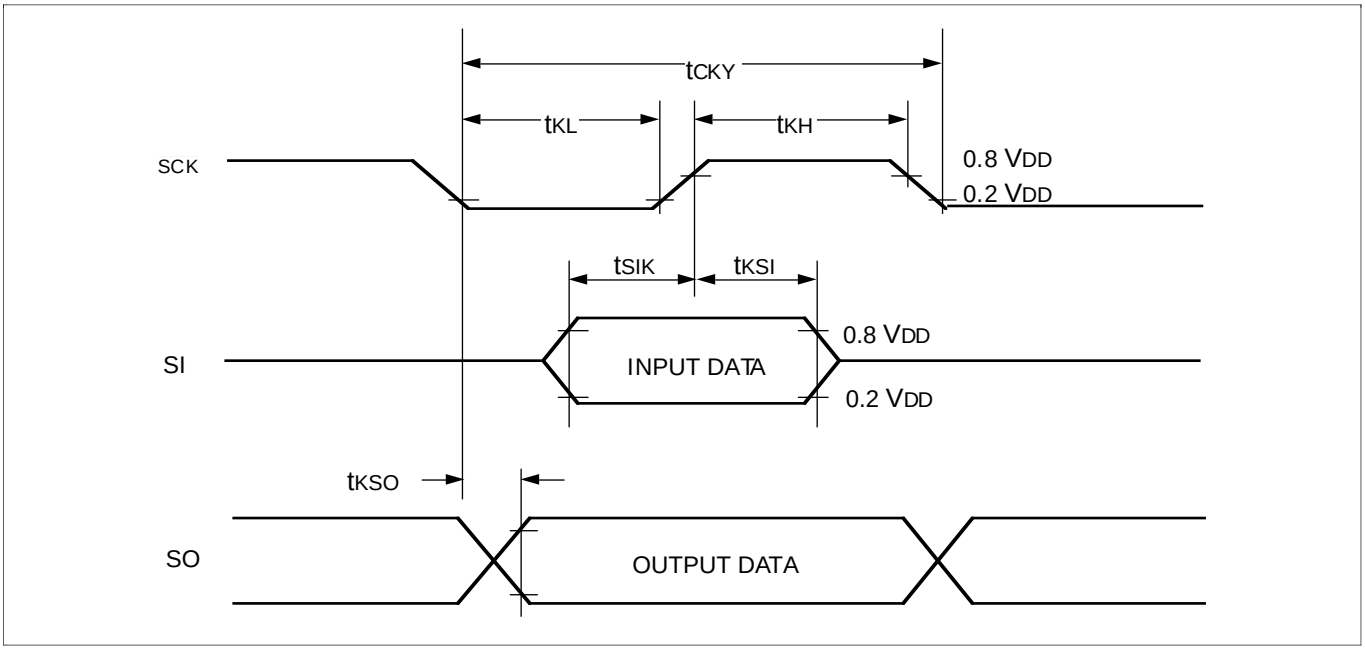

Figure 68. Serial Data Transfer Timing

NOTES