15 ELECTRICAL DATA

In this section, preliminary information on KS57C2408 electrical characteristics is presented as tables and graphics. This information is arranged in the following order:

Standard Electrical Characteristics

- Absolute maximum ratings
- D.C. electrical characteristics
- A.C. electrical characteristics
- I/O capacitance
- A/D converter
- Operating voltage range

Oscillation Characteristics

- Main system clock oscillator frequencies
- Main system clock stabilization times
- Subsystem clock oscillator frequencies
- Subsystem clock stabilization times

Stop Mode Characteristics and Timing Waveforms

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by $\overline{\text{RESET}}$
- Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

- Clock timing measurement at X_{in}
- Clock timing measurement at XT_{in}
- TCL timing
- Input timing for $\overline{\text{RESET}}$
- Input timing for external interrupts and quasi-interrupts
- Serial data transfer timing

D.C. Characteristic Curves

- I_{DD1}, I_{DD2} vs. V_{DD}
- I_{DD3} vs. V_{DD}
- I_{DD4} vs. V_{DD}
- I_{DD5} vs. V_{DD}
- I_{OH} vs. V_{OH}
- I_{OL} vs. V_{OL}
- I_{DD1} vs. Frequency
- I_{DD1} vs. Frequency (V_{DD} = 5.5 V)
- I_{DD2} vs. Frequency
- Frequency vs. V_{DD}
- Frequency vs. Resistor

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Table 15–1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply voltage	V_{DD}		– 0.3 to + 7.0	V
Input voltage	V_{I1}	Applies to I/O ports 4 and 5 only. Pull-up resistors are individually assignable to pins at ports 4 and 5, or they can remain open-drain.	– 0.3 to V_{DD} + 0.3 (with pull-up resistor) – 0.3 to + 9.0 (open-drain)	V
	V_{I2}	All I/O ports except 4 and 5	– 0.3 to V_{DD} + 0.3	
Output voltage	V_O		– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output current low	I_{OL}	One I/O port active	+ 30 (peak value)	mA
			+ 15 *	
		Total value for ports 0, 2, 3, and 5	+ 100 (peak value)	
			+ 60 *	
		Total value for ports 4, 6, and 7	+ 100	
Operating temperature	T_A		– 40 to + 85	°C
Storage temperature	T_{STG}		– 65 to + 150	°C

* The values for output current low (I_{OL}) are calculated as Peak Value × $\sqrt{\text{Duty}}$

Table 15–2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0–2, 6, 7, 9, and 10	0.8 V_{DD}		V_{DD}	
		$\overline{\text{RESET}}$	0.85 V_{DD}			
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}		V_{DD}	
		Ports 4 and 5 open-drain	0.7 V_{DD}		9	
	V_{IH4}	X_{in}, X_{out}, and XT_{in}	V_{DD} – 0.5		V_{DD}	
Input low voltage	V_{IL1}	Ports 3, 4, 5			0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 2, 6, 7, 9, and 10			0.2 V_{DD}	
		$\overline{\text{RESET}}$			0.15 V_{DD}	
	V_{IL3}	X_{in}, X_{out}, and XT_{in}			0.4	

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Table 15–2. D.C. Electrical Characteristics (Continued)

(T_A = −40 °C to +85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −1 mA Ports 0, 2, 3, 6, 7, and BIAS	V_{DD} − 1.0			V
		I_{OH} = −100 µA	V_{DD} − 0.5			
	V_{OH2}	V_{DD} = 4.5 V to 6.0 V I_{OH} = −100 µA; port 8 only	V_{DD} − 2.0			
		I_{OH} = −30 µA	V_{DD} − 1.0			
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 15 mA Ports 4 and 5 only		0.4	2	V
		I_{OL} = 1.6 mA Ports 0, 2, 3, 6, and 7 only			0.4	
		I_{OL} = 400 µA Ports 0, 2, 3, 6, and 7 only			0.2	
	V_{OL2}	V_{DD} = 4.5 V to 6.0 V I_{OL} = 100 µA; port 8 only			1	
		I_{OL} = 50 µA			1	
Input high leakage current	I_{LIH1}	V_{in} = V_{DD} All input pins except ports 4 and 5, X_{in}, X_{out}, and XT_{in}			3	µA
	I_{LIH2}	V_{in} = V_{DD} X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			20	
	I_{LIH3}	V_{in} = 9 V Ports 4 and 5 are open-drain			20	
Input low leakage current	I_{LIL1}	V_{in} = 0 V All input pins except X_{in}, X_{out}, and XT_{in}			−3	µA
	I_{LIL2}	V_{in} = 0 V X_{in}, X_{out}, XT_{in}, and $\overline{RESET}$ only			−20	
Output high leakage current	I_{LOH1}	V_{out} = V_{DD} All output pins except for port 4 and port 5			3	µA
	I_{LOH2}	Ports 4 and 5 are open-drain V_{out} = 9 V			20	
Output low leakage current	I_{LOL}	V_{out} = 0 V			−3	µA

Table 15–3. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95		64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8		64	
		With subsystem clock (fxt)	114	122	125	
TCL0, TCL1 input frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0		1	MHz
		V_{DD} = 2.7 V to 4.5 V			275	kHz
TCL0, TCL1 input high, low width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48			µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	800			ns
		Internal $\overline{SCK}$ source	950			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	3200			
		Internal $\overline{SCK}$ source	3800			
$\overline{SCK}$ high, low width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	400			ns
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 50$			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	1600			
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 150$			
SI setup time to $\overline{SCK}$ high	t_{SIK}	External $\overline{SCK}$ source	100			ns
		Internal $\overline{SCK}$ source	150			
SI hold time to $\overline{SCK}$ high	t_{KSI}	External $\overline{SCK}$ source	400			ns
		Internal $\overline{SCK}$ source	400			
Output delay for $\overline{SCK}$ to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source			300	ns
		Internal $\overline{SCK}$ source			250	
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source			1000	
		Internal $\overline{SCK}$ source			1000	

Table 15–3. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95		64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8		64	
		With subsystem clock (fxt)	114	122	125	
TCL0, TCL1 input frequency	f_{TI0}, f_{TI1}	V_{DD} = 4.5 V to 6.0 V	0		1	MHz
		V_{DD} = 2.7 V to 4.5 V			275	kHz
TCL0, TCL1 input high, low width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 6.0 V	0.48			µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	800			ns
		Internal $\overline{SCK}$ source	950			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	3200			
		Internal $\overline{SCK}$ source	3800			
$\overline{SCK}$ high, low width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source	400			ns
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 50$			
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source	1600			
		Internal $\overline{SCK}$ source	$t_{KCY}/2 - 150$			
SI setup time to $\overline{SCK}$ high	t_{SIK}	External $\overline{SCK}$ source	100			ns
		Internal $\overline{SCK}$ source	150			
SI hold time to $\overline{SCK}$ high	t_{KSI}	External $\overline{SCK}$ source	400			ns
		Internal $\overline{SCK}$ source	400			
Output delay for $\overline{SCK}$ to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V External $\overline{SCK}$ source			300	ns
		Internal $\overline{SCK}$ source			250	
		V_{DD} = 2.7 V to 4.5 V External $\overline{SCK}$ source			1000	
		Internal $\overline{SCK}$ source			1000	

Table 15–3. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)			µs
		INT1, INT2, INT4, KS0–KS7	10			
$\overline{RESET}$ input low width	t_{RSL}	Input	10			µs

NOTES:
1. Unless otherwise specified, instruction cycle time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

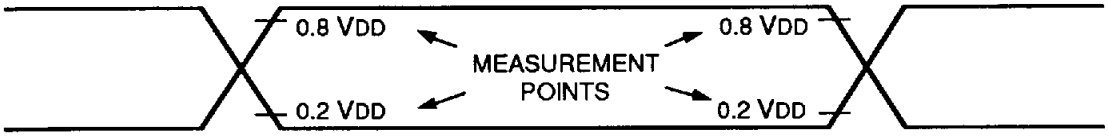

Figure 15–1. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

Table 15–4. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are returned to V_{SS}	—	—	15	pF
Output capacitance	C_{OUT}		—	—	15	pF
I/O capacitance	C_{IO}		—	—	15	pF

Table 15–5. A/D Converter Electrical Characteristics

(T_A = – 10 °C to + 70 °C, V_{DD} = 3.5 V to 6.0 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution			8	8	8	bit
Absolute accuracy (1)		2.5 V < AV_{REF} < V_{DD}			± 1.5	LSB
Conversion time (2)	t_{CON}				100/fx (3)	µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}			1000		MΩ

NOTES:

1. Absolute accuracy does not include the quantization error (± 1/2 LSB).
2. Conversion time is the time required from the moment a conversion operation starts until it ends (EOC = 0).
3. 'fx' is the abbreviation for main system clock.

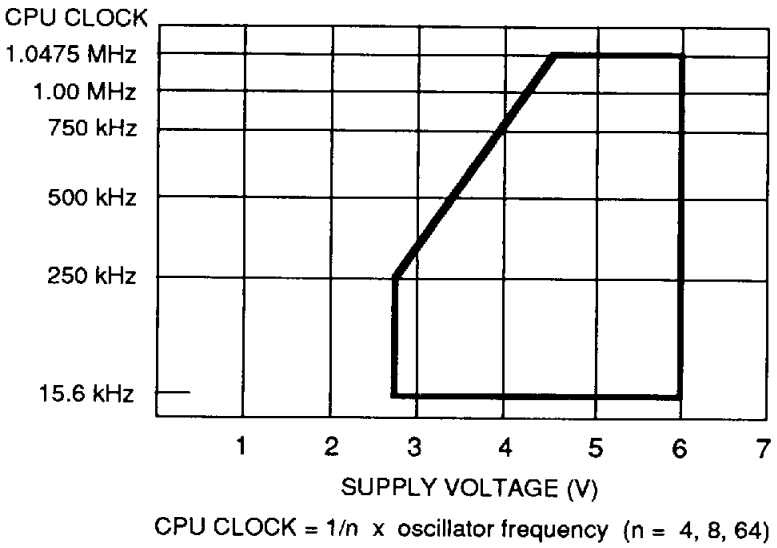

Figure 15–2. Standard Operating Voltage Range

Table 15–6. Main System Clock Oscillator Frequencies

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Clock	Conditions	Min	Typ	Max	Unit
Ceramic	fx		0.4		4.5	MHz
Crystal	fx		0.4	4.19	4.5	MHz
Resistor-capacitor (RC)	fx	R = 20 K, V_{DD} = 5 V		4.0		MHz
	fx	R = 100 K, V_{DD} = 3 V		1.0		MHz
External clock	X_{in} input		0.4		4.5	MHz

NOTE: 'fx' is the main system clock.

Table 15–7. Main System Clock Oscillation Stabilization Times

(T_A = – 40 °C + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Conditions	Min	Typ	Max	Unit
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	—	—	4	ms
	V_{DD} = 4.5 V to 6.0 V	—	—	10	ms
	V_{DD} = 2.7 V to 4.5 V	—	—	30	ms
External clock	X_{in} input high and low level width (t_{XH}, t_{XL})	100	—	—	ns

NOTE: Oscillation stabilization time is the time required for the main system clock to return to normal oscillation frequency after a power-on occurs, or when stop mode is terminated.

Table 15–8. Subsystem Clock Oscillator Frequencies

(T_A = −40 °C +85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Clock	Conditions	Min	Typ	Max	Unit
Crystal	fxt	—	32	32.768	35	kHz
External clock	XT_{in} input (fxt)	—	32	—	100	kHz

NOTE: 'fxt' is the subsystem clock

Table 15–9. Subsystem Clock Oscillation Stabilization Time

(T_A = −40 °C +85 °C, V_{DD} = 2.7 V to 6.0 V)

Oscillator Type	Conditions	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 6.0 V	—	1.0	2	s
	V_{DD} = 2.7 V to 4.5 V	—	—	10	s
External clock	XT_{in} input high and low level width (t_{XTH}, t_{XTL})	5	—	15	μs

NOTE: Oscillation stabilization time is the time required for the subsystem clock to return to normal oscillation frequency after a power-on occurs.

Table 15–10. RAM Data Retention Supply Voltage in Stop Mode

(T_A = −40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	2.0	—	7.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V	—	0.1	10	μA
Release signal set time	t_{SREL}	Normal operation	0	—	—	μs
Oscillator stabilization wait time (Note1)	t_{WAIT}	Released by $\overline{RESET}$	—	2^{17} / fx	—	ms
		Released by interrupt	—	(Note 2)	—	ms

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

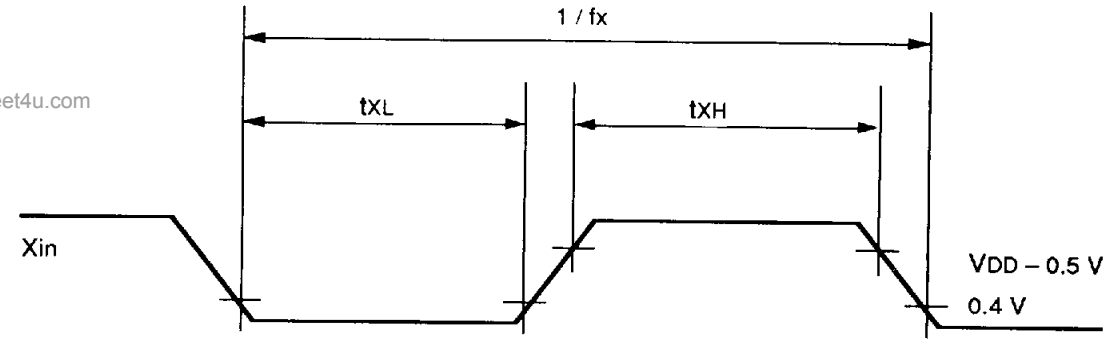

Figure 15–5. Clock Timing Measurement at X_{in}

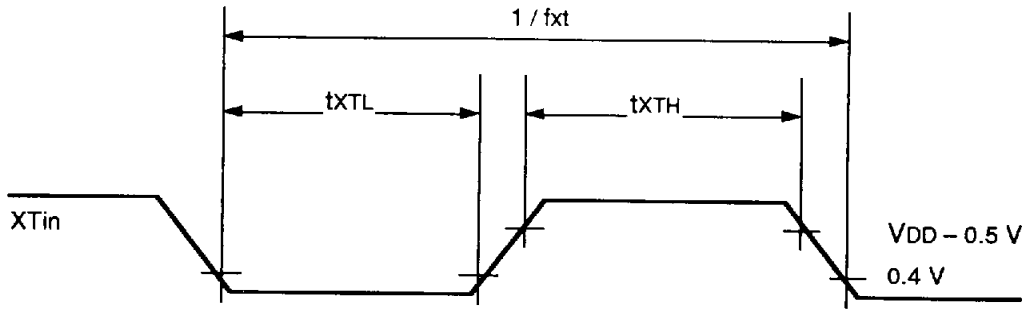

Figure 15–6. Clock Timing Measurement at XT_{in}

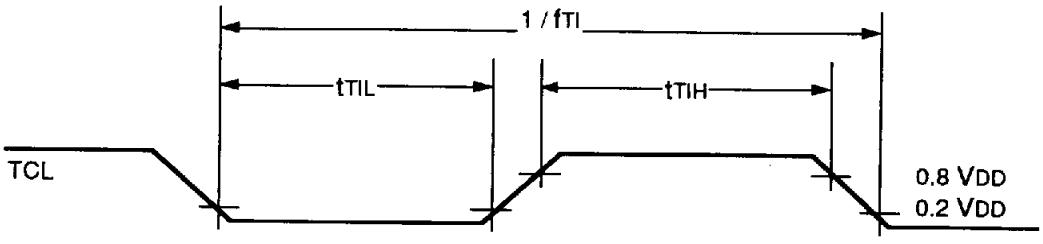

Figure 15–7. TCL Timing

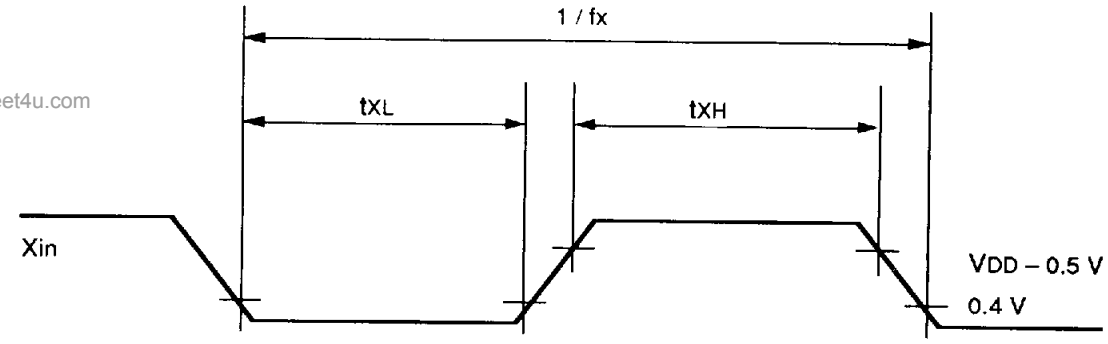

Figure 15–5. Clock Timing Measurement at X_{in}

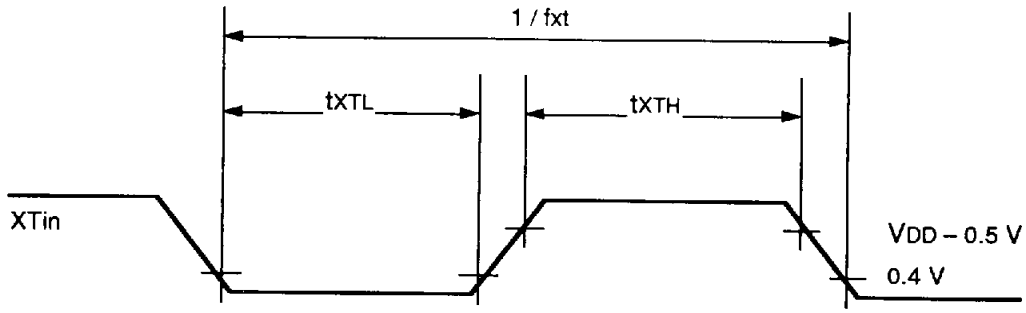

Figure 15–6. Clock Timing Measurement at XT_{in}

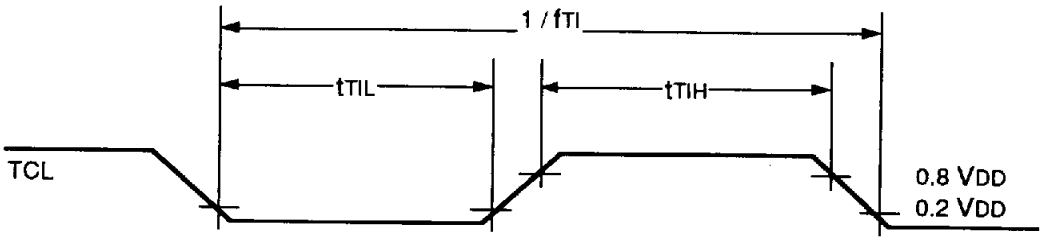

Figure 15–7. TCL Timing

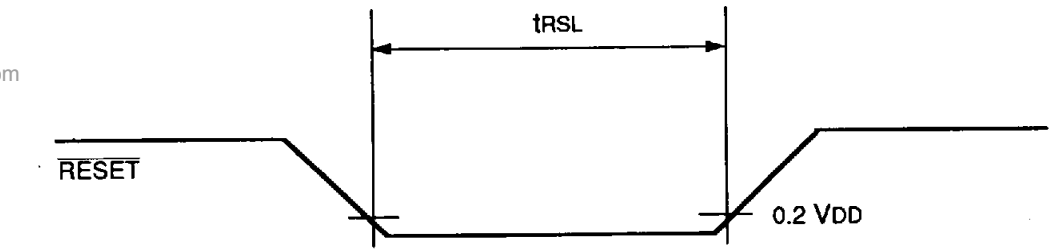

Figure 15–8. Input Timing for $\overline{\text{RESET}}$ Signal

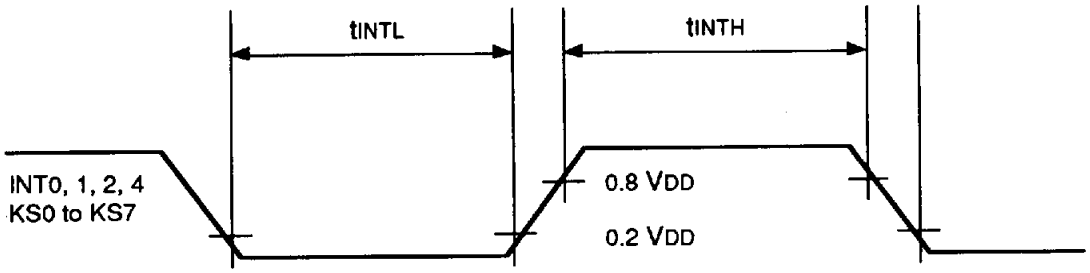

Figure 15–9. Input Timing for External Interrupts and Quasi-Interrupts

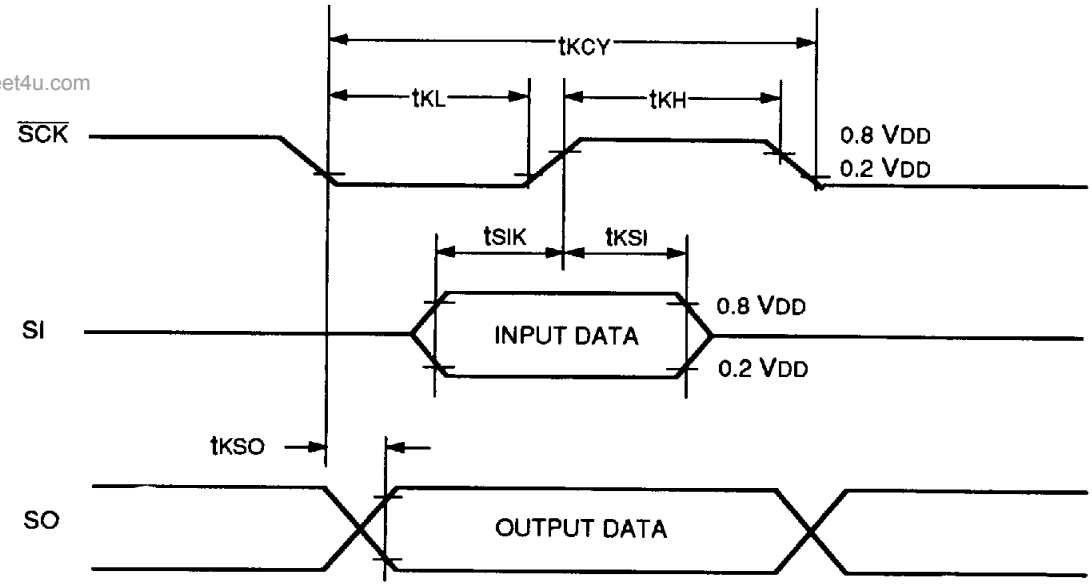

Figure 15–10. Serial Data Transfer Timing

D.C. CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

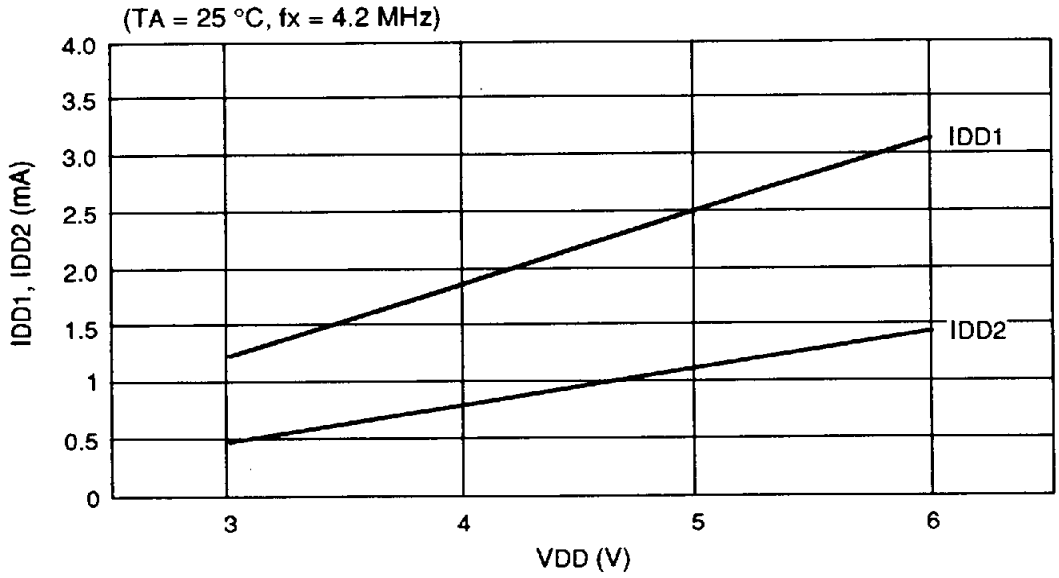

Figure 15–11. I_{DD1}, I_{DD2} vs. V_{DD}

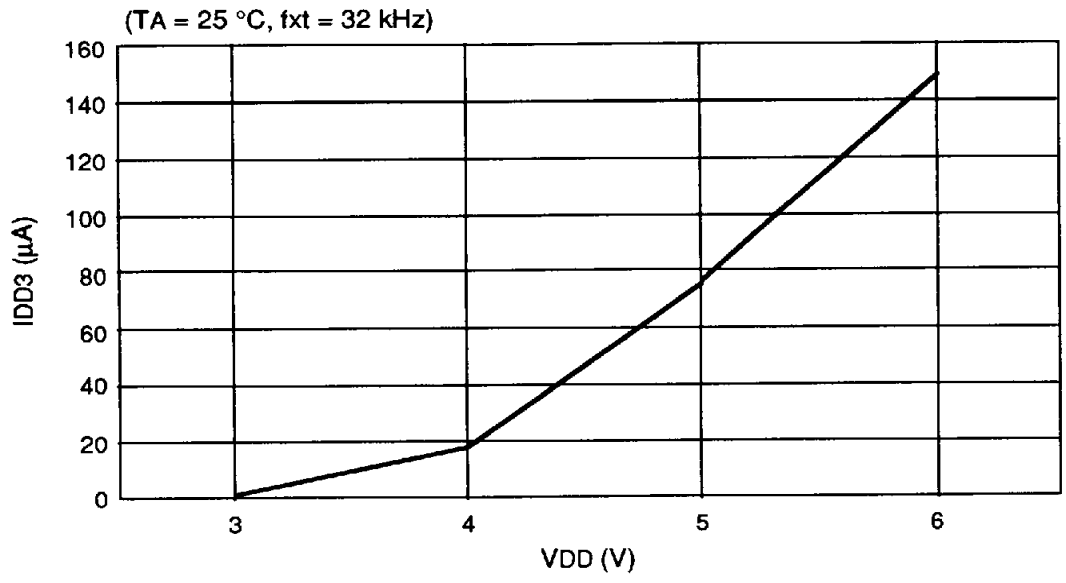

Figure 15–12. I_{DD3} vs. V_{DD}

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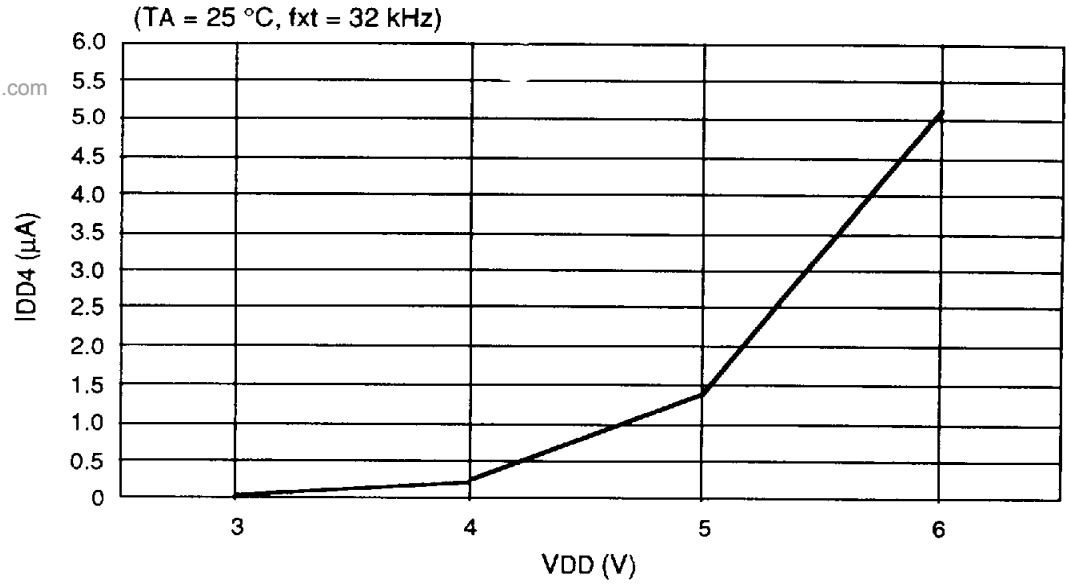


Figure 15–13. I_{DD4} vs. V_{DD}

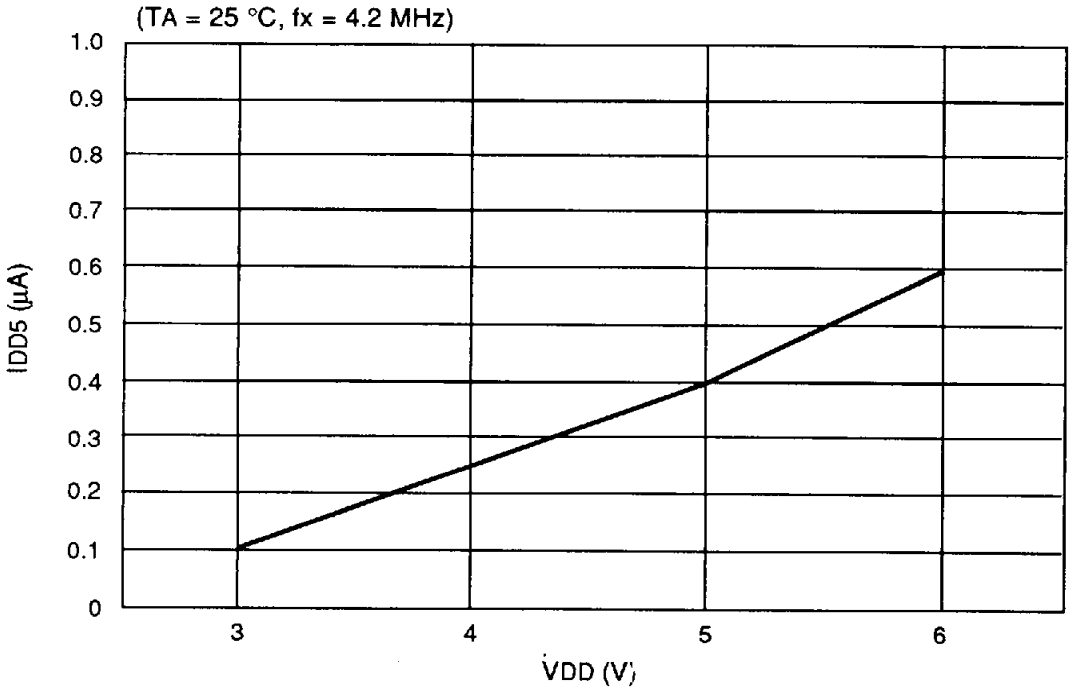


Figure 15–14. I_{DD5} vs. V_{DD}

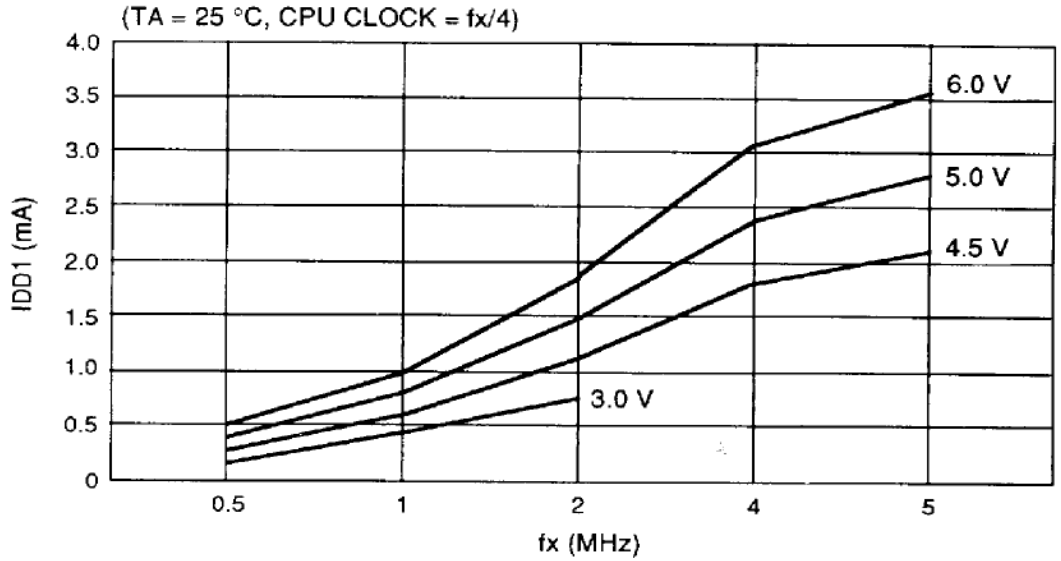
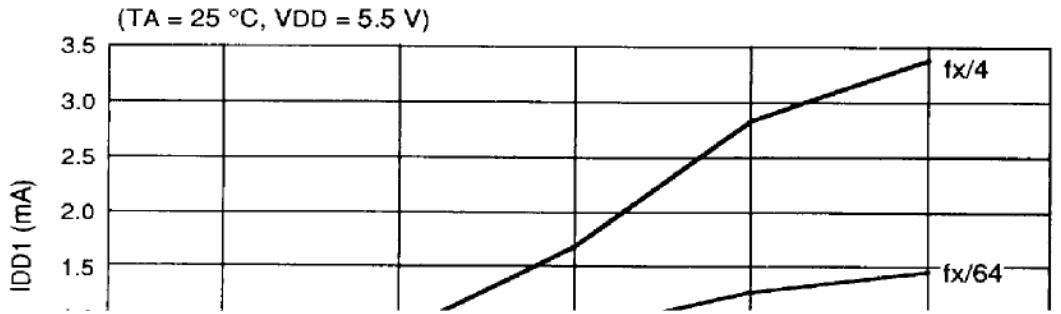


Figure 15–17. I_{DD1} vs. Frequency (fx)



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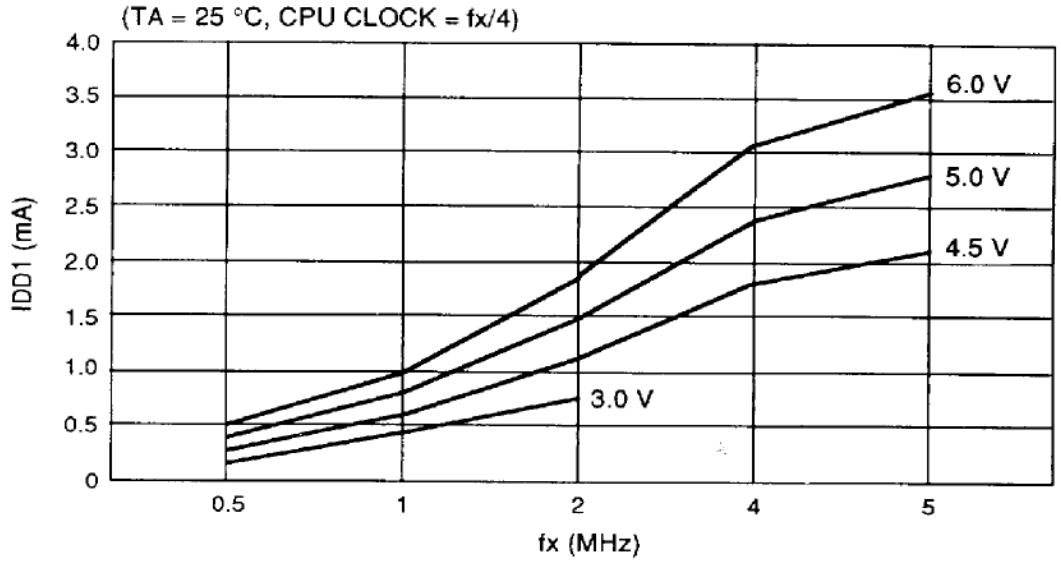
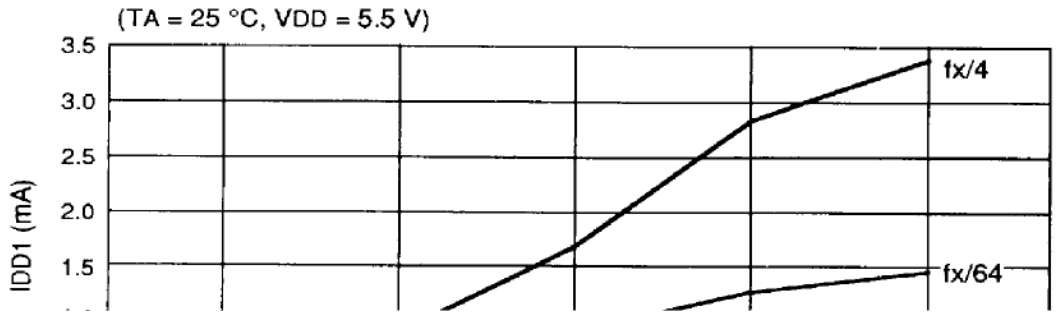


Figure 15–17. I_{DD1} vs. Frequency (fx)



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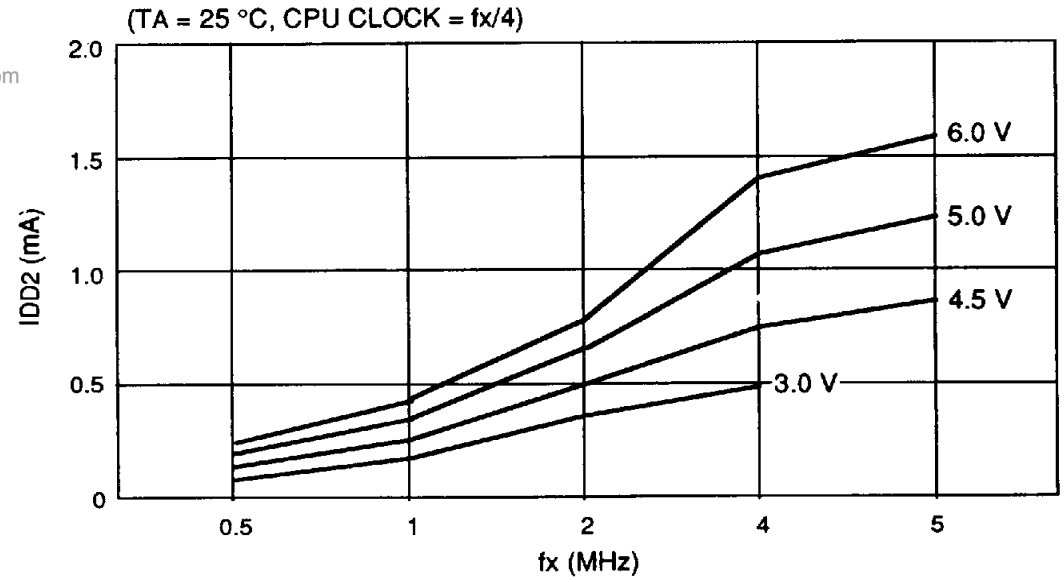

Figure 15–19. I_{DD2} vs. Frequency (fx)

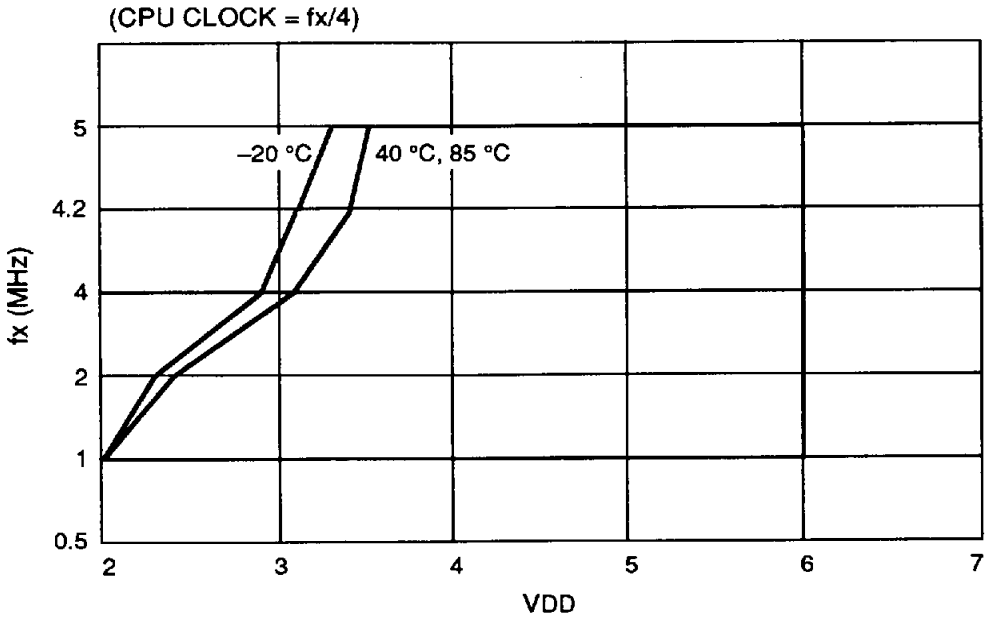

Figure 15–20. Frequency (fx) vs. V_{DD}

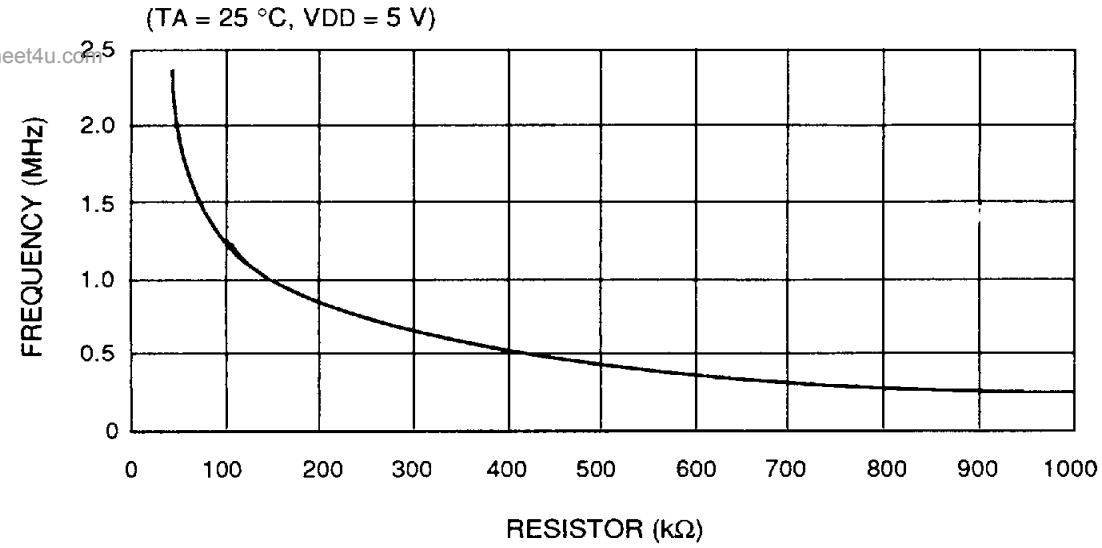

Figure 15–21. Frequency (fx) vs. Resistor