

**KS54AHCT 01**  
**KS74AHCT**

**Quad 2-Input NAND Gates with Open-Drain Outputs**

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

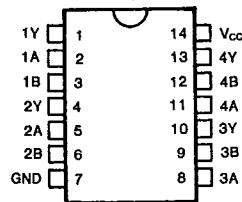
**DESCRIPTION**

These devices contain four independent 2-input NAND gates with open-drain outputs. Using a suitable pull-up resistor, these outputs may be connected to other open-drain outputs to implement wired-AND functions.

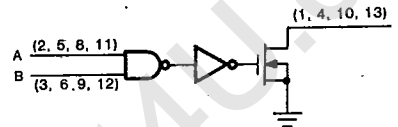
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



**LOGIC DIAGRAM**



**FUNCTION TABLE**

(Each Gate)

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H



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**Quad 2-Input NAND Gates  
with Open-Drain Outputs**

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$ , ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N):  $-12\text{mW}/^\circ\text{C}$  from  $65^\circ\text{C}$  to  $85^\circ\text{C}$   
 Ceramic Package (J):  $-12\text{mW}/^\circ\text{C}$  from  $100^\circ\text{C}$  to  $125^\circ\text{C}$

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  .. 0V to  $V_{CC}$   
 Operating Temperature  
 Range  
 KS74AHCT:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 KS54AHCT:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit
			Typ	KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$	
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O=20\mu\text{A}$ $I_O=4\text{mA}$ $I_O=8\text{mA}$	0 0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$
Maximum Output Leakage Current	$I_{OZ}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $V_{OUT}=V_{CC}$	$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.0	20.0	40.0	$\mu\text{A}$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I=2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$	2.7	2.9	3.0	mA

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT01

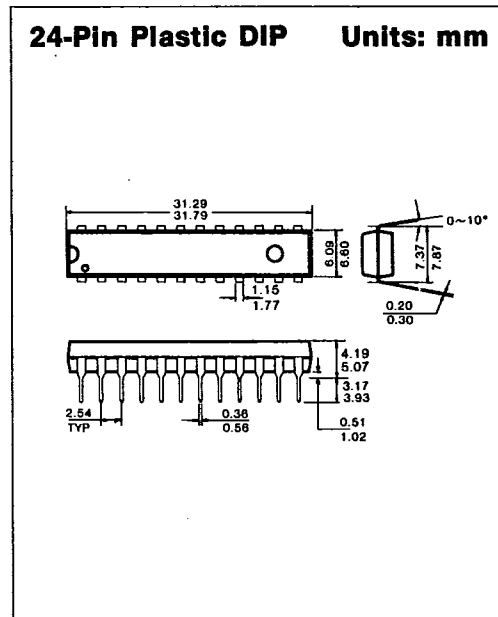
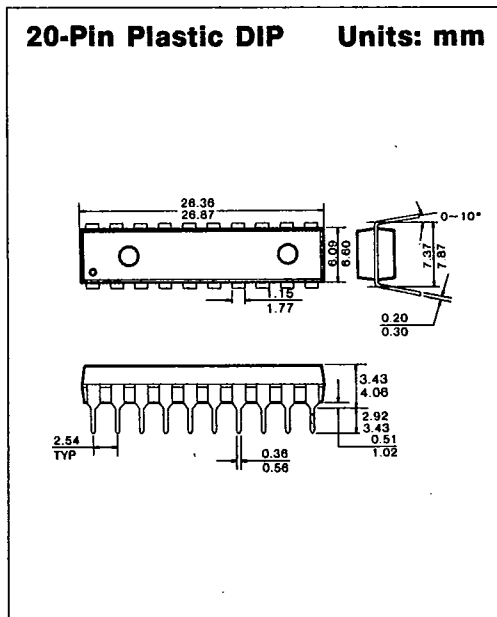
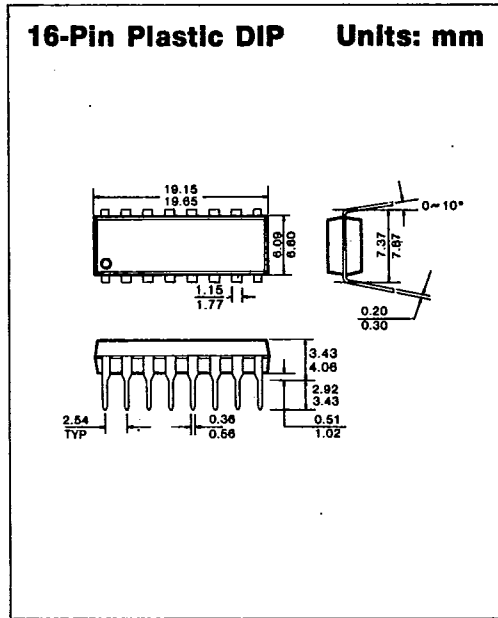
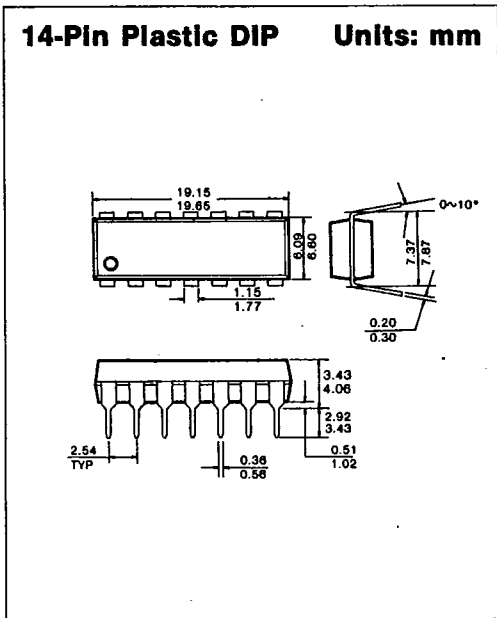
Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			$V_{CC}=5.0V$	Typ	Min	Max	Min	Max	
Propagation Delay	$t_{PLH}$	$C_L=50\text{pF}$ $R_L=1k\Omega$	17		25		29	ns	
	$t_{PHL}$		10		16		19		
Input Capacitance	$C_{IN}$		5					pF	
Power Dissipation Capacitance*	$C_{PD}$	(per gate)	15					pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .  
 † For AC switching test circuits and timing waveforms see section 2.

**PACKAGE DIMENSIONS**

T-90-20

**1. PLASTIC PACKAGES**



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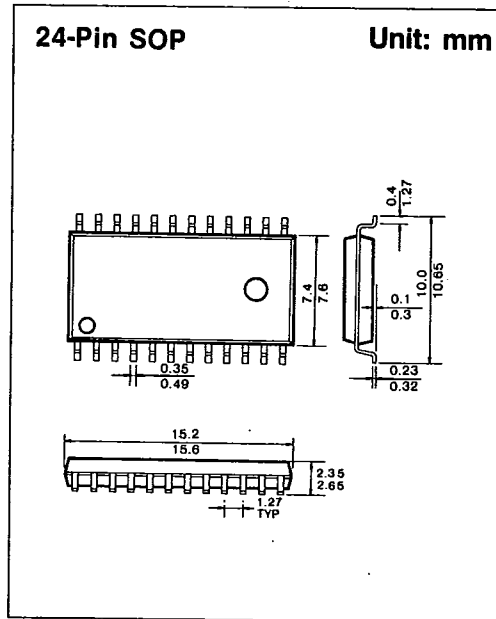
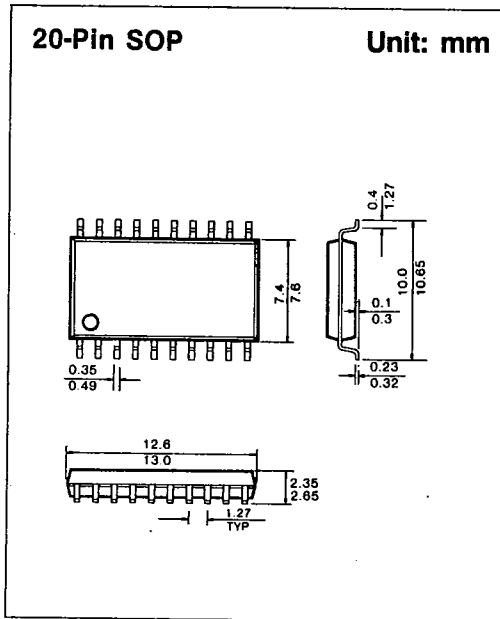
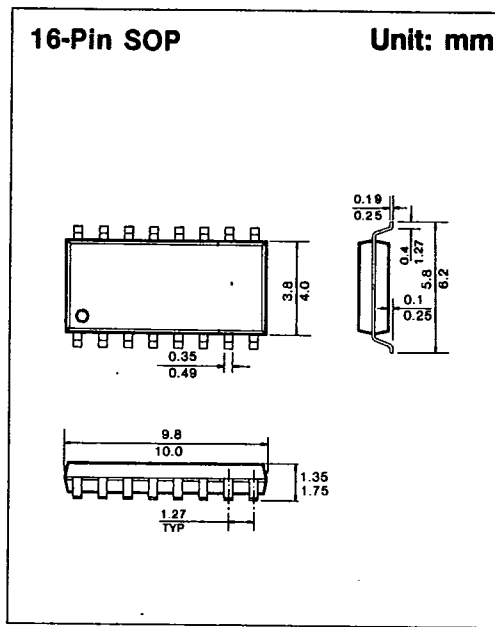
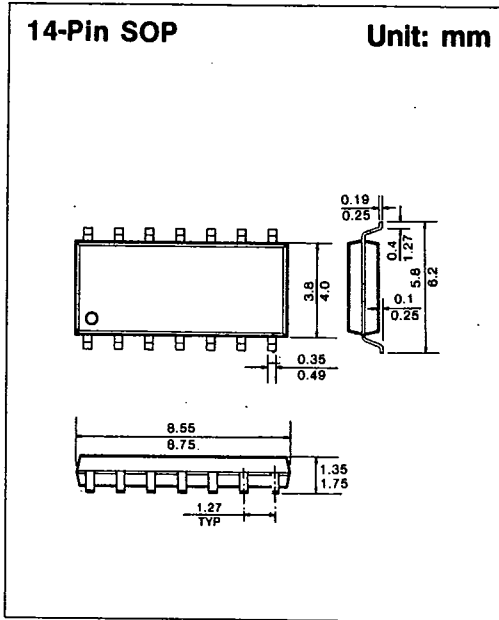
SAMSUNG SEMICONDUCTOR

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**PACKAGE DIMENSIONS**

T-90-20

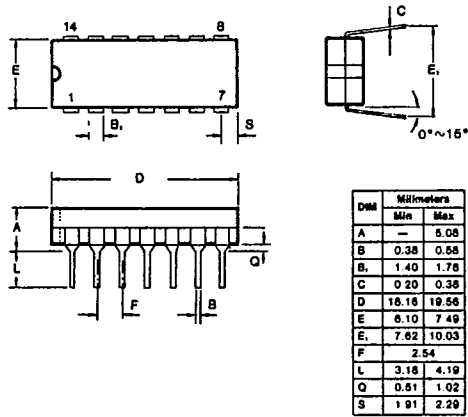


**PACKAGE DIMENSIONS**

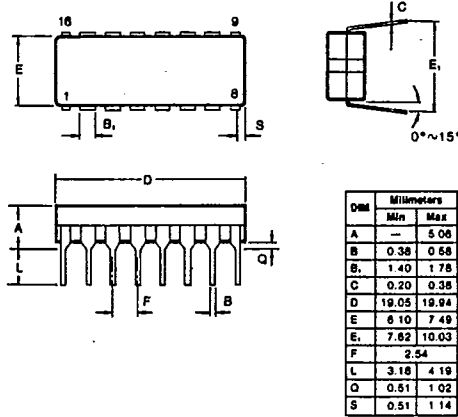
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**2. CERAMIC PACKAGES**

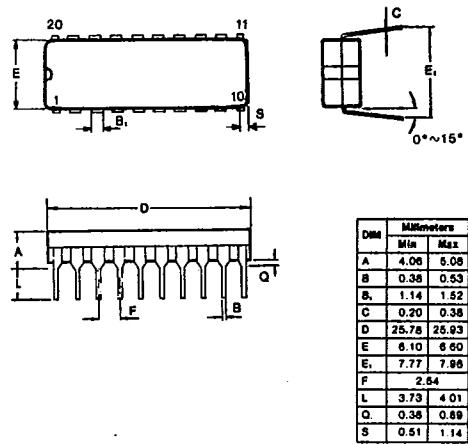
**14-Pin Ceramic DIP Units: mm**



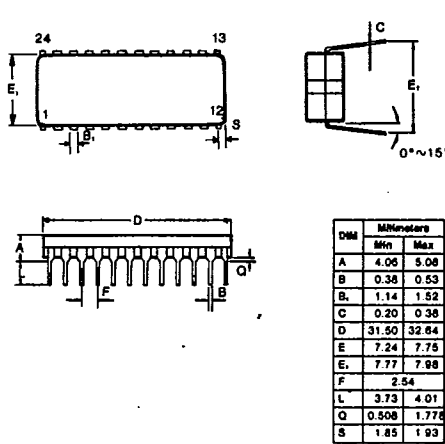
**16-Pin Ceramic DIP Units: mm**



**20-Pin Ceramic DIP Units: mm**



**24-Pin Ceramic DIP Units: mm**



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