KS54AHCT 132
KS74AHCT 132

Quad Schmitt-Trigger NAND Gates

Preliminary Specifications

FEATURES

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges: KS74AHCT: −40°C to +85°C KS54AHCT: −55°C to +125°C**
- **Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs**

DESCRIPTION

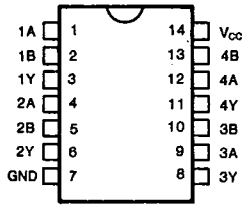
These Schmitt-trigger devices contain four independent NAND gates. They perform the Boolean function $Y = \overline{A \cdot B} = \bar{A} + \bar{B}$ in positive logic.

The input threshold levels are temperature compensated and can be triggered from the slowest of input ranges and still give jitter-free output signals.

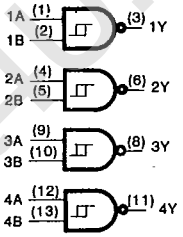
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

(Each Gate)

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

KS54AHCT 132 / KS74AHCT 132 — Quad Schmitt-Trigger NAND Gates

Absolute Maximum Ratings*

Supply Voltage Range V_{CC}, ... −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±35 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±125 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74AHCT T_a=−40°C to +85°C	KS54AHCT T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.11$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	T_a=25°C		KS74AHCT T_a=−40°C to +85°C		KS54AHCT T_a=−55°C to +125°C		Unit
			Min	Max	Min	Max	Min	Max	
Positive-Going Threshold Voltage	V_{T+}	V_{CC}=4.5V	1.2	1.9	1.2	1.9	1.2	1.9	V
		V_{CC}=5.5V	1.4	2.1	1.4	2.1	1.4	2.1	
Negative-Going Threshold Voltage	V_{T-}	V_{CC}=4.5V	0.5	1.2	0.5	1.2	0.5	1.2	V
		V_{CC}=5.5V	0.6	1.4	0.6	1.4	0.6	1.4	
Hysteresis (V_{T+}-V_{T-})	V_H	V_{CC}=4.5V	0.4	1.4	0.4	1.4	0.4	1.4	V
		V_{CC}=5.5V	0.4	1.5	0.4	1.5	0.4	1.5	

KS54AHCT 132 / KS74AHCT 132 — Quad Schmitt-Trigger NAND Gates

AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 2$ ns), AHCT132

Characteristic	Symbol	Conditions†	$T_a = 25°C$, $V_{CC} = 5.0V$	KS74AHCT $T_a = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$		KS54AHCT $T_a = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay, Any input to Y	t_{PLH}	$C_L = 50pF$	8		14		17	ns
	t_{PHL}		8		14		17	
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}	(per gate)	15					pF

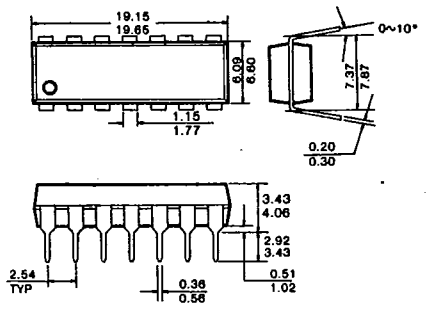
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

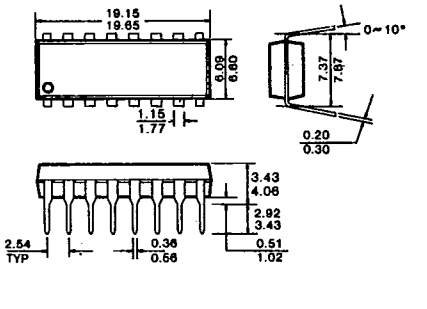
T-90-20

1. PLASTIC PACKAGES

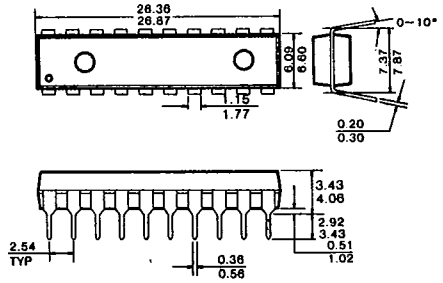
14-Pin Plastic DIP **Units: mm**



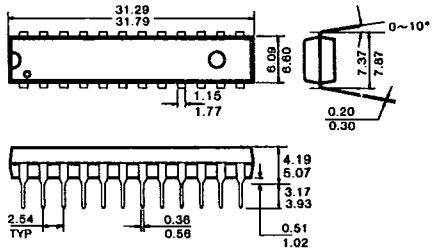
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



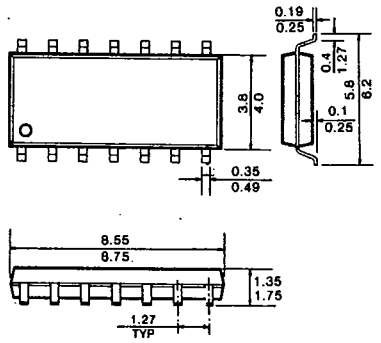
7

PACKAGE DIMENSIONS

T-90-20

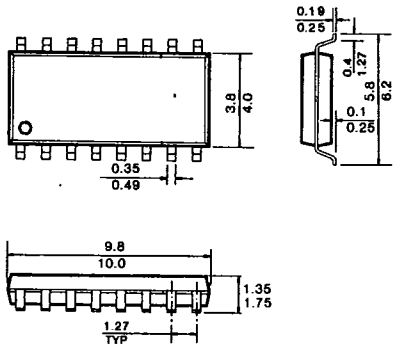
14-Pin SOP

Unit: mm



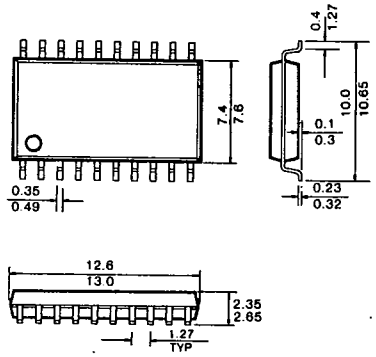
16-Pin SOP

Unit: mm



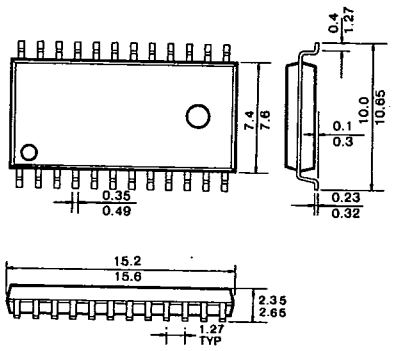
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

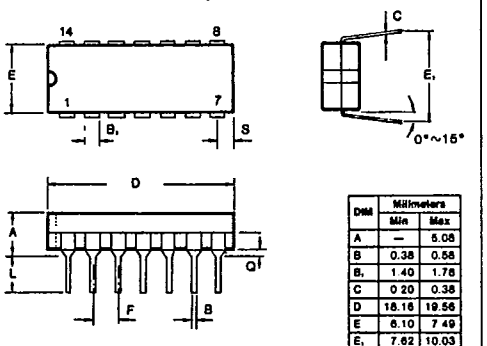


PACKAGE DIMENSIONS

T-90-20

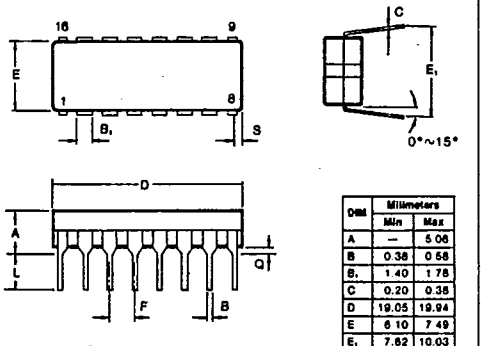
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



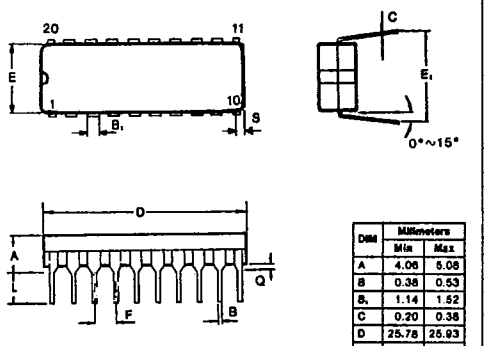
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



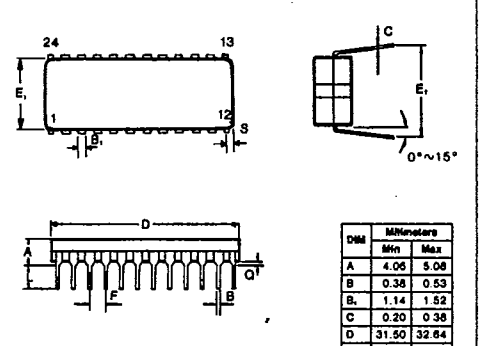
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.16	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

7