

KS54AHCT 259

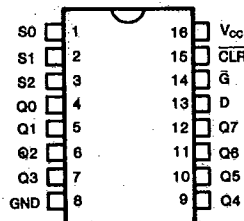
KS74AHCT

8-Bit Addressable Latches

FEATURES

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/Disable input simplifies expansion
- Expandable for N-bit applications
- Four distinct functional modes
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA}$ @ $V_{OL} = 0.5 \text{ V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^{\circ}\text{C}$
KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



FUNCTION TABLE

Inputs		Output of Addressed Latch	Each Other Output	Function
CLR	G			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

D = the level at the data input.

Q_{i0} = the level of Q_{i0} ($i = Q, 1, \dots, 7$, as appropriate) before the indicated steady-state input conditions were established.

DESCRIPTION

The '259 is a high-speed addressable latch designed for general purpose storage applications in digital systems. It can be used for implementing working registers, serial-holding registers and active-high decoders or demultiplexers.

The '259 has four distinct modes of operation that are selected via the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs: 1) addressable latch; 2) memory; 3) active-high eight-channel demultiplexer; and 4) clear.

In the addressable latch mode, data on the data input (D) is written into the addressed latch. In this mode, data will be written into the addressed latch with all non-addressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous state and are unaffected by the data of address inputs.

In the demultiplexing mode, addressed outputs will follow the state of the D input and all other outputs will remain low.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{cc} and ground.

LATCH SELECTION TABLE

Select Inputs			Latch Addressed
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7



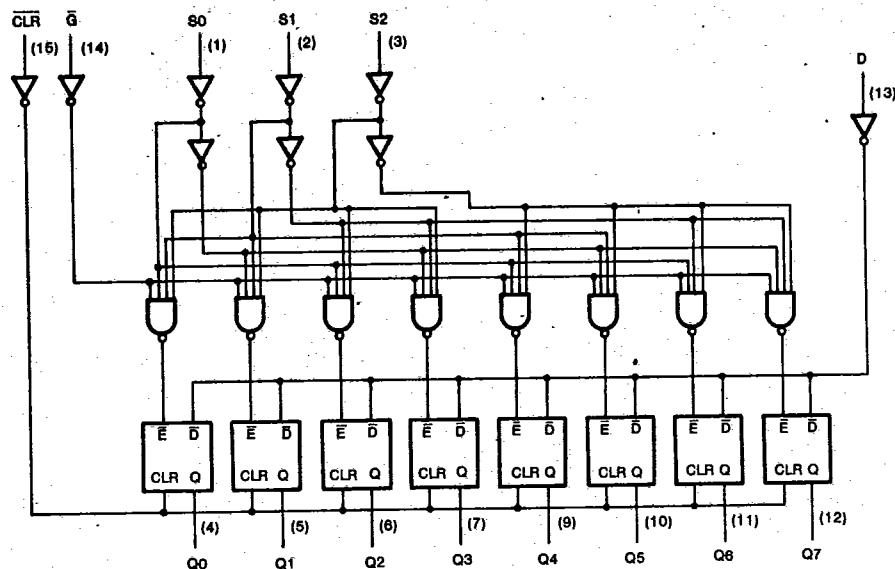
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8-Bit Addressable Latches

T-46-07-05

LOGIC DIAGRAM

**Absolute Maximum Ratings***

Supply Voltage Range V_{CC} , -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{stg} -65°C to $+150^\circ\text{C}$
 Power Dissipation Per Package, P_d [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): $-12\text{mW}/^\circ\text{C}$ from 65°C to 85°C
 Ceramic Package (J): $-12\text{mW}/^\circ\text{C}$ from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature

Range KS74AHCT: -40°C to $+85^\circ\text{C}$
 KS54AHCT: -55°C to $+125^\circ\text{C}$

Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

KS54AHCT
KS74AHCT **259**
8-Bit Addressable Latches**DC ELECTRICAL CHARACTERISTICS** ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT	Unit	
					T _a = -40°C to +85°C	T _a = -55°C to +125°C		
			Typ				Guaranteed Limits	
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	V	
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA	
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μA	
Additional Worst Case Supply Current	ΔI _{CC}	per input pin V _I =2.4V other inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA	

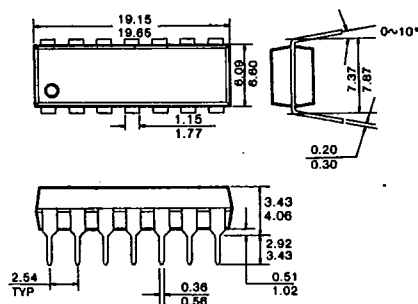
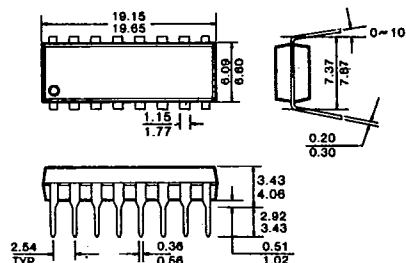
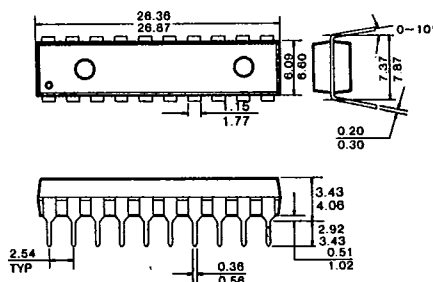
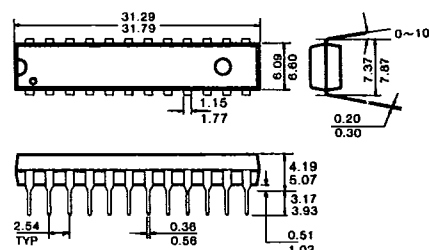
AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2\text{ ns}$, AHCT259)

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC}=5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC}=5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay CLR to any Q	t_{PHL}	$C_L=50\text{pF}$	9		15		18	ns
Propagation Delay, Data to any Q	t_{PLH}		12		19		23	ns
	t_{PHL}		12		19		23	
Propagation Delay, Address to any Q	t_{PLH}		13		22		27	ns
	t_{PHL}		13		22		27	
Propagation Delay, G to any Q	t_{PLH}		12		20		24	ns
	t_{PHL}		12		20		24	
Pulse Width	CLR Low	t_w	6	10		10		ns
	G Low		9	15		20		
Setup Time Data or Address before $\bar{G}t$	t_{su}		10	15		20		ns
Hold Time, Data or Address before $\bar{G}t$	t_h		-3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Power Dissipation Capacitance*	C_{PD}		80					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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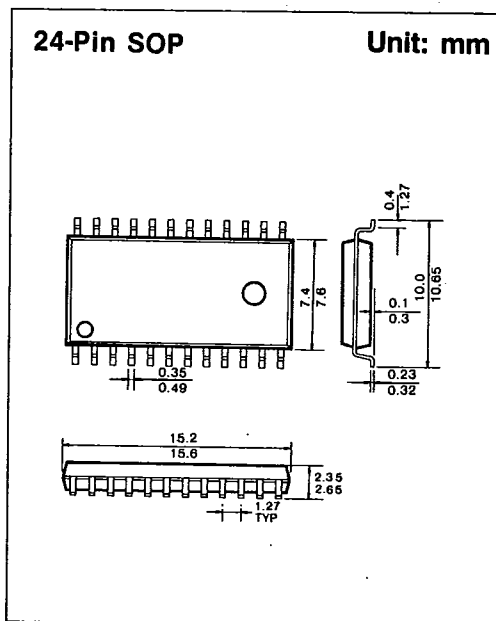
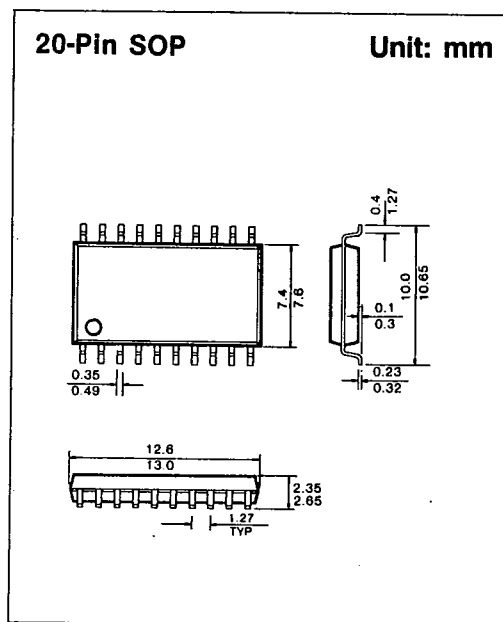
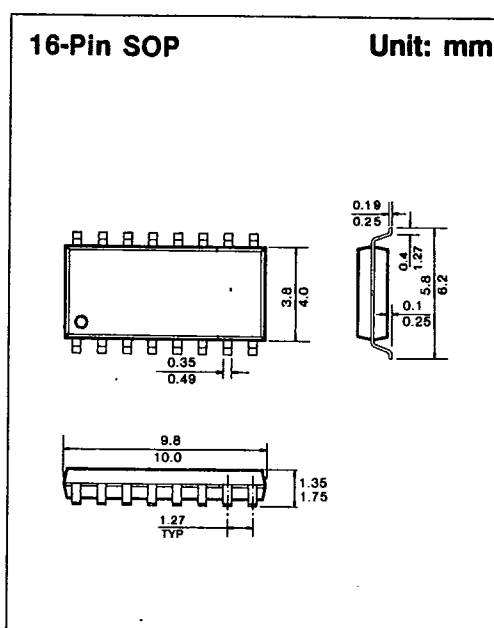
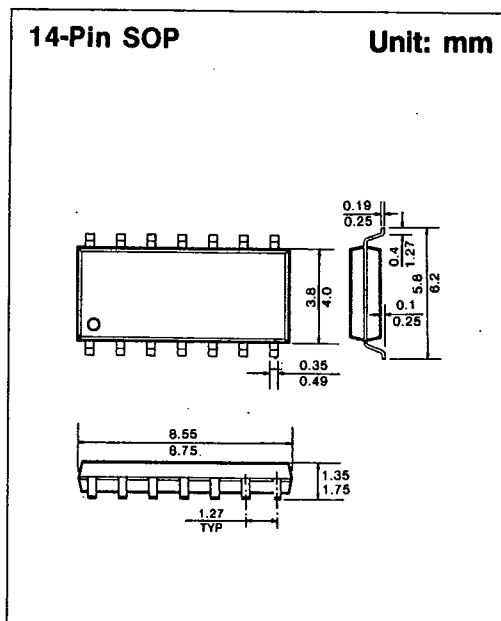
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PACKAGE DIMENSIONS

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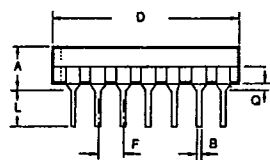
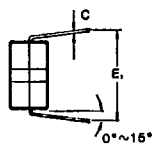
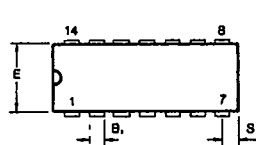
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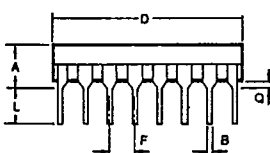
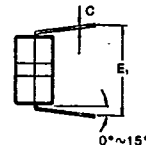
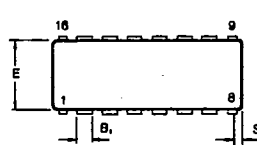
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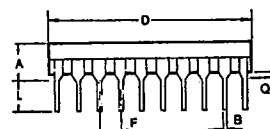
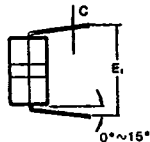
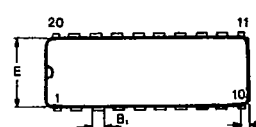
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2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

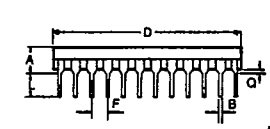
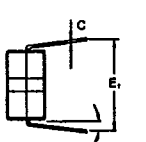
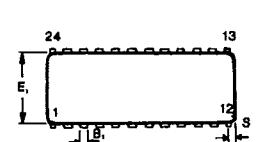
Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93

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