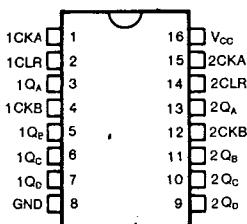


**KS54AHCT 390
KS74AHCT****Dual 4-Bit Decade Counters****FEATURES**

- Individual clock for A and B flip-flops provide dual + 2 and + 5 counters
- Direct clear for each 4-bit counter
- Significant improvement in system density through reduced counter package count.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
($I_{OL} = 8 \text{ mA}$ @ $V_{OL} = 0.5\text{V}$)
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74HCTLs: -40°C to +85°C
KS54HCTLs: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION**FUNCTION TABLES**

**BCD COUNT SEQUENCE
(EACH COUNTER)**
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**BIQUINARY (5-2)
(EACH COUNTER)**
(See Note B)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES A. Output Q_A is connected to input CKB for BCD count.

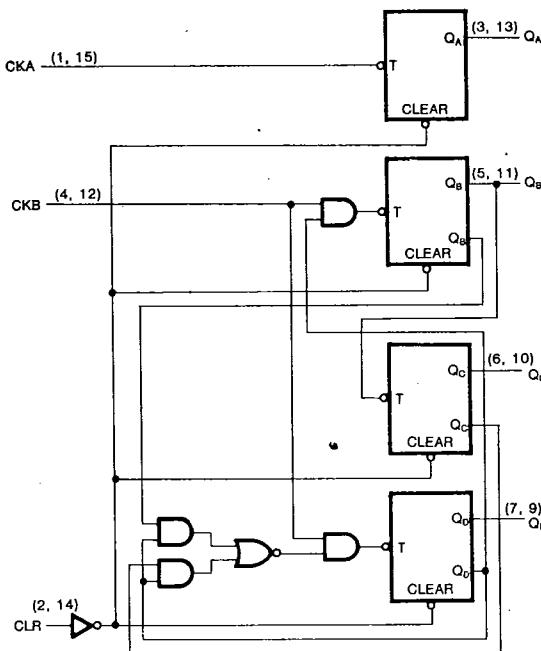
B. Output Q_D is connected to input CKA for biquinary count.



SAMSUNG SEMICONDUCTOR

KS54AHCT 390**Dual 4-Bit Decade Counters**

T-45-23-13

LOGIC DIAGRAM**Absolute Maximum Ratings***

Supply Voltage Range Vcc, -0.5V to +7V
DC Input Diode Current, I_{ik} (V_i < -0.5V or V_i > Vcc +0.5V) ±20 mA

DC Output Diode Current, I_{ok} (V_o < -0.5V or V_o > Vcc +0.5V) ±20 mA
Continuous Output Current Per Pin, I_o (-0.5V < V_o < Vcc +0.5V) ±35 mA

Continuous Current Through Vcc or GND pins ±125 mA
Storage Temperature Range, T_{stg} -65°C to +150°C

Power Dissipation Per Package, P_d[†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, Vcc 4.5V to 5.5V

DC Input & Output Voltages*, V_{IN}, V_{OUT} .. 0V to Vcc

Operating Temperature

Range	KS74AHCT: -40°C to +85°C
	KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either Vcc or GND)



SAMSUNG SEMICONDUCTOR

**KS54AHCT 390
KS74AHCT****Dual 4-Bit Decade Counters
T-45-23-13****DC ELECTRICAL CHARACTERISTICS** ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$		KS74AHCT		KS54AHCT		Unit
			Typ		$T_a = -40^\circ C$ to $+85^\circ C$	$V_{CC} = 5.0V \pm 10\%$	$T_a = -55^\circ C$ to $+125^\circ C$	$V_{CC} = 5.0V \pm 10\%$	
Minimum High-Level Input Voltage	V_{IH}			2.0		2.0		2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8		0.8		0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-4mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84		$V_{CC}-0.1$ 3.7		V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$ or V_{IH} $I_O=20\mu A$ $I_O=4mA$ $I_O=8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5		0.1 0.4		V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1		± 1.0		± 1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0		80.0		160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leq 2$ ns), AHCT390

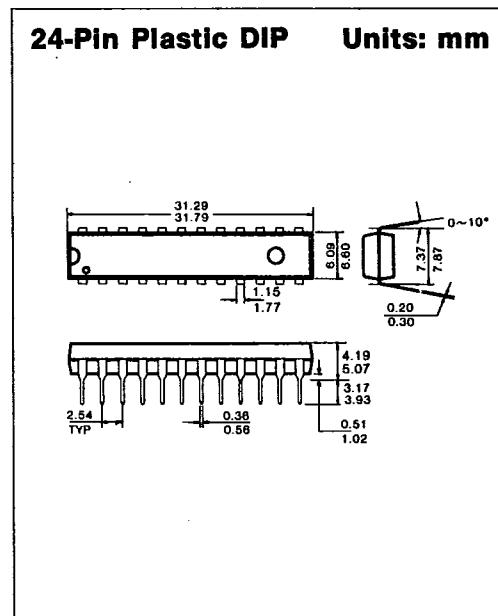
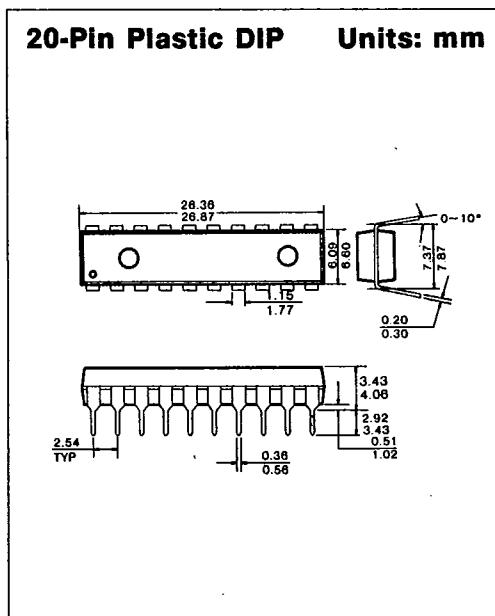
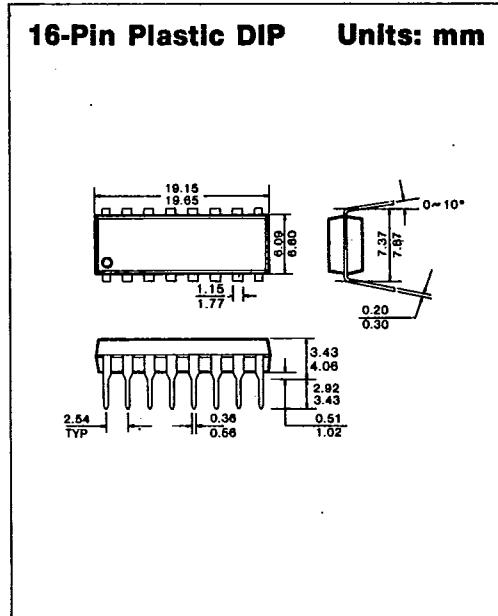
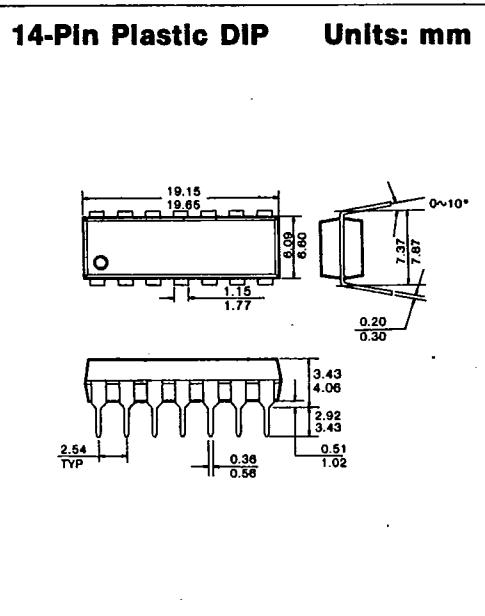
Characteristic	Symbol	Conditions [†]	KS74AHCT			KS54AHCT			Unit
			Typ	Min	Max	Min	Max		
Propagation Delay, CKA to Q _A or CKB to Q _B	t_{PLH}		50	30		25			MHz
Propagation Delay, CKA to Q _A	t_{PHL}		9		15		18		ns
Propagation Delay, CKA to Q _C	t_{PLH}	$C_L=50pF$	9		15		18		ns
Propagation Delay, CKA to Q _C	t_{PHL}		24		40		48		ns
Propagation Delay, CKB to Q _B	t_{PLH}		24		40		48		ns
Propagation Delay, CKB to Q _B	t_{PHL}		10		17		21		ns
Propagation Delay, CKB to Q _C	t_{PLH}		10		17		21		ns
Propagation Delay, CKB to Q _C	t_{PHL}		16		27		33		ns
Propagation Delay, CKB to Q _D	t_{PLH}		16		27		33		ns
Propagation Delay, CKB to Q _D	t_{PHL}		10		17		21		ns
Propagation Delay, CLR to Any Q	t_{PHL}		10		17		21		ns
Pulse Width	CKA or CKB High or Low CLR High	t_w		7	12		15		ns
Minimum Setup Time, CLR inactive before CKA or CKB	t_{SU}			7	12		15		ns
Input Capacitance	C_{IN}			5					pF
Power Dissipation Capacitance	C_{PD}			5					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D=C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.



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PACKAGE DIMENSIONST-90-20**1. PLASTIC PACKAGES**

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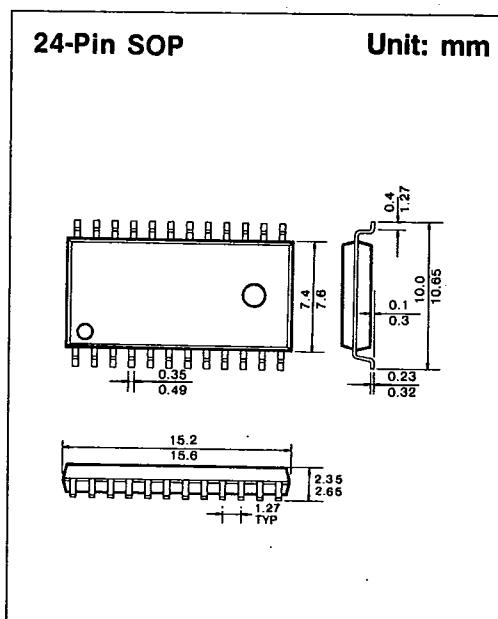
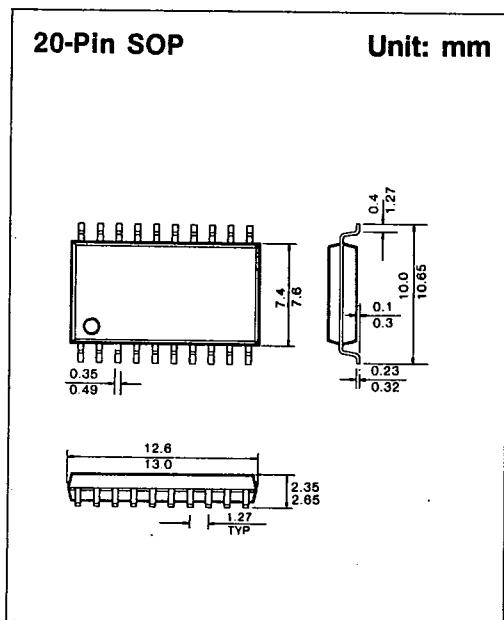
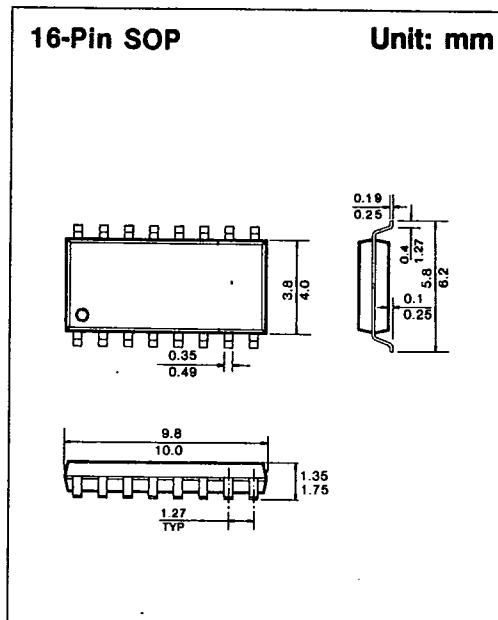
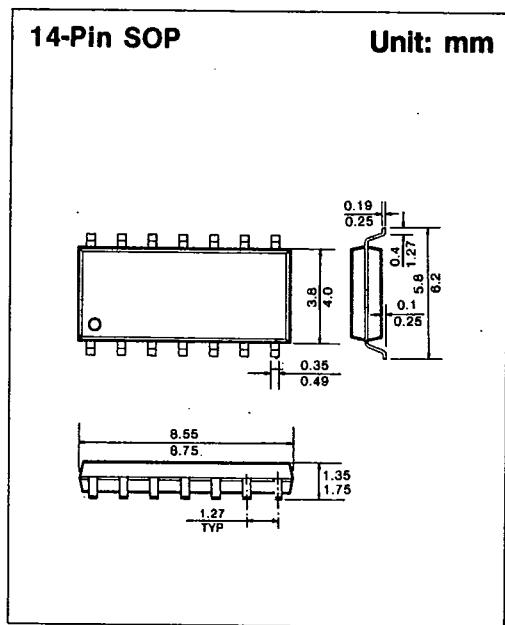


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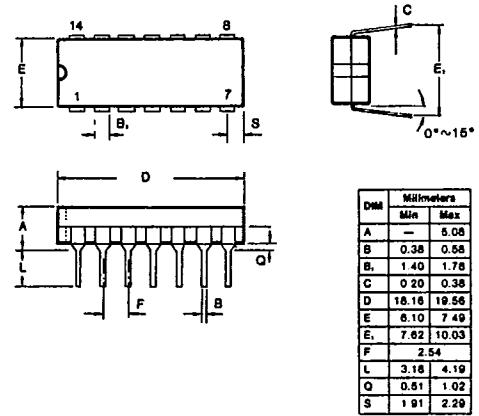
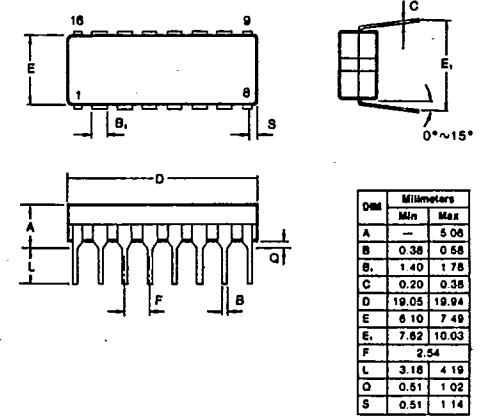
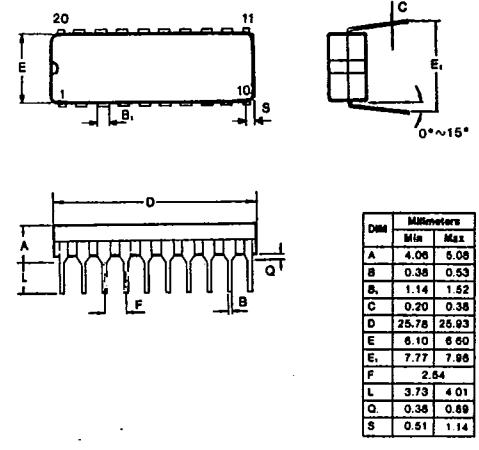
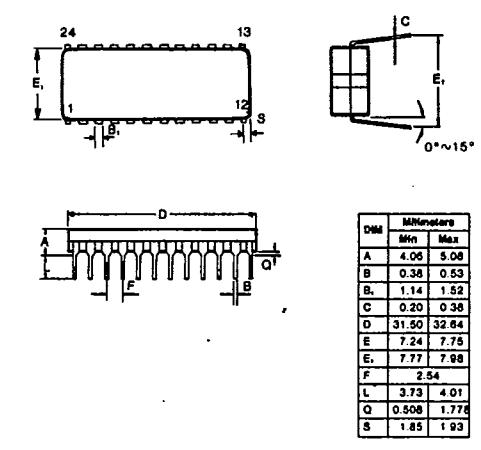
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PACKAGE DIMENSIONS**T-90-20****SAMSUNG SEMICONDUCTOR**

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PACKAGE DIMENSIONST-90-20**2. CERAMIC PACKAGES****14-Pin Ceramic DIP Units: mm****16-Pin Ceramic DIP Units: mm****20-Pin Ceramic DIP Units: mm****24-Pin Ceramic DIP Units: mm**

7



SAMSUNG SEMICONDUCTOR

1677

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783