

**KS54AHCT 51/58**  
**KS74AHCT**

**Dual AND-OR-Invert Gates**  
**and Dual AND-OR Gates**

**FEATURES**

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:  
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
 KS74AHCT:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 KS54AHCT:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

**DESCRIPTION**

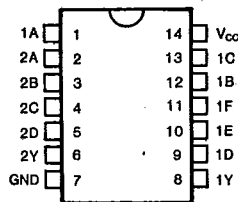
The '51 performs the following Boolean functions:  
 $1Y = (\overline{1A} \cdot \overline{1B} \cdot 1C) + (1D \cdot \overline{1E} \cdot \overline{1F})$   
 $2Y = (2A \cdot 2B) + (2C \cdot 2D)$

The '58 performs:  
 $1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$   
 $2Y = (2A \cdot 2B) + (2C \cdot 2D)$

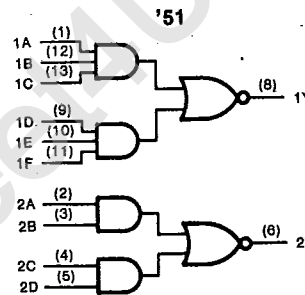
These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

**PIN CONFIGURATION**



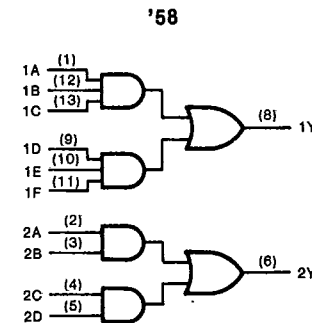
**LOGIC DIAGRAMS**



**FUNCTION TABLES**

| Inputs                |    |    |    |    |    | Output 1Y |     |
|-----------------------|----|----|----|----|----|-----------|-----|
| 1A                    | 1B | 1C | 1D | 1E | 1F | '51       | '58 |
| H                     | H  | H  | X  | X  | X  | L         | H   |
| X                     | X  | X  | H  | H  | H  | L         | H   |
| Any other combination |    |    |    |    |    | H         | L   |

| Inputs                |    |    |    | Output 2Y |     |
|-----------------------|----|----|----|-----------|-----|
| 2A                    | 2B | 2C | 2D | '51       | '58 |
| H                     | H  | X  | X  | L         | H   |
| X                     | X  | H  | H  | L         | H   |
| Any other combination |    |    |    | H         | L   |



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**Dual AND-OR-Invert Gates**  
**and Dual AND-OR Gates**

**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 35$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 125$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -65°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature

Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns

\* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

| Characteristic                       | Symbol          | Test Conditions  | $T_a = 25^\circ C$ |  |   | Unit                  |         |
|--------------------------------------|-----------------|--|--------------------|--|---|-----------------------|---------|
|                                      |                 |  | Typ                | KS74AHCT<br>$T_a = -40^\circ C$ to $+85^\circ C$ | KS54AHCT<br>$T_a = -55^\circ C$ to $+125^\circ C$ |                       |         |
| Minimum High-Level Input Voltage     | $V_{IH}$        |  | 2.0                | 2.0  | 2.0   | V                     |         |
| Maximum Low-Level Input Voltage      | $V_{IL}$        |  | 0.8                | 0.8  | 0.8   | V                     |         |
| Minimum High-Level Output Voltage    | $V_{OH}$        | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O = -20\mu A$<br>$I_O = -4mA$                          | $V_{CC}$<br>4.2    | $V_{CC} - 0.1$<br>3.98                           | $V_{CC} - 0.1$<br>3.84                            | $V_{CC} - 0.1$<br>3.7 | V       |
| Maximum Low-Level Output Voltage     | $V_{OL}$        | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O = 20\mu A$<br>$I_O = 4mA$<br>$I_O = 8mA$             | 0                  | 0.1<br>0.26<br>0.39                              | 0.1<br>0.33<br>0.5                                | 0.1<br>0.4            | V       |
| Maximum Input Current                | $I_{IN}$        | $V_{IN}=V_{CC}$ or GND   |                    | $\pm 0.1$  | $\pm 1.0$   | $\pm 1.0$             | $\mu A$ |
| Maximum Quiescent Supply Current     | $I_{CC}$        | $V_{IN}=V_{CC}$ or GND<br>$I_{OUT}=0\mu A$   |                    | 2.0  | 20.0  | 40.0                  | $\mu A$ |
| Additional Worst Case Supply Current | $\Delta I_{CC}$ | per input pin<br>$V_I = 2.4V$<br>other inputs:<br>at $V_{CC}$ or GND<br>$I_{OUT}=0\mu A$ |                    | 2.7  | 2.9   | 3.0                   | mA      |

**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r$ ,  $t_f \leq 2$  ns), AHCT51, AHCT58

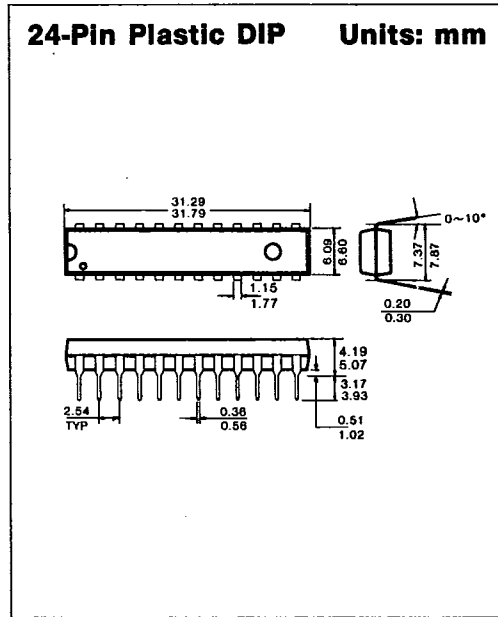
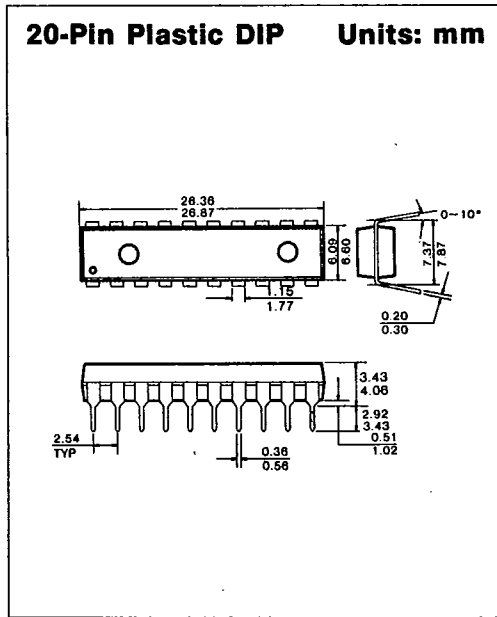
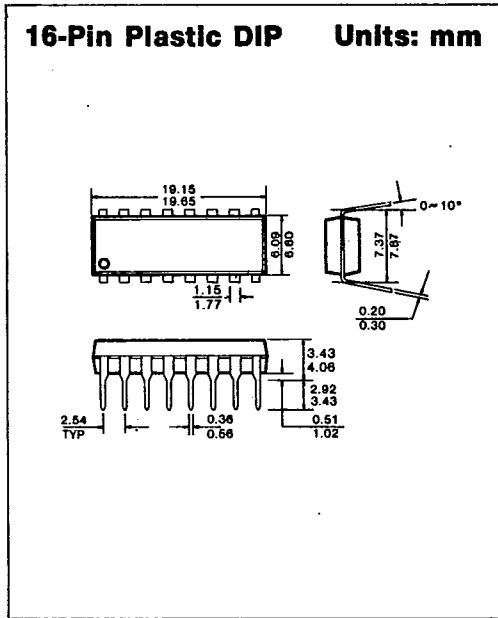
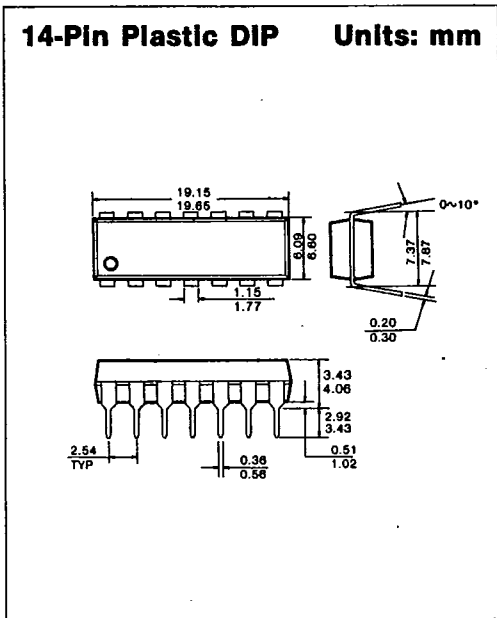
| Characteristic                 | Symbol    | Conditions†  | $T_a = 25^\circ C$ |     | KS74AHCT<br>$T_a = -40^\circ C$ to $+85^\circ C$ |     | KS54AHCT<br>$T_a = -55^\circ C$ to $+125^\circ C$ |     | Unit |
|--------------------------------|-----------|--------------|--------------------|-----|--|-----|---|-----|------|
|                                |           |              | Typ                | Max | Min  | Max | Min   | Max |      |
| Propagation Delay              | $t_{PLH}$ | $C_L = 50pF$ | 9                  | 15  |  |     | 18  | ns  |      |
|                                | $t_{PHL}$ |              | 9                  | 15  |  |     | 18  |     |      |
| Input Capacitance              | $C_{IN}$  |              | 5                  | #   |  |     |   | pF  |      |
| Power Dissipation Capacitance* | $C_{PD}$  | (per gate)   | 15                 |     |  |     |   | pF  |      |

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .  
 † For AC switching test circuits and timing waveforms see section 2.

**PACKAGE DIMENSIONS**

T-90-20

**1. PLASTIC PACKAGES**



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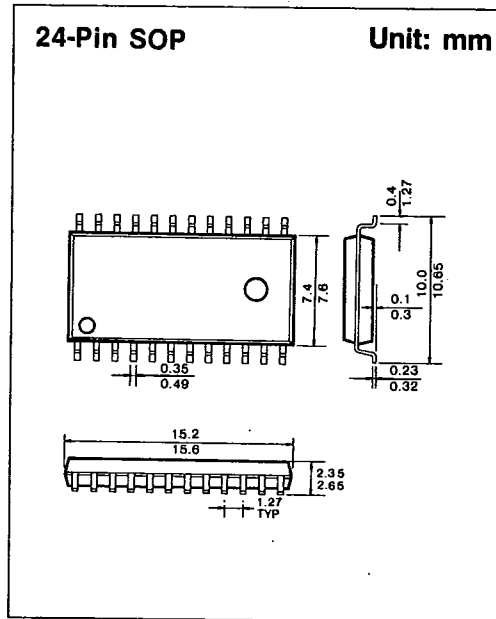
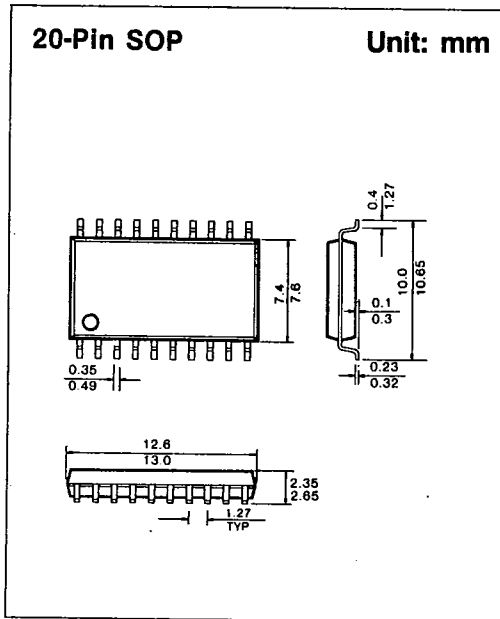
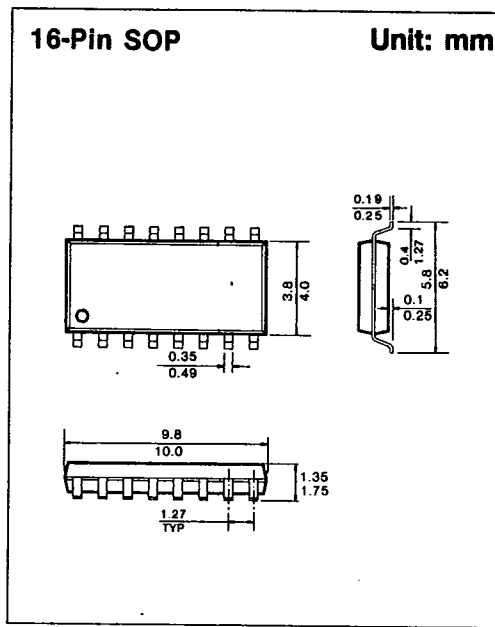
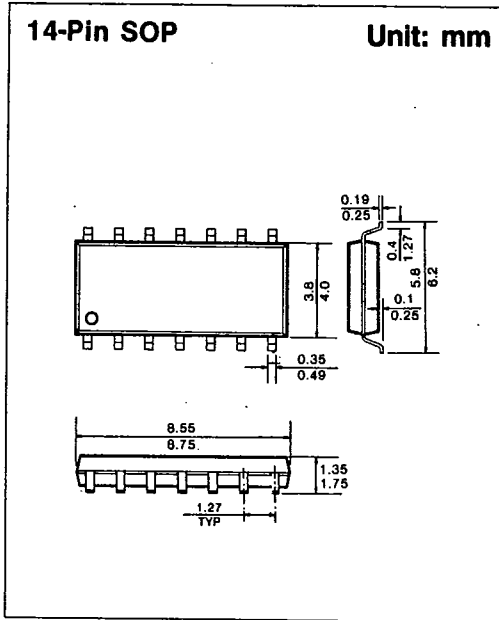
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**PACKAGE DIMENSIONS**

T-90-20

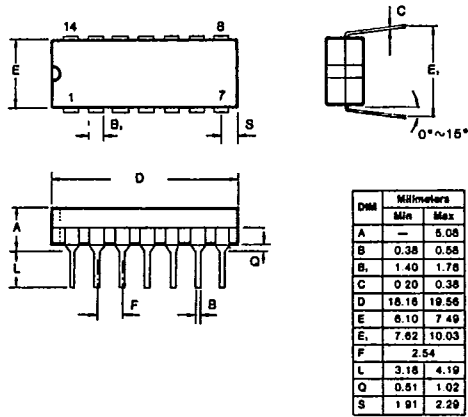


**PACKAGE DIMENSIONS**

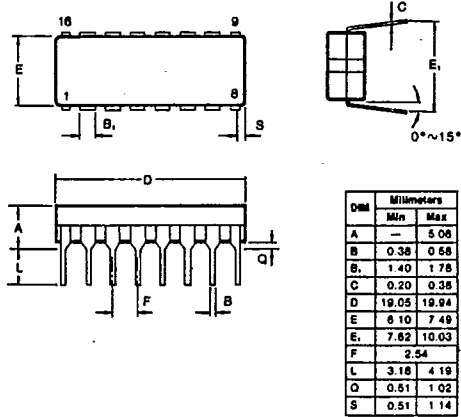
T-90-20

**2. CERAMIC PACKAGES**

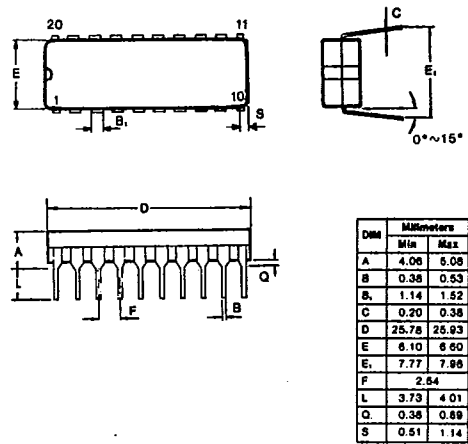
**14-Pin Ceramic DIP Units: mm**



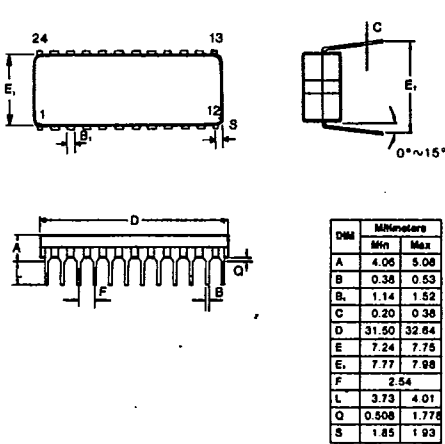
**16-Pin Ceramic DIP Units: mm**



**20-Pin Ceramic DIP Units: mm**



**24-Pin Ceramic DIP Units: mm**



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