

# KS54AHCT 590/591 KS74AHCT

## 8-Bit Binary Counters with Output Registers

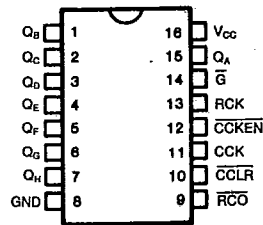
Preliminary Specifications

T-45-23-17

### FEATURES

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current (I<sub>OL</sub> = 24 mA @ V<sub>OL</sub> = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:  
KS74AHCT: -40°C to +85°C  
KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

### PIN CONFIGURATION



### DESCRIPTION

These devices each consist of an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, CCKEN, is low. When the counter increments to the all ones condition, ripple carry out, RCO, will go low. This enables either synchronous cascading of the counters by connecting the RCO of the first stage to the CCKEN of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G-bar, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

### FUNCTION TABLE

G-bar	INPUTS				FUNCTION
	RCK	CCLR	CCKEN	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L		X	X	X	Counter data is stored into register
L		X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L		Advance one count
L	X	H	L		No count
L	X	H	H	X	No count

X: Don't care

$$RCO = Q_A' \cdot Q_B' \cdot Q_C' \cdot Q_D' \cdot Q_E' \cdot Q_F' \cdot Q_G' \cdot Q_H'$$

(Q<sub>A</sub>' ~ Q<sub>H</sub>': Internal outputs of the counter)

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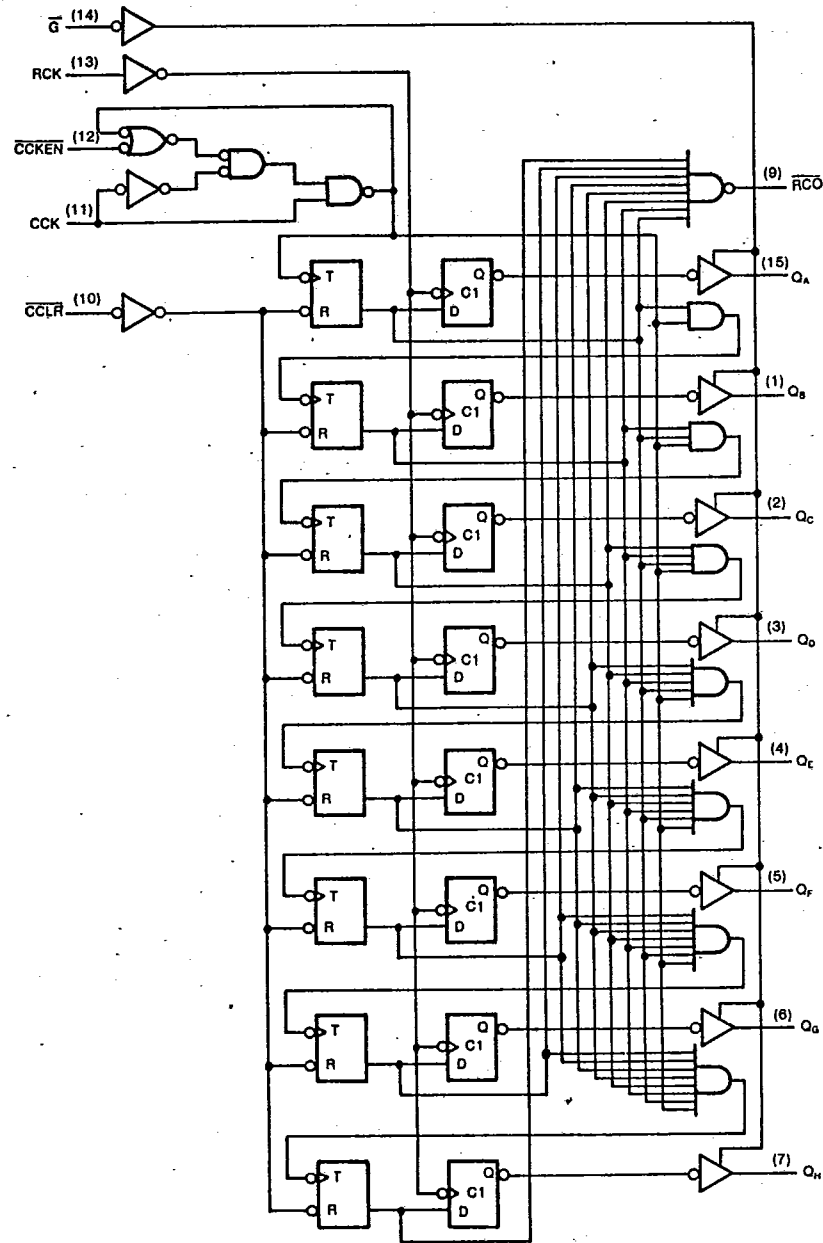
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**LOGIC DIAGRAM**



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**Absolute Maximum Ratings\***

Supply Voltage Range  $V_{CC}$  ..... -0.5V to +7V  
 DC Input Diode Current,  $I_{IK}$   
 ( $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 DC Output Diode Current,  $I_{OK}$   
 ( $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20$  mA  
 Continuous Output Current Per Pin,  $I_O$   
 ( $-0.5V < V_O < V_{CC} + 0.5V$ ) .....  $\pm 70$  mA  
 Continuous Current Through  
 $V_{CC}$  or GND pins .....  $\pm 250$  mA  
 Storage Temperature Range,  $T_{stg}$  ..... -85°C to +150°C  
 Power Dissipation Per Package,  $P_d$ † ..... 500 mW

\* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:  
 Plastic Package (N): -12mW/°C from 65°C to 85°C  
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

**Recommended Operating Conditions**

Supply Voltage,  $V_{CC}$  ..... 4.5V to 5.5V  
 DC Input & Output Voltages\*,  $V_{IN}$ ,  $V_{OUT}$  ... 0V to  $V_{CC}$   
 Operating Temperature  
 Range KS74AHCT: -40°C to +85°C  
 KS54AHCT: -55°C to +125°C  
 Input Rise & Fall Times,  $t_r$ ,  $t_f$  ..... Max 500 ns  
 \* Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{CC}$  or GND)

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 10\%$  Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		Guaranteed Limits
Minimum High-Level Input Voltage	$V_{IH}$		2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	$V_{IL}$		0.8	0.8	0.8	V	
Minimum High-Level Output Voltage (All '590 Outputs and '591 RCO Output)	$V_{OH}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = -20\mu A$ $I_O = -6mA$	$V_{CC}$ 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	$V_{OL}$	$V_{IN}=V_{IH}$ or $V_{IL}$ $I_O = 20\mu A$ $I_O = 12mA$ $I_O = 24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	$I_{IN}$	$V_{IN}=V_{CC}$ or GND		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
Maximum Output Leakage Current	$I_{OZ}$	Output Enable = $V_{IH}$ $V_{OUT}=V_{CC}$		$\pm 0.5$	$\pm 5.0$	$\pm 10.0$	$\mu A$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	$\mu A$
Additional Worst Case Supply Current	$\Delta I_{CC}$	per input pin $V_I = 2.4V$ other inputs: at $V_{CC}$ or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA



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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT590

Characteristic	Symbol	Conditions†	54/74AHT	KS74AHT		54AHT		Unit	
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$ Typical	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$			
Maximum Clock Frequency	$f_{max}$		50	30		25		ns	
Propagation Delay, CCK† to RCO	$t_{PLH}$	$C_L = 50\text{pF}$	15		25		29	ns	
	$t_{PHL}$		15		25		29		
Propagation Delay, CCLR‡ to RCO	$t_{PHL}$		17		28		33	ns	
Propagation Delay, RCK† to Q	$t_{PLH}$		10		16		19	ns	
	$t_{PHL}$		10		16		19		
Output Enable Time, $\bar{G}$ † to Q	$t_{PZH}$		$C_L = 50\text{pF}$ $R_L = 1\text{K}\Omega$	13		18		22	ns
	$t_{PZL}$	13			18		22		
Output Disable Time, $\bar{G}$ † to Q	$t_{PHZ}$	13			18		22	ns	
	$t_{PLZ}$	13			18		22		
Pulse Duration	CCK or RCK High or Low	$t_w$		10	15		20		ns
	CCLR Low			10	15		20		
Setup Time	CCKEN‡ before CCK†	$t_{su}$	10	15		20		ns	
	CCLR‡ before CCK†		6	10		10			
	CCK† to RCK†††		15	20		25			
Input Capacitance	$C_{IN}$		5					pF	
Output Capacitance (Q Outputs)	$C_{OUT}$	Output Disabled	10					pF	
Power Dissipation Capacitance*	$C_{PD}$							pF	

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

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**AC ELECTRICAL CHARACTERISTICS** (Input  $t_r, t_f \leq 2$  ns), AHCT591

Characteristic	Symbol	Conditions†	54/74AHCT	KS74AHCT		54AHCT		Unit
			$T_a = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$ Typical	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ Min Max		$T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ Min Max		
Maximum Clock Frequency	$f_{max}$	$C_L = 50\text{pF}$ $R_L = 1\text{k}\Omega$	50	30		25		MHz
Propagation Delay, CCK† to RCO	$t_{PLH}$		15		25		29	ns
	$t_{PHL}$		15		25		29	
Propagation Delay, CCLR‡ to RCO	$t_{PHL}$		17		28		33	ns
Propagation Delay, RCK† to Q	$t_{PLH}$		18		31		37	ns
	$t_{PHL}$		10		16		19	
Propagation Delay, G† to Q	$t_{PHL}$		14		20		24	ns
Propagation Delay, G† to Q	$t_{PLH}$	14		20		24	ns	
Pulse Duration	$t_w$	CCK or RCK High or Low	10	15		20		ns
		CCLR Low	10	15		20		
Setup Time	$t_{su}$	CCKEN‡ Low to CCK†	10	15		20		ns
		CCLR‡ High to CCK†	6	10		10		
		CCK† to RCK††	15	20		25		
Input Capacitance	$C_{IN}$		5					pF
Power Dissipation Capacitance*	$C_{PD}$							pF

\*  $C_{PD}$  determines the no-load dynamic power dissipation:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

† For AC-switching test circuits and timing waveforms see section 2.

†† This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

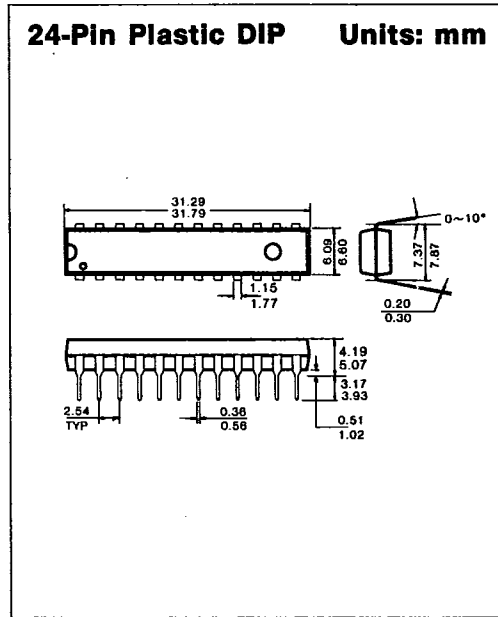
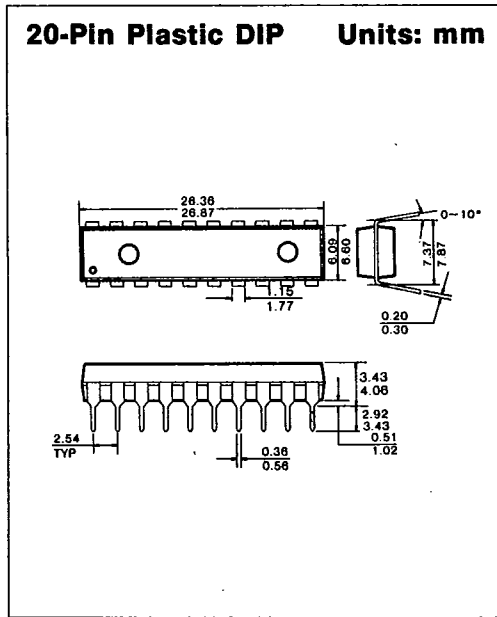
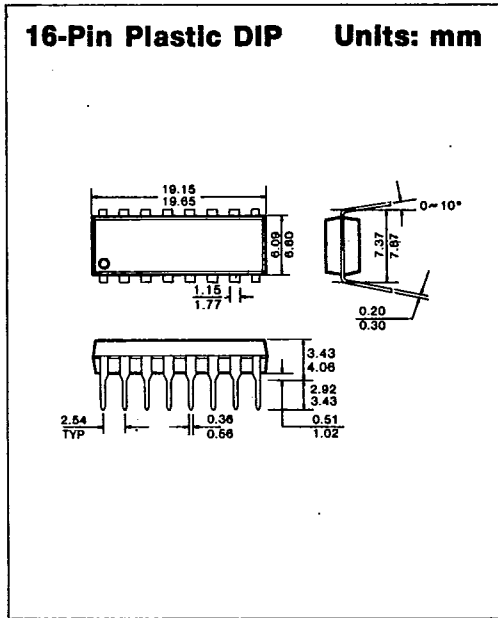
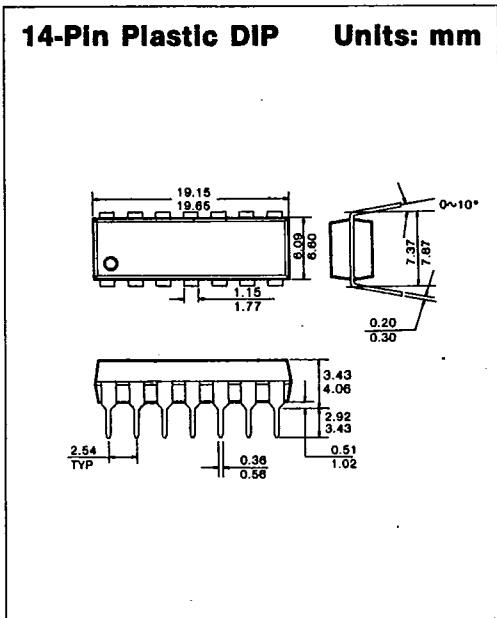
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**PACKAGE DIMENSIONS**

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**1. PLASTIC PACKAGES**

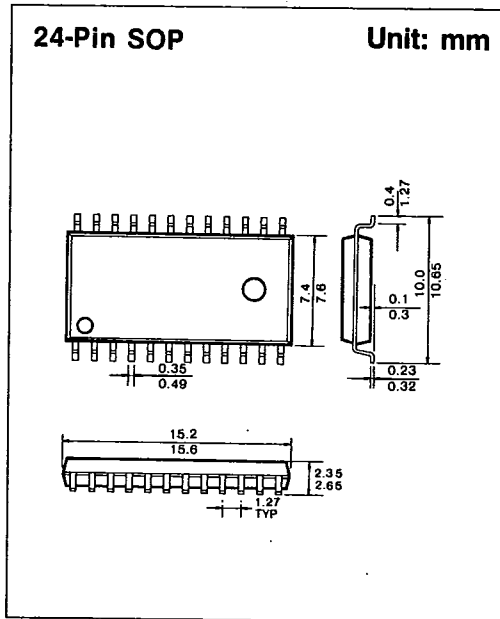
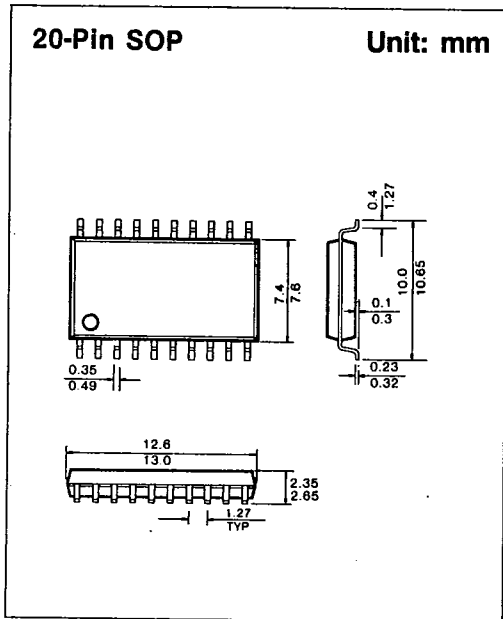
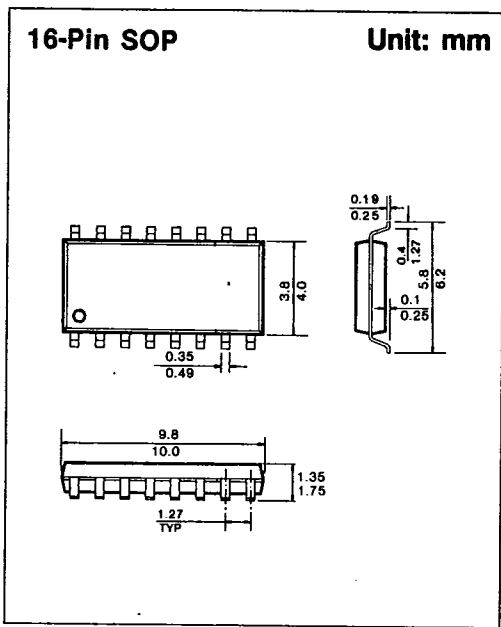
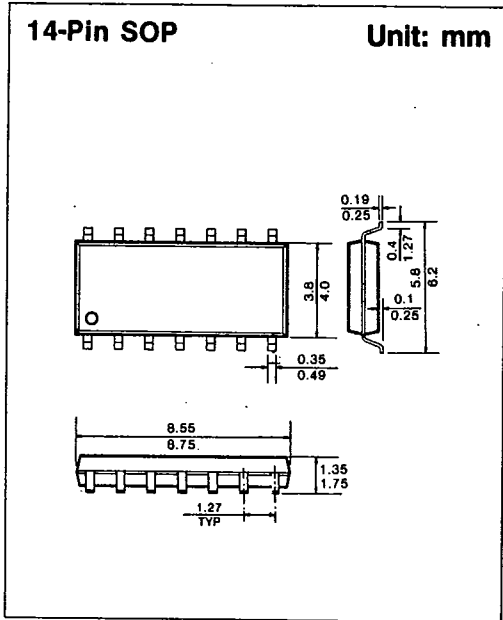


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**PACKAGE DIMENSIONS**

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**2. CERAMIC PACKAGES**

**14-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	18.16	19.58
E	8.10	7.49
E <sub>1</sub>	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

**16-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B <sub>1</sub>	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E <sub>1</sub>	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

**20-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E <sub>1</sub>	7.77	7.88
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

**24-Pin Ceramic DIP Units: mm**

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B <sub>1</sub>	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E <sub>1</sub>	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93

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