

KS54AHCT 823/824

KS74AHCT

9-Bit Bus Interface Flip-Flops

with 3-State Outputs T-46-07-05

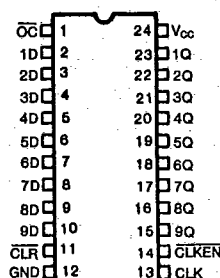
Preliminary Specifications

FEATURES

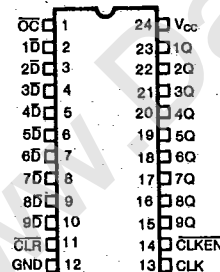
- Functionally Equivalent to AMD's Am29823 and Am29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up-High-Impedance State
- FUNCTION, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5\text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^\circ\text{C}$
KS54AHCT: -55°C to $+125^\circ\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATIONS

'823



'824



DESCRIPTION

These 9-bit bus interface flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{\text{CLKEN}}$) low, the D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The '823 has noninverting D inputs and the '824 has inverting $\overline{\text{D}}$ inputs. Taking the $\overline{\text{CLR}}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{\text{OC}}$) can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

FUNCTION TABLES

'823

INPUT					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

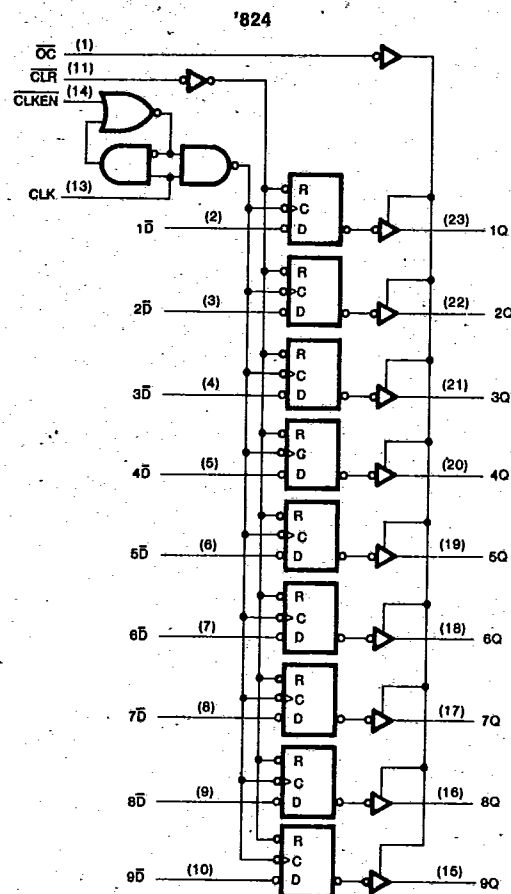
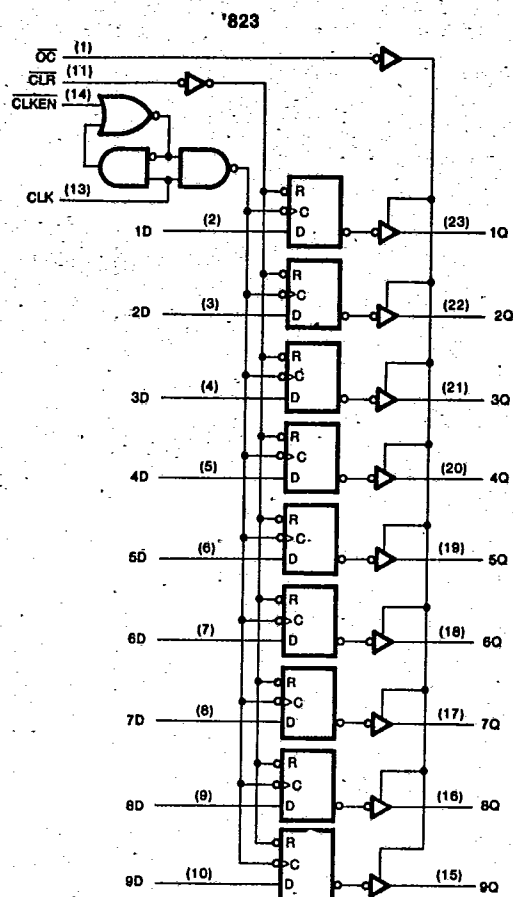
'824

INPUTS					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	$\overline{\text{D}}$	Q
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z



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LOGIC DIAGRAMS


KS54AHCT 823/824
KS74AHCT
9-Bit Bus Interface Flip-Flops
with 3-State Outputs T-46-07-05
Absolute Maximum Ratings*

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} -65°C to +150°C
 Power Dissipation Per Package, P_d [†] 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

[†] Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} .. 0V to V_{CC}
 Operating Temperature

Range KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^{\circ}\text{C}$		KS74AHCT	KS54AHCT	Unit
					$T_a = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	$T_a = -55^{\circ}\text{C to } +125^{\circ}\text{C}$	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu\text{A}$ $I_O=-6\text{mA}$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu\text{A}$ $I_O=12\text{mA}$ $I_O=24\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IH} $V_{OUT}=V_{CC}$ or GND		± 0.5	± 5.0	± 10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4\text{V}$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

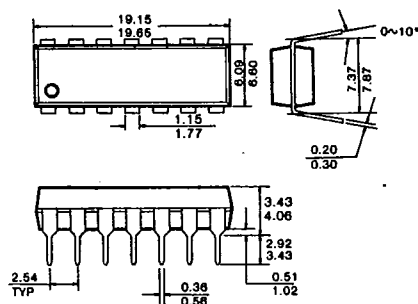
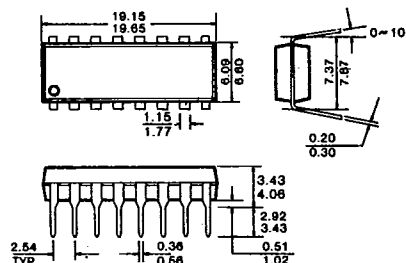
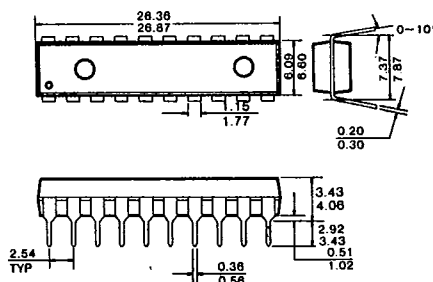
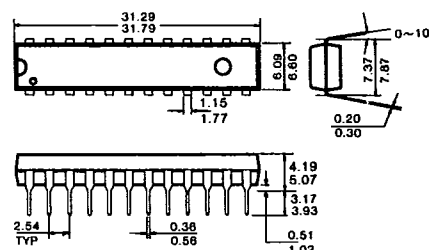


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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT823, AHCT824

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Operating Frequency	f_{max}	$C_L = 50\text{pF}$	50	35		30		MHz
Propagation Delay CLK to any Q	t_{PLH}	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	ns
	t_{PHL}	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	8 11		14 19		17 23	
Propagation Delay, CLR to Any Q	t_{PHL}	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	10 13		17 22		21 27	ns
Output Enable Time, OC to any Q	t_{PZH}	$R_L = 1\text{k}\Omega$ $C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	ns
	t_{PZL}	$C_L = 50\text{pF}$ $C_L = 150\text{pF}$	11 14		18 23		22 28	
Output Disable Time, OC to any Q	t_{PHZ}	$R_L = 1\text{k}\Omega$	13		18		22	ns
	t_{PLZ}	$C_L = 50\text{pF}$	13		18		22	
Pulse Width	CLR low	t_w	9	15		18		ns
	CLK high or low		9	15		18		
Setup Time before CLK†	CLR inactive	t_{su}	9	14		17		ns
	Data		9	14		17		
	CLKEN high		9	14		17		
	or low		9	14		17		
Hold Time, CLKEN or data after CLK†	t_h		-3	0		0		ns
Input Capacitance	C_{IN}		5					pF
Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance* (per stage)	C_{PD}	OC = V_{CC}	5					pF
		OC = GND	30					pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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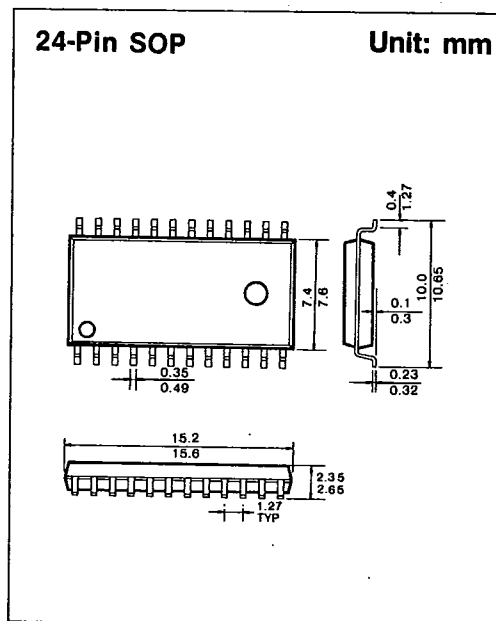
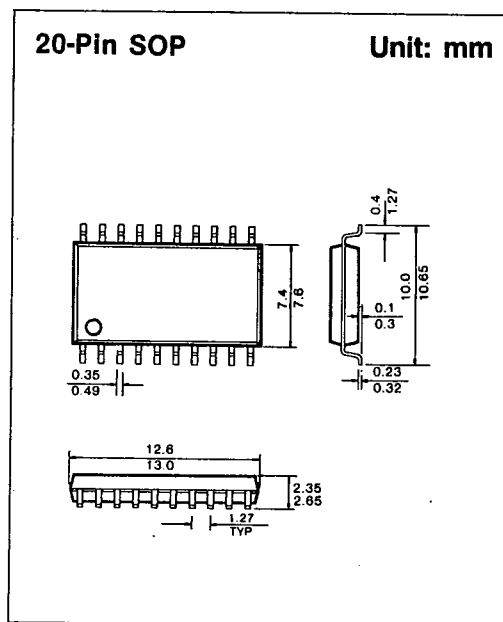
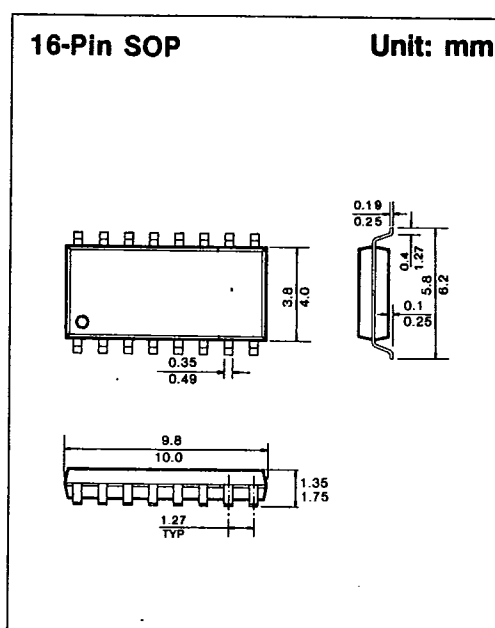
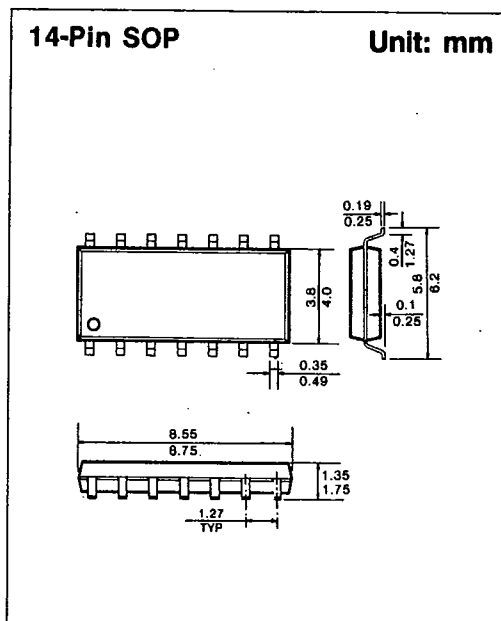
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PACKAGE DIMENSIONS

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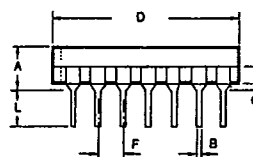
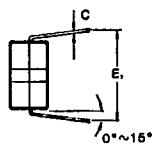
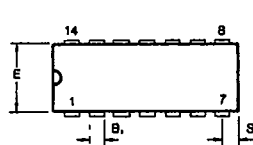
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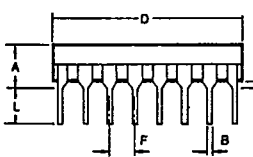
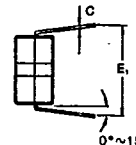
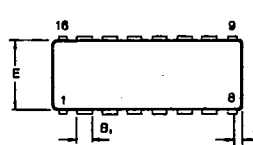
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PACKAGE DIMENSIONS

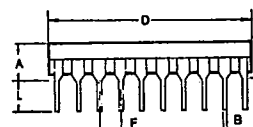
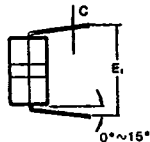
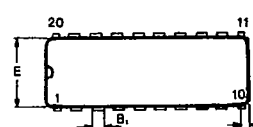
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2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

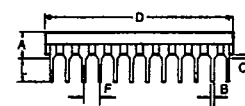
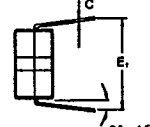
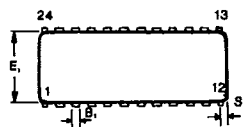
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93



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