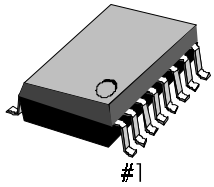
INTRODUCTION

KA8808A is a superior low-power-programmable PLL frequency synthesizer which can be used in a high performance Wide Area Pager system.

KS8808A consists of 2 kinds of divider block including a 17bit Shift register, 16-bit Latch, 14/16-bits Counter, Prescaler, and a phase detector block including a Phase detector, Lock detector and a Charge pump.

16–TSSOP–0044



(Magnification = 1 : 4)

FEATURES

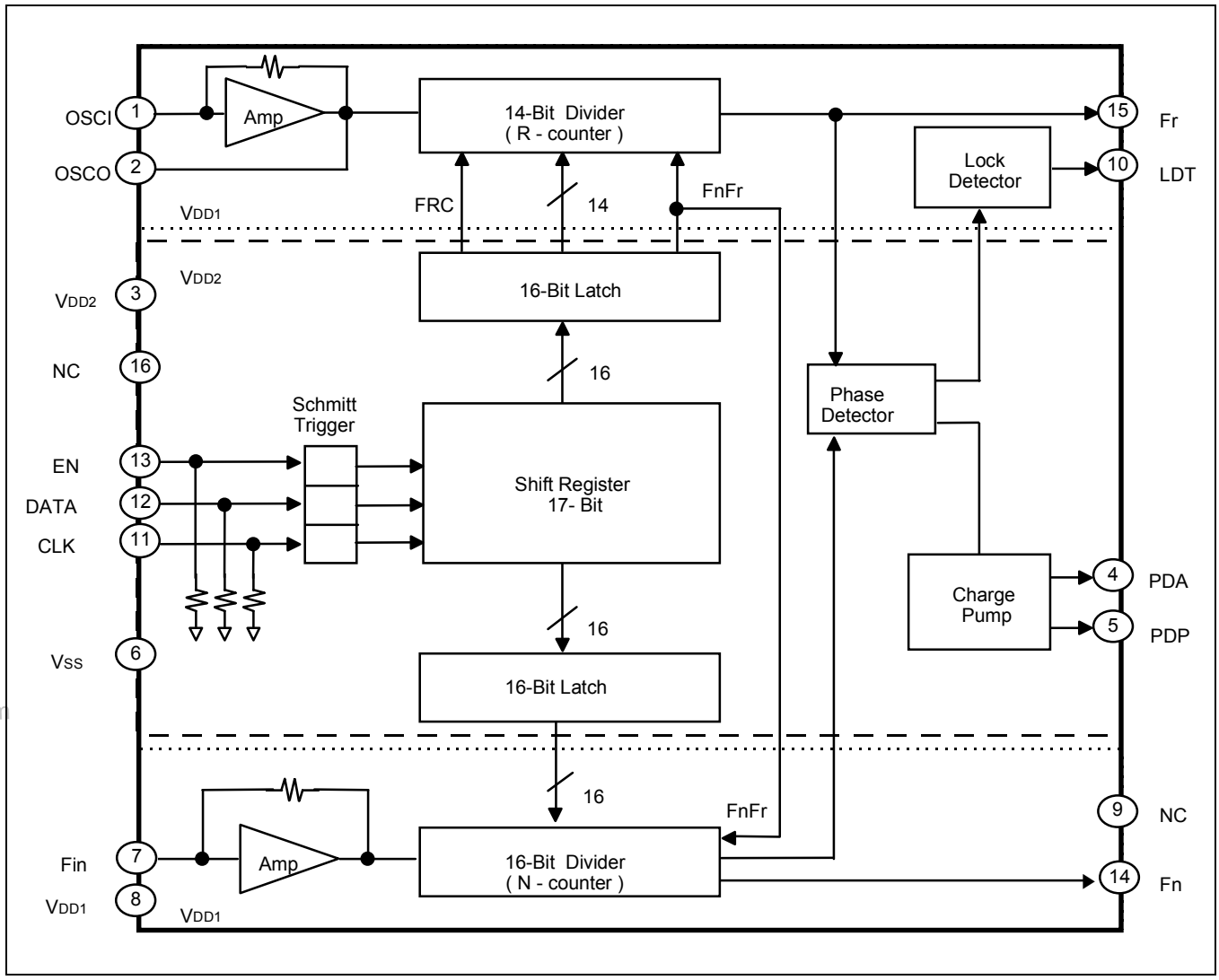
- Maximum operating frequency:
  120MHz @ 500mV$_{P-P}$, V_{DD1} = 0.95V, V_{DD2} = 3.0V
  165MHz @ 500mV$_{P-P}$, V_{DD1} = 1.0V, V_{DD2} = 3.0V
- On-chip reference oscillator supports external crystal which oscillates up to 18MHz
- Superior supply current:
  F_{FIN} = 90MHz, I_{DD1} = 0.6mA (Typ.) @ V_{DD1} = 1.0V, V_{DD2} = 3.0V
  F_{FIN} = 150MHz, I_{DD1} = 0.9mA (Typ.) @ V_{DD1} = 1.0V, V_{DD2} = 3.0V
- Operating voltage: V_{DD1} = 0.95 ~ 2.0V and V_{DD2} = 2.0 ~ 3.3V
- Reference frequency counter divider range: 1 / 28 ~ 1 / 65532 (Multiple 4)
  But, the Divider range with FRC_High state: 1 / 7 ~ 1 / 16383
- RX frequency counter divider range: 1 / 28 ~ 1 / 65535
- Package type: 16–TSSOP (0.65mm)

ORDERING INFORMATION

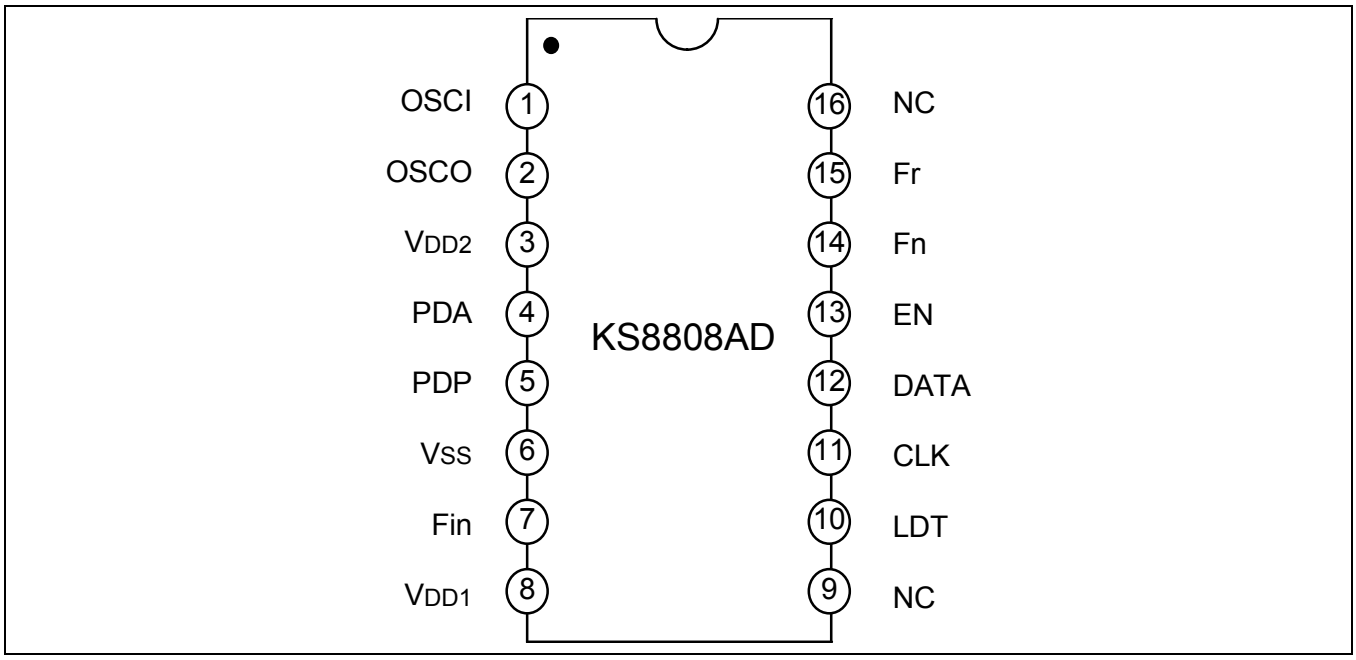
Device	Package	Operating Temperature
+KS8808AD	16–TSSOP–0044	–25°C to +75°C

+: New Product

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	OSCI	I	These input / output pins generate the reference frequency. In case of OSCI Pin, external reference frequency can be used through the AC coupling.
2	OSCO	O	
3	V_{DD2}	–	The highest potential supply terminal that can be supplied up to 2.0 ~ 3.3V, except for V_{DD1}.
4	PDA	O	The Output of RX Phase detector terminal for active loop filter There are 3-kinds of output signal states according to Rx Loop Error; – If Fr > Fn (Fr is leading), the output is negative pulse state, – If Fr < Fn (Fr is lagging), the output is positive pulse state, – If Fr = Fn (the same phase), the output is high impedance state.
5	PDP	O	The Output of RX Phase detector terminal for passive loop filter There are 3-kinds of output signal states according to Rx Loop Error; – If Fr > Fn (Fr is lagging), the output is negative pulse state, – If Fr < Fn (Fr is leading), the output is positive pulse state, – If Fr = Fn (the same phase), the output is high impedance state.
6	V_{SS}	–	Ground terminal
7	Fin	I	Input terminal for 16 bit Divider from VCO. Mostly, VCO output should be input through the AC coupling and the minimum input level is 500mV_{P-P} (in case of 90MHz)
8	V_{DD1}	–	Voltage supply terminal for Oscillator and Fin block. This pin can be supplied up to 0.95 ~ 2.0V from V_{SS}.
9	NC	–	No Connection
10	LDT	O	Lock detector is also on output of the Phase Detector. The Low state of this output shows unlock status, which is the error width between the Ref. signal and the VCO output signal.
11	CLK	I	These pins are controlled by the μ-controller and it also has Schmitt Trigger architecture. Internally biased pull-down. The features of these pins are as follows : Clock input for 17-bit Shift Register, Serial data input (it include FnFr-on / off and FRC), Latch enable input (User selectable EN1 or EN2).
12	DATA	I	
13	EN	I	
14	Fn	O	Output terminal for divider value of N-counter. To control the output On/Off, the FnFr bit of the Reference register can be programmed. When FnFr bit is set to High, this output shows low level.
15	Fr	O	Output terminal of divider value of N-counter. To control the output On/Off, the FnFr bit of the Reference register can be programmed. When FnFr bit is set to High, this output shows low level.
16	NC	–	No Connection. Internally biased pull-up.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD} ~ V_{DD2}	–0.3 ~ +4.0	V
Input Voltage	V_I	V_{SS} ~ 0.3 ~ V_{DD} + 0.3	V
Power Dissipation	P_D	350	mW
Operating Temperature	T_{OPR}	–25 ~ +75	°C
Storage Temperature	T_{STG}	–40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{DD1} = 1.0V, V_{DD2} = 3.0V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Operating voltage	V_{DD1}	–		0.95	1.0	2.0	V
	V_{DD2}	–		2.0	3.0	3.3	
Operating current	I_{DD1}	F_{OSCI} = 12.8MHz @ 0.5V_{P-P} V_{DD1} = 1.0V V_{DD2} = 3.0V	F_{FIN} = 90MHz	–	0.6	–	mA
	I_{DD2}		F_{FIN} = 150MHz	–	0.9	–	
Standby current	I_{SB}	V_{DD1} = 0V, V_{DD2} = 3.0V		–	–	10	µA
Input Voltage (DATA, CLK, EN, BS)	V_{IL}	–		–	–	0.3	V
	V_{IH}	–		V_{DD3}-0.3	–	–	
Input current (Fin, Xin)	V_{IH}	V_{IH} = V_{DD1}		–	–	20	µA
	V_{IL}	V_{IL} = 0V		–	–	20	
Input frequency	F_{FIN}	F_{FIN} = 0.5V_{P-P}	V_{DD1} = 0.95V	–	–	120	MHz
			V_{DD1} = 1.0V	–	–	165	
	F_{OSCI}	V_{OSCI} = 0.5V_{P-P}		7	–	18	
Output current (PDA, PDP)	I_{OH1}	V_{OH} = 0.4V		1.0	–	–	mA
	I_{OL1}	V_{OL} = V_{DD1} - 0.4V		1.0	–	–	
Output current (Fr, Fn, LDT)	I_{OH2}	V_{OH} = 0.4V		0.1	–	–	mA
	I_{OL2}	V_{OL} = V_{DD1} - 0.4V		0.1	–	–	
Setup-time (DATA-CLK, CLK-EN)	ts	–		2	–	–	µS
Hold time	t_H	–		2	–	–	µS

FUNCTIONAL DESCTRIPTION

Table 1. N-Counter Register Program Scheme (17 bits)

Bit	Bit 16 (ND 15) ~ Bit 1 (ND 0)	Bit 0 (LSB)
Name	RxD	PMC
Description	Rx. Program Data (ND 15 ~ ND 0)	Program Mode Control
Function	16 Bit Programmable Rx. N-Counter Data	0: Rx. N-Counter 1: Ref. R-Counter

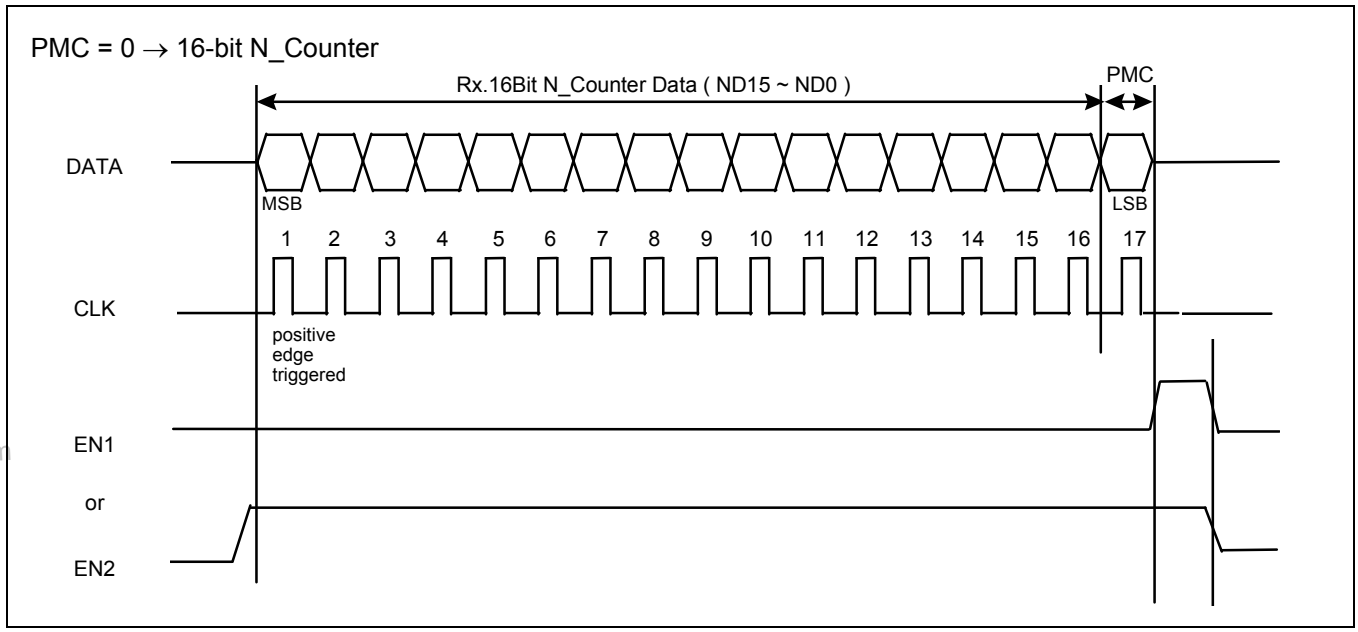
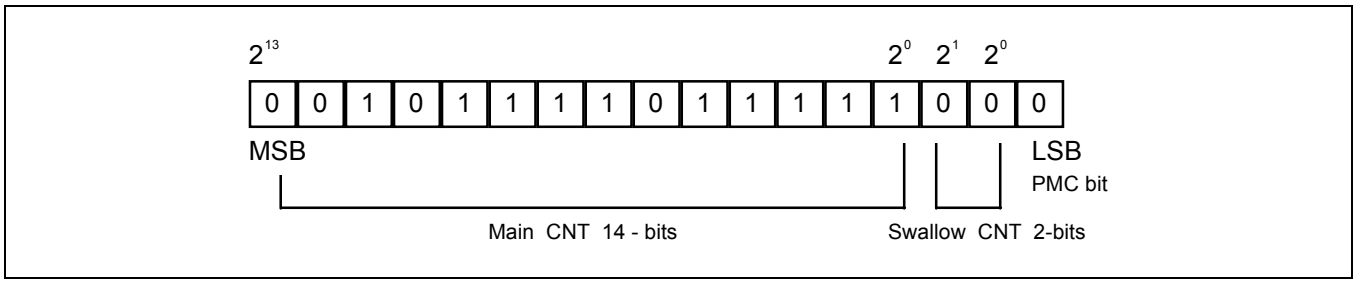


Figure 1. Rx. Register Programming Timing

- Programmable N-counter consists of 2-bits Swallow Counter, 4/5 Dual moduars Prescaler and 14-bits Main Counter
- The Divide Ratio is;
  N = (P + 1) × S + P (M – S) = PM + S;
  - — P = Dual Modulars Prescaler (4)
  - — S = 2-bits Swallow Counter value (0 ~ 3)
  - — M = 14-bits (7 ~ 16383)
  - — N = Programmable N-Counter value (N > S : 28 ~ 65535)

- Ex 1) In case of 14-bits program, Fc = 325.300MHz, Multiplier = 4, Fin = 75.975MHz
  [Fin Freq. / Ref. Freq.] = 75.975MHz / 6.25kHz = 12156



- According to the above equation, 12156/4(P) = 3039 & left = 0, that means, Swallow CNT value is “0”, Main CNT value is “3039”.
- The PMC bit is Program Control Bit, if [0], the N-Counter will be Enabled.

Table 2. R-Counter Register Program Scheme (17 bits)

Bit	Bit 16 (RD 13) ~ Bit 3 (RD 0)	Bit 2	Bit 1	Bit 0 (LSB)
Name	RefD	FRC	FnFr	PMC
Description	Reference Program Data (RD 13 ~ RD 0)	Control Mode		Program mode control
Function	14 Bit Programmable Ref. R-Counter	0: No FRC (OSCI/4R) 1: FRC (OSCI/R)	0: Fn, Fr function 1: Fn, Fr Low	0: Rx. N-Counter 1: Ref. R-Counter

Table 3. Control Mode

FRC	FnFr	Fn (Pin 14)	Fr (Pin 15)
0	0	Fn out (Fin / N counter)	Fr out (OSCI / 4 x R)
0	1	Low	Low
1	0	Fn out (Fin / N-counter)	Fr out (OSCI / R)
1	1	Low	Low

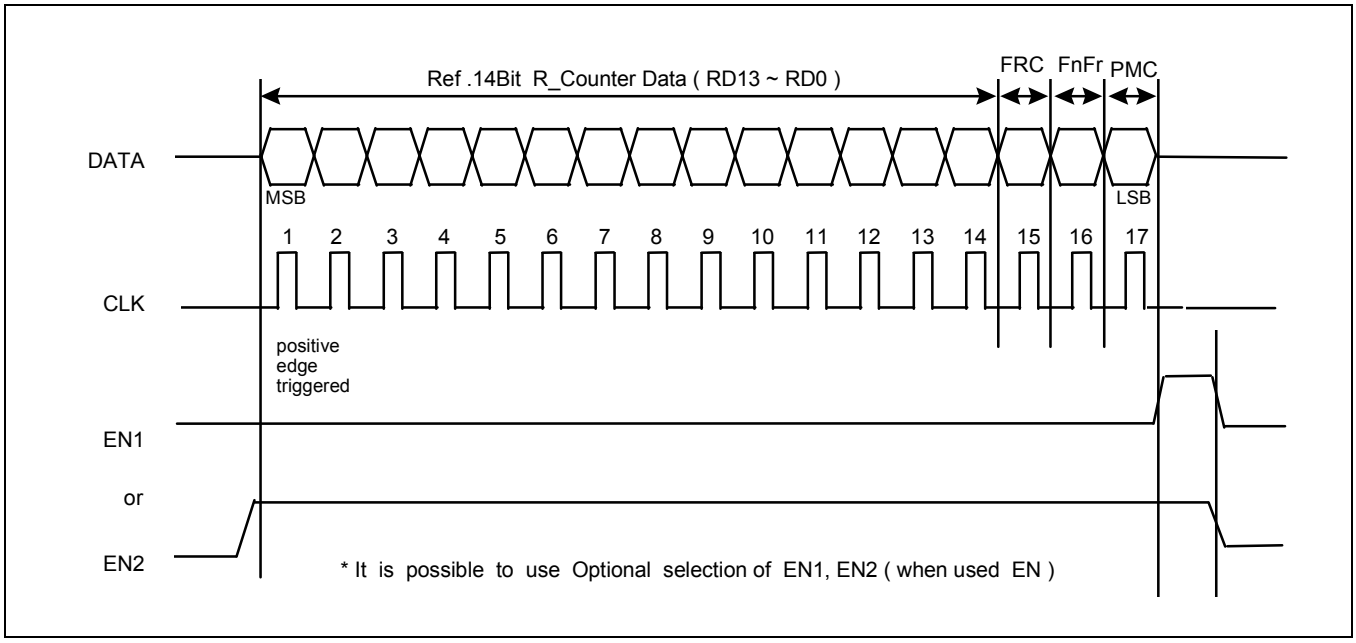
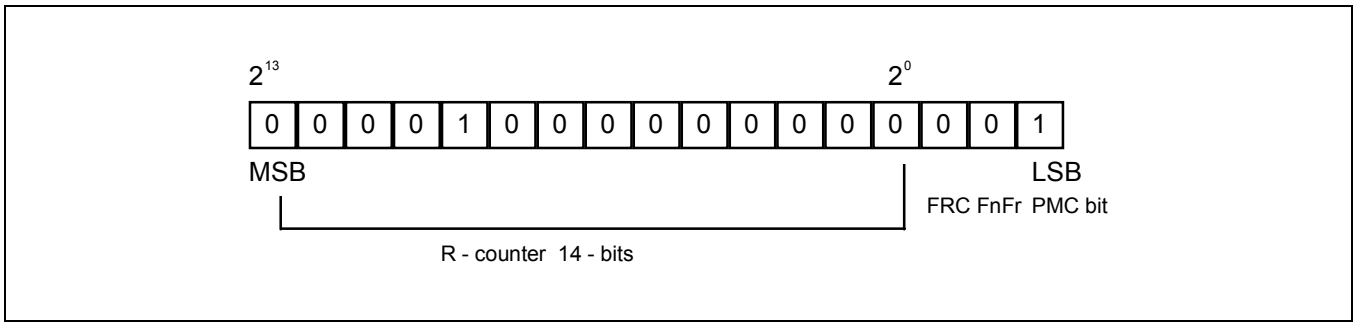


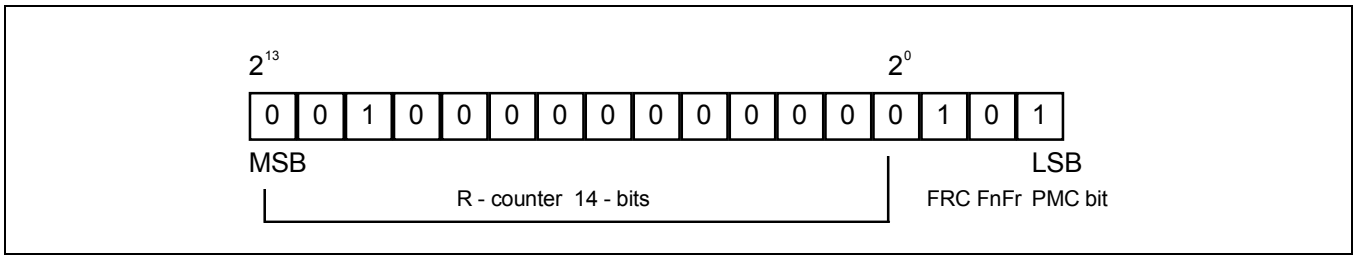
Figure 2. Ref. Register Programming Timing

- The Input Reference Frequency (X-tal Oscillator) will be divided by 1/4 Prescaler, and then divided by Pre-programmed R-counter value once more.
- Programmable R-Counter consists of Fixed 1/4 Prescaler, 14-bits Programmable Counter
  When FRC = 0, Fixed 1/4 Prescaler is used, 14-bits counter, Can divide Multiple 4
  RD = 4, R = 28 (=4 x 7) ~ 65532 -- (Min. Divide value:7)

  When FRC = 1, Fixed 1/4 Prescaler isn's used, but using 14-bits counter, Can divide all value
  RD = R = 7 ~ 16384 [All value] --- (Min. Divide value:7)
- Ex 1) FRC = 0, In case of 14-bits Program, Fosc = 12.8MHz and fixed 1/4 prescaler is used
  [(Osc. Freq. / Prescaler) / Ref. Freq.] = [(12.8MHz / 4) / 6.25kHz] = 512



- Ex 2) FRC = 1, In case of 14-bits Program, Fosc = 12.8MHz and fixed 1/4 prescaler is not used
  [Osc. Freq. / Ref. Freq.] = [12.8MHz / 6.25kHz] = 2048



* The PMC bit is program Control Bit, if [1], the R-Counter will be Enablrf

Serial DATA Input Timing & Phase Detector / Lock Detector Output Waveforms

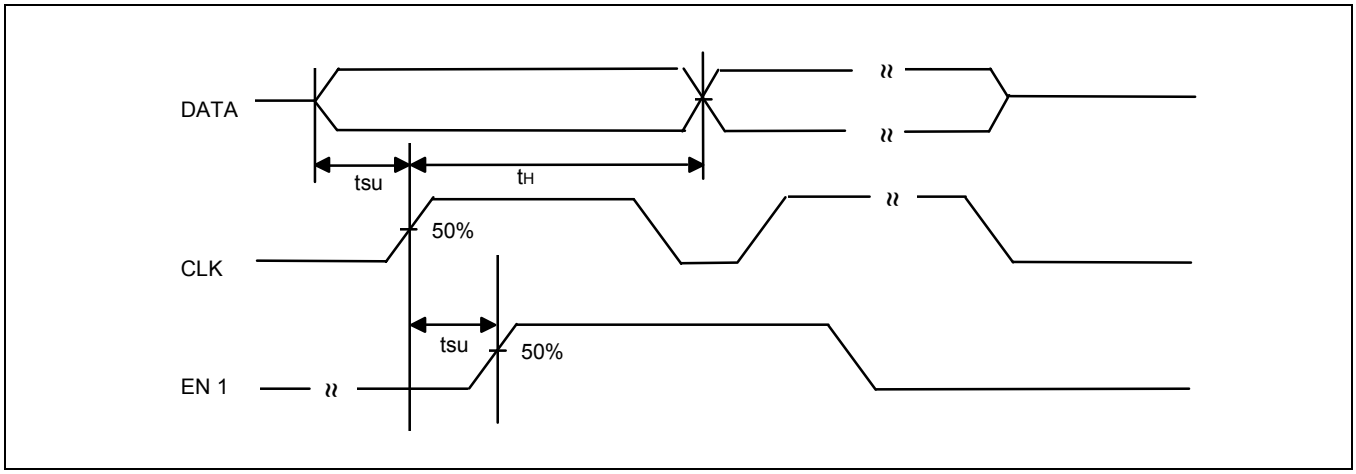


Figure 3. Serial Data Input Timing

The architecture of R-Count Divider

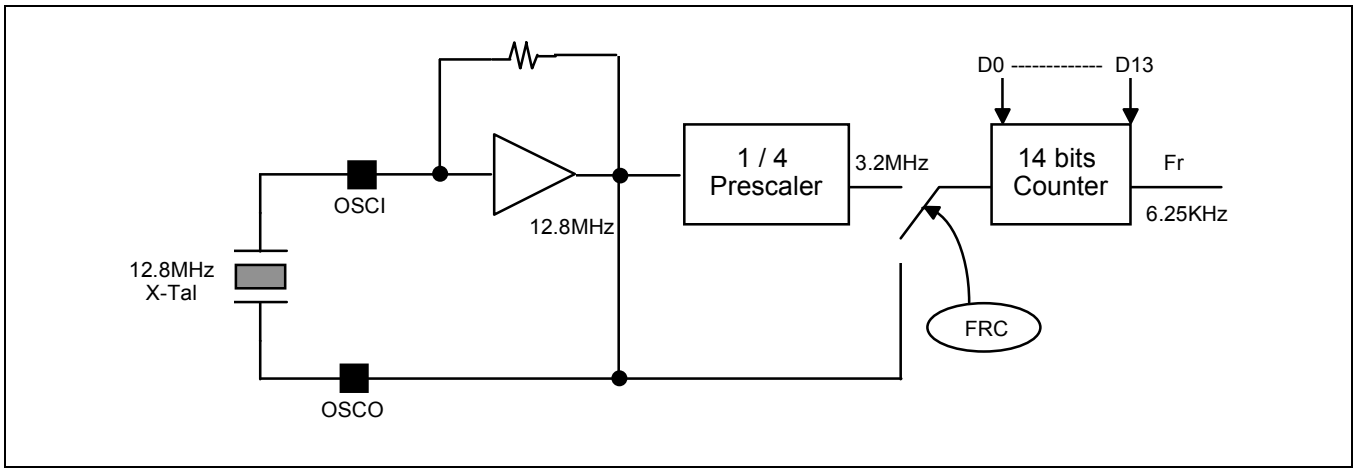


Figure 4. R-CNT architecture

VCO output Frequency

$f_{VCO} = N \times f_{VCO} / RD$

f_{VCO} = VCO output frequency
f_{OSC} = X-tal Oscillator Frequency
RD = Programmable Reference R-counter value
N = Programmable N-counter value

Phase Detector / Lock Detector

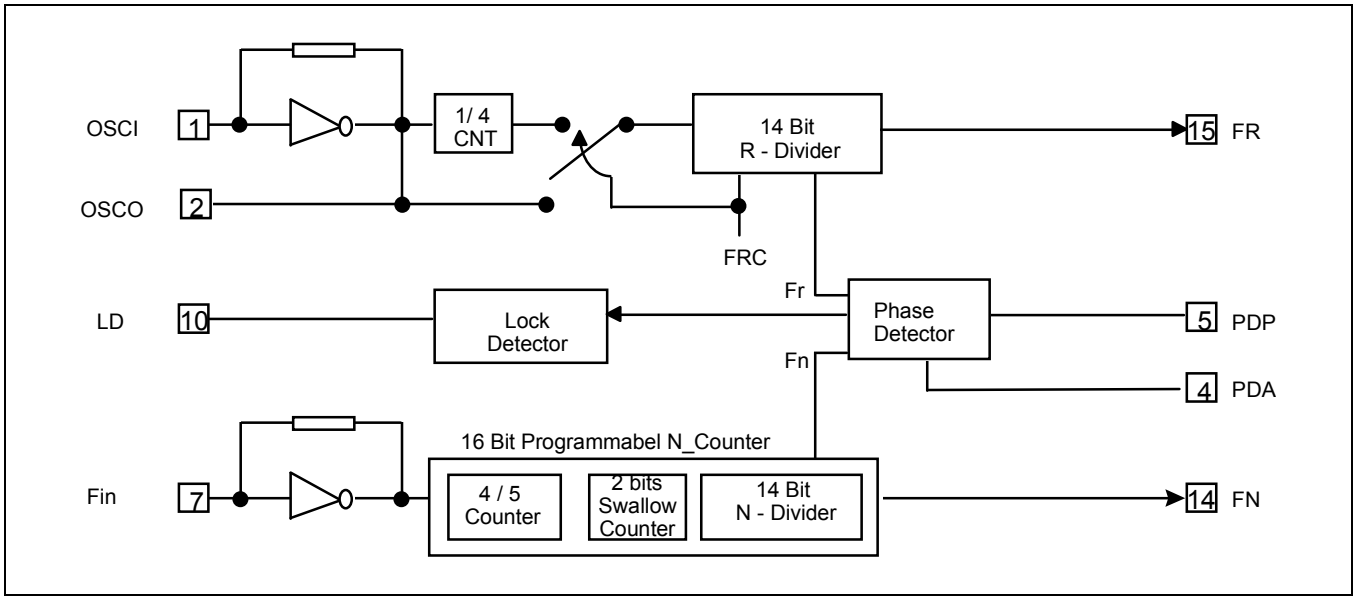


Figure 5. Phase Detector / Lock Detector Block Diagram

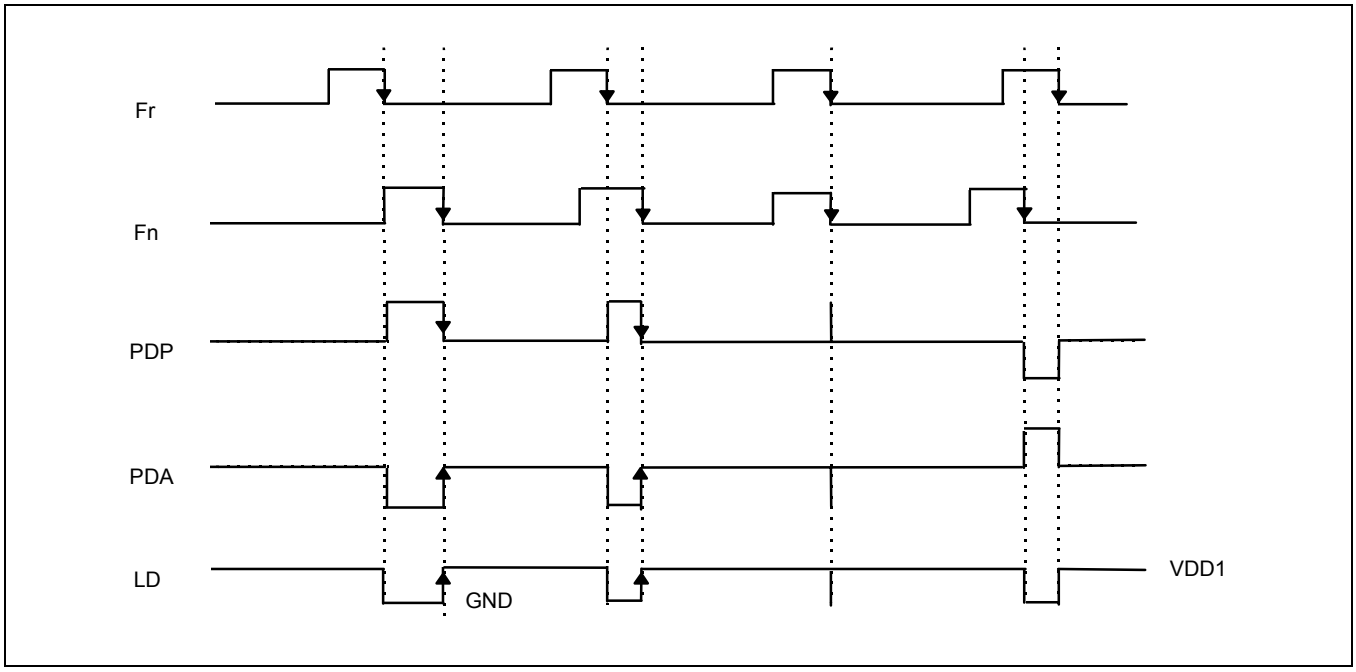


Figure 6. Phase Detector / Lock Detector Output Waveforms

NOTES:

1. Phase detector always compares the Phase difference of N-counter with R-counter, and set to High or Low state as much as the phase difference.
2. The LD output set to Low level same as Phase detector error width.

APPLICATION CIRCUIT