

INTRODUCTION

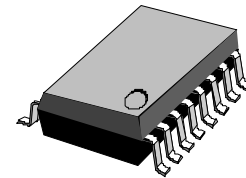
KA8808 is a superior low-power-programmable PLL frequency synthesizer which can be used in a high performance Wide Area Pager system.

KS8808 consists of 2 kinds of divider block including a 17-bit Shift register, 16-bit Latch, 14/16-bits Counter, Prescaler, and a phase detector block including a Phase detector, Lock detector and a Charge pump.

FEATURES

- Maximum operating frequency:
150MHz @ 500mV_{P-P}, V_{DD1} = 0.95V
180MHz @ 500mV_{P-P}, V_{DD1} = 1.0V
- On-chip reference oscillator supports external crystal which oscillates up to 18MHz
- Superior supply current: (V_{DD1} = V_{DD2} = 1.0V, V_{DD3} = 3.0V)
 - F_{FIN} = 90MHz, I_{DD1} = 0.6mA (Typ.)
 - F_{FIN} = 150MHz, I_{DD1} = 0.9mA (Typ.)
 - F_{FIN} = 180MHz, I_{DD3} = 1.1mA (TyP.)
- Operating voltage: V_{DD1} = 0.95 ~ 2.0V and V_{DD2} = 0.95V ~ 2.0V and V_{DD3} = 2.0V ~ 3.3V
- Reference frequency counter divider range: 1 / 28 ~ 1 / 65532 (Multiple 4)
But, the Divider range with FRC_High state: 1 / 7 ~ 1 / 16383
- RX frequency counter divider range: 1 / 28 ~ 1 / 65535
- Package type: 16SSOP (0.8mm)

16-SSOP-0044

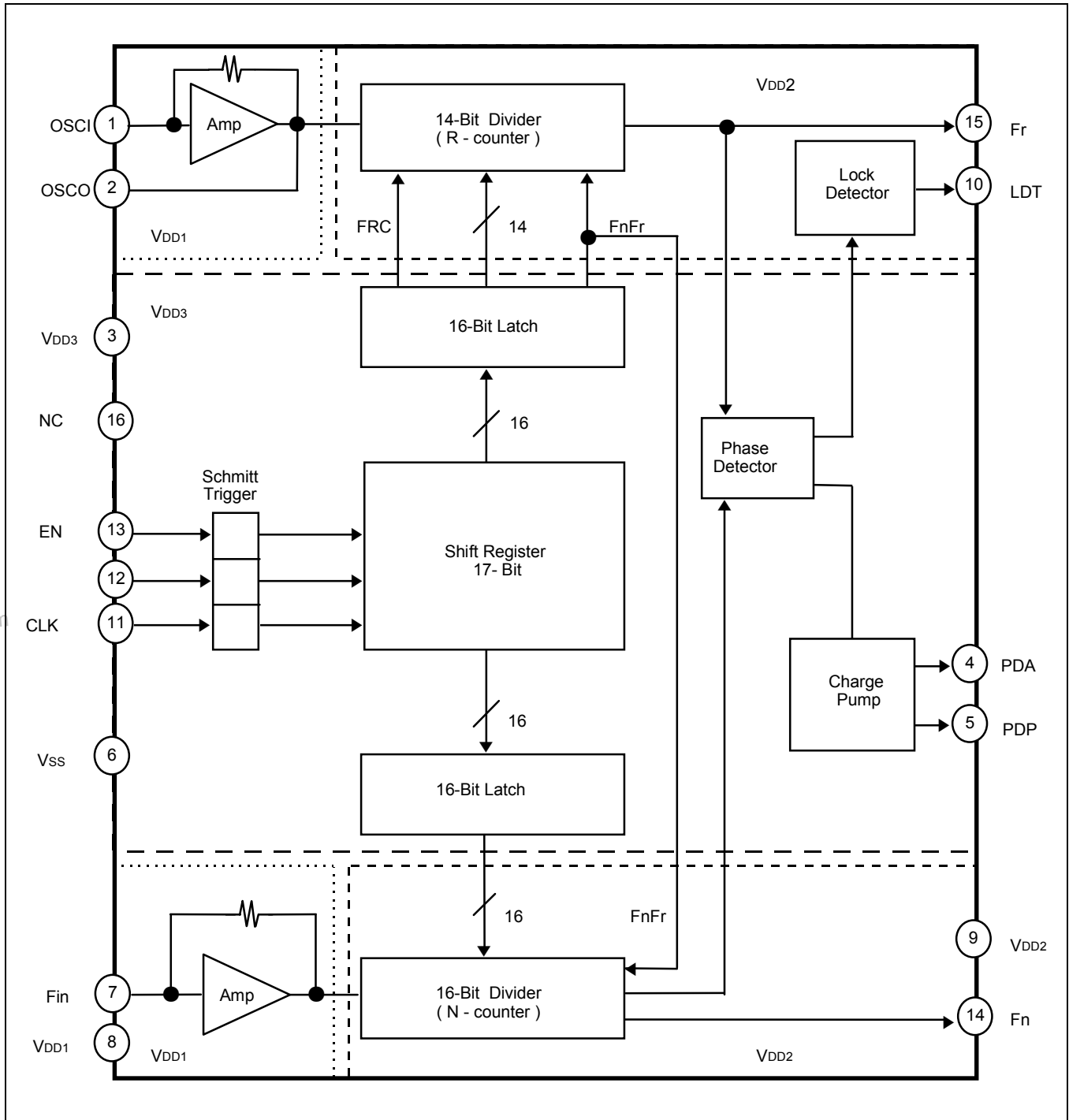


(Magnification = 1 : 4)

ORDERING INFORMATION

Device	Package	Operating Temperature
KS8808	16-SSOP-0044	-25°C to +75°C

BLOCK DIAGRAM

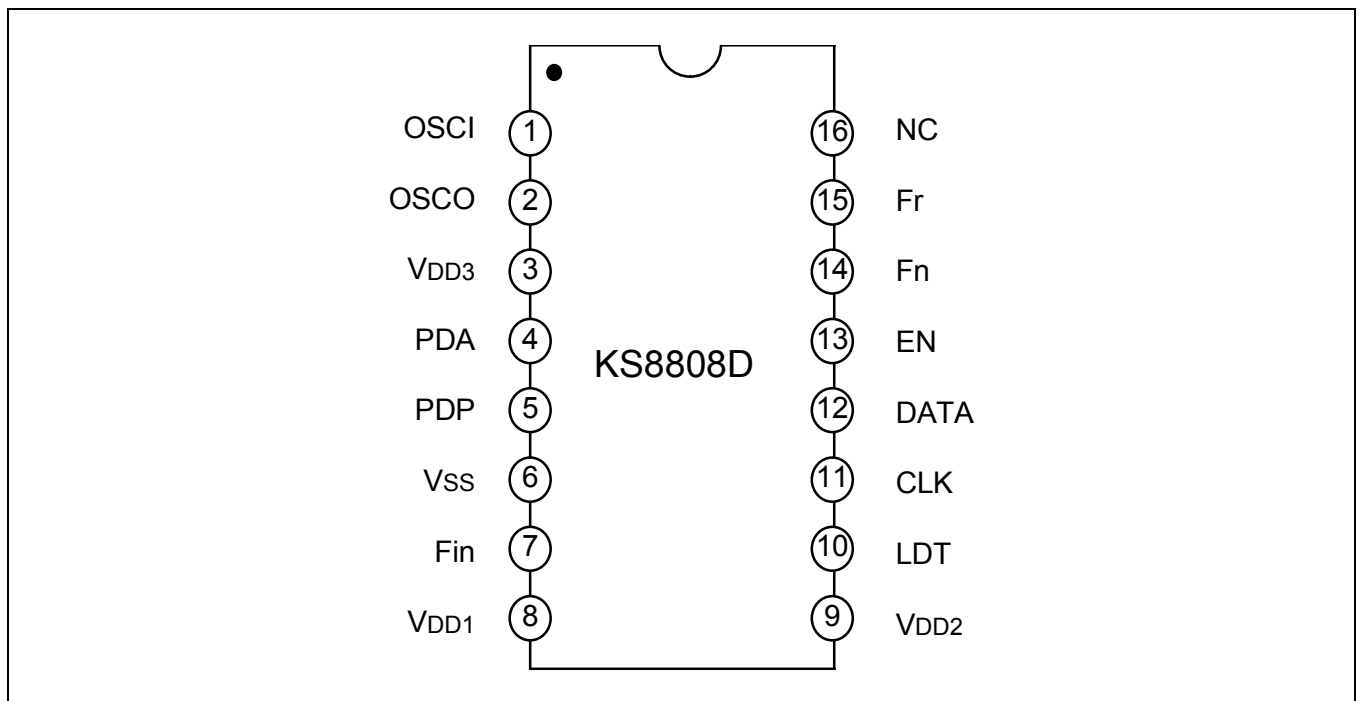


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PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	OSCI	I	These input / output pins generate the reference frequency. In case of an OSCI pin, external reference frequency can be input through an AC coupling.
2	OSCO	O	
3	V _{DD3}	–	The highest potential supply terminal that can be supplied up to 2.0V ~ 3.3V, except for V _{DD1} and V _{DD2} .
4	PDA	O	The Output of RX Phase detector terminal for active loop filter. There are 3-kinds of output signal states according to Rx Loop Error – If Fr < Fn (Fr is leading), the output is negative pulse state – If Fr > Fn (Fr is lagging), the output is positive pulse state – If Fr = Fn (the same phase), the output is high impedance state
5	PDP	O	The Output of RX Phase detector terminal for active loop filter. There are 3-kinds of output signal states according to Rx Loop Error – If Fr < Fn (Fr is lagging), the output is negative pulse state – If Fr > Fn (Fr is leading), the output is positive pulse state – If Fr = Fn (the same phase), the output is high impedance state
6	V _{SS}	–	Ground terminal
7	Fin	I	Input terminal for 16-bit Divider from VCO. Mostly, VCO output should be input through an AC coupling and the minimum input level is 500mV _{P-P} (in case of 90MHz)
8	V _{DD1}	I	Voltage supply terminal for Oscillator and Fin block. This pin can be supplied up to 0.95 ~ 2.0V from V _{SS} .
9	V _{DD2}	I	Voltage supply terminal for each Divider block (N & R counter). This pin can be supplied up to 0.95V ~ 2.0V.
10	LDT	O	Lock detector is also an output of the Phase Detector. The Low state of this output shows the unlock status, which is the error width between the Ref. signal and the VCO output signal.
11	CLK	I	These pins are controlled by μ -controller and it also has Schmitt Trigger architecture. Internally biased pull-down. The features of these pins are as follows; Clock input for 17-bit Shift Register, Serial data input (it include FnFr-on / off and FRC), Latch enable input (User selectable EN1 or EN2)
12	DATA	I	
13	EN	I	
14	Fn	O	Output terminal for divider value of N-counter. To control the output On/Off, the FnFr bit of the Reference register can be programmed. When FnFr bit set to High, this output shows low level.
15	Fr	O	Output terminal for divider value of N-counter. To control the output On/Off, the FnFr bit of Reference register can be programmed. When FnFr bit set to High, this output shows low level.
16	NC	–	No Connection. (Internally biased Pull-up)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{DD} \sim V_{DD2}$	-0.3 ~ +4.0	V
Input Voltage	V_I	$V_{SS} - 0.3 \sim V_{DD} + 0.3$	V
Power Dissipation	P_D	350	mW
Operating Temperature	T_{OPR}	-25 ~ +75	°C
Storage Temperature	T_{STG}	-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

($T_a = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 1.0\text{V}$, $V_{DD3} = 3.0\text{V}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Operating voltage	V_{DD1}	–	0.95	1.0	2.0	V	
	V_{DD2}	–	2.0	3.0	3.3		
Operating current	I_{DD1}	$F_{OSCI} = 12.8\text{MHz}$ @ $0.5V_{P-P}$ $V_{DD1} = V_{DD2} = 1.0\text{V}$ $V_{DD3} = 3.0\text{V}$	$F_{FIN} = 90\text{MHz}$	–	0.6	–	mA
	I_{DD2}		$F_{FIN} = 150\text{MHz}$	–	0.9	–	
	I_{DD3}		$F_{FIN} = 180\text{MHz}$	–	1.1	–	
Standby current	I_{SB}	$V_{DD1} = V_{DD2} = 0\text{V}$, $V_{DD3} = 3.0\text{V}$	–	–	10	μA	
Input Voltage (DATA, CLK, EN, BS)	V_{IL}	–	–	–	0.3	V	
	V_{IH}	–	$V_{DD3}-0.3$	–	–		
Input current (Fin, Xin)	V_{IH}	$V_{IH} = V_{DD1}$	–	–	20	μA	
	V_{IL}	$V_{IL} = 0\text{V}$	–	–	20		
Input frequency	F_{FIN}	$F_{FIN} = 0.5V_{P-P}$	$V_{DD1} = 0.95\text{V}$	–	–	150	MHz
			$V_{DD1} = 1.0\text{V}$	–	–	180	
	F_{OSCI}	$V_{OSCI} = 0.5V_{P-P}$	7	–	18		
Output current (PDA, PDP)	I_{OH1}	$V_{OH} = 0.4\text{V}$	1.0	–	–	mA	
	I_{OL1}	$V_{OL} = V_{DD1} - 0.4\text{V}$	1.0	–	–		
Output current (Fr, Fn, LDT)	I_{OH2}	$V_{OH} = 0.4\text{V}$	0.1	–	–	mA	
	I_{OL2}	$V_{OL} = V_{DD1} - 0.4\text{V}$	0.1	–	–		
Setup-time (DATA-CLK, CLK-EN)	t_s	–	2	–	–	μS	
Hold time	t_H	–	2	–	–	μS	

FUNCTIONAL DESCRIPTION

Table 1. Rx Register (17 bits)

Bit	Bit 16 (ND 15) ~ Bit 1 (ND 0)	Bit 0 (LSB)
Name	RxD	PMC
Description	Rx. Program Data (ND 15 ~ ND 0)	Program Mode Control
Function	16 Bit Programmable Rx. N-Counter Data	0: Rx. N-Counter 1: Ref. R-Counter

Table 2. Reference Register (17 bits)

Bit	Bit 16 (RD 13) ~ Bit 3 (RD 0)	Bit 2	Bit 1	Bit 0 (LSB)
Name	RefD	FRC	FnFr	PMC
Description	Reference Program Data (RD 13 ~ RD 0)	Control Mode		Program mode control
Function	14 Bit Programmable Ref. R-Counter	0: No FRC (OSCI/4R) 1: FRC (OSCI/R)	0: Fn, Fr function 1: Fn, Fr Low	0: Rx. N-Counter 1: Ref. R-Counter

Table 3. Control Mode

FRC	FnFr	Fn (Pin 14)	Fr (Pin 15)
0	0	Fn out (Fin / N counter)	Fr out (OSCI / 4 x R)
0	1	Low	Low
1	0	Fn out (Fin / N-counter)	Fr out (OSCI / R)
1	1	Low	Low

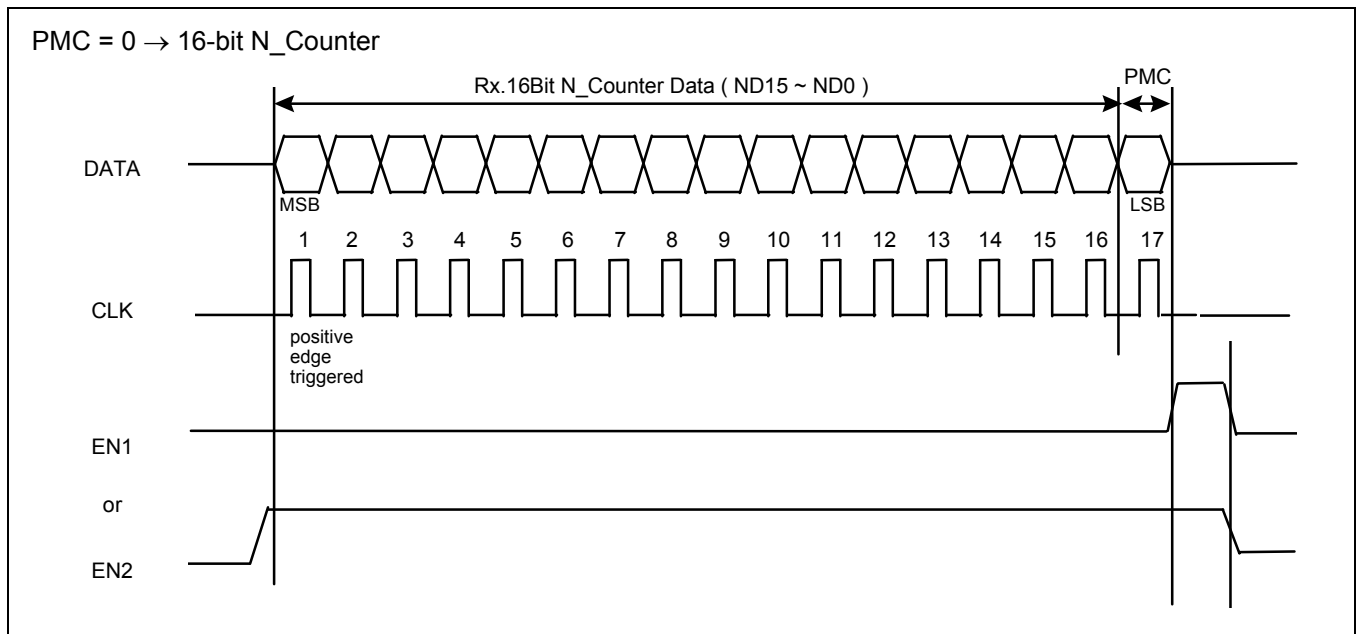


Figure 1. Rx. Register Programming Timing

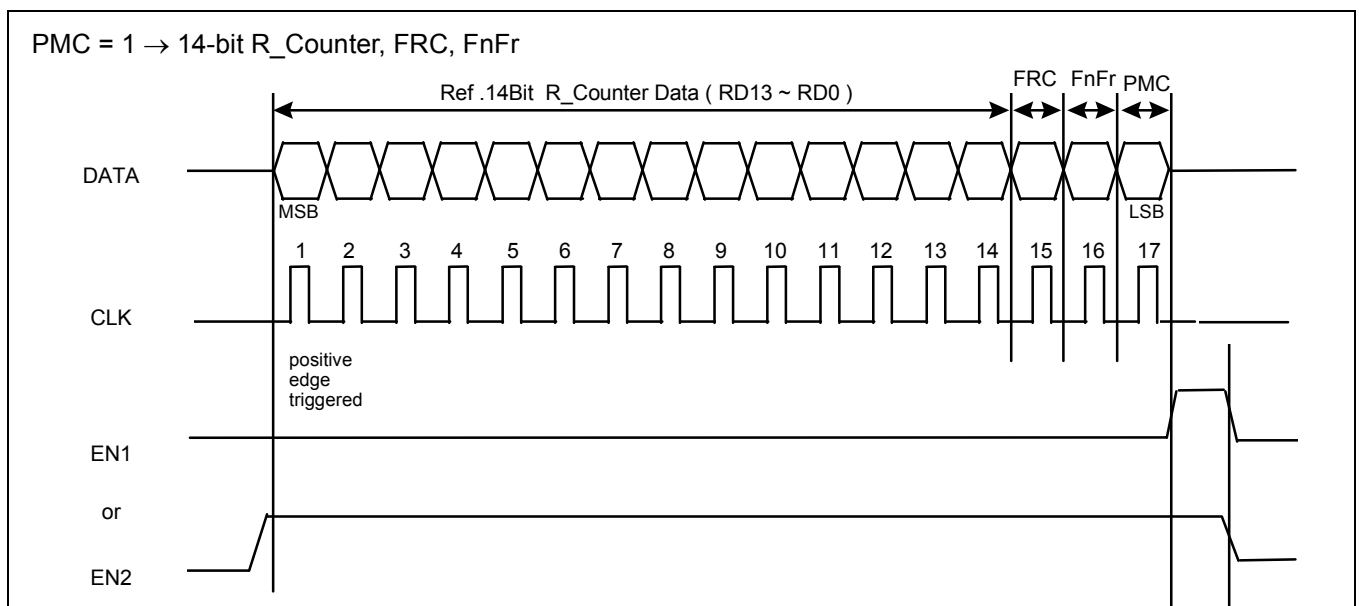


Figure 2. Ref. Register Programming Timing

- It is possible to use an optional selection of EN1, EN2 (when used EN)

Serial DATA Input Timing & Phase Detector / Lock Detector Output Waveforms

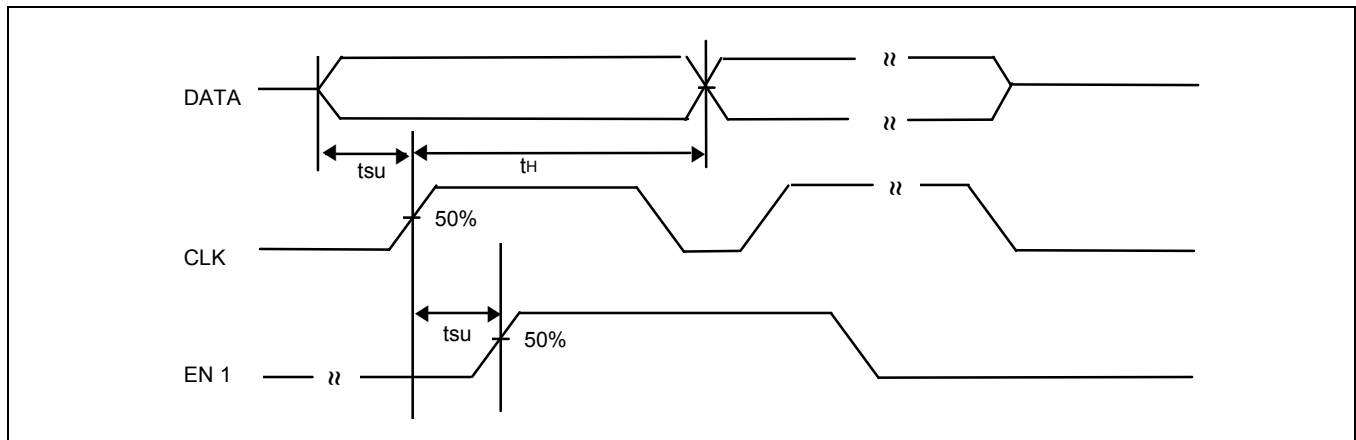


Figure 3. Serial Data Input Timing

The architecture of R-Count Divider

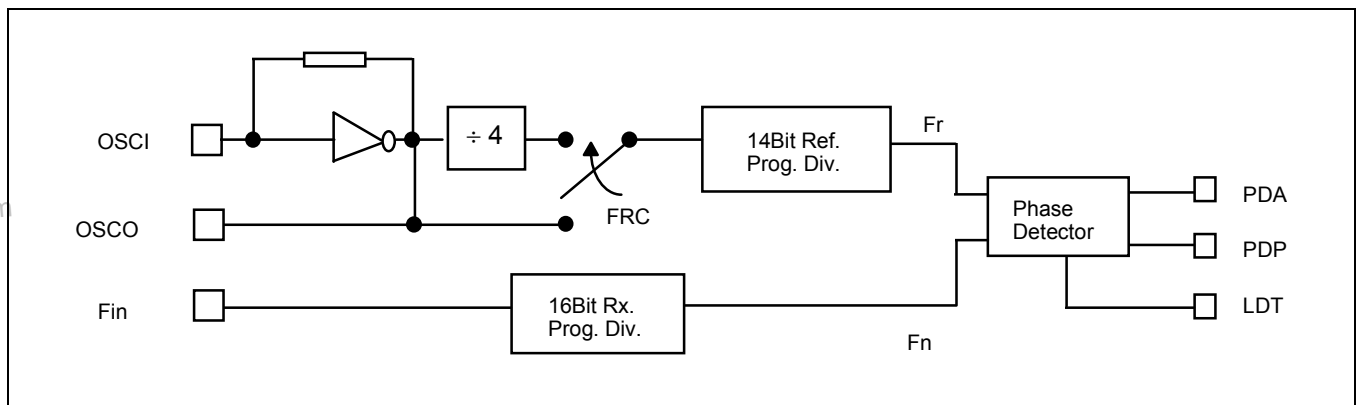


Figure 4. Phase Detector / Lock Detector Block Diagram

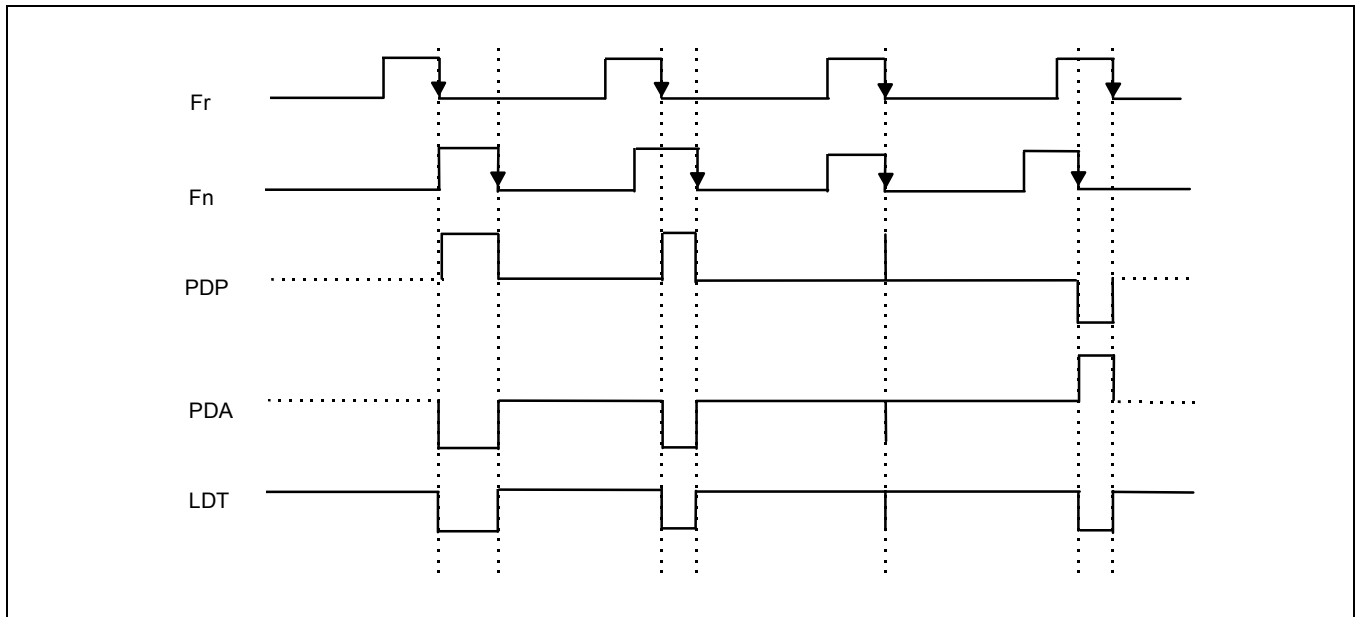


Figure 5. Phase Detector / Lock Detector Output Waveforms

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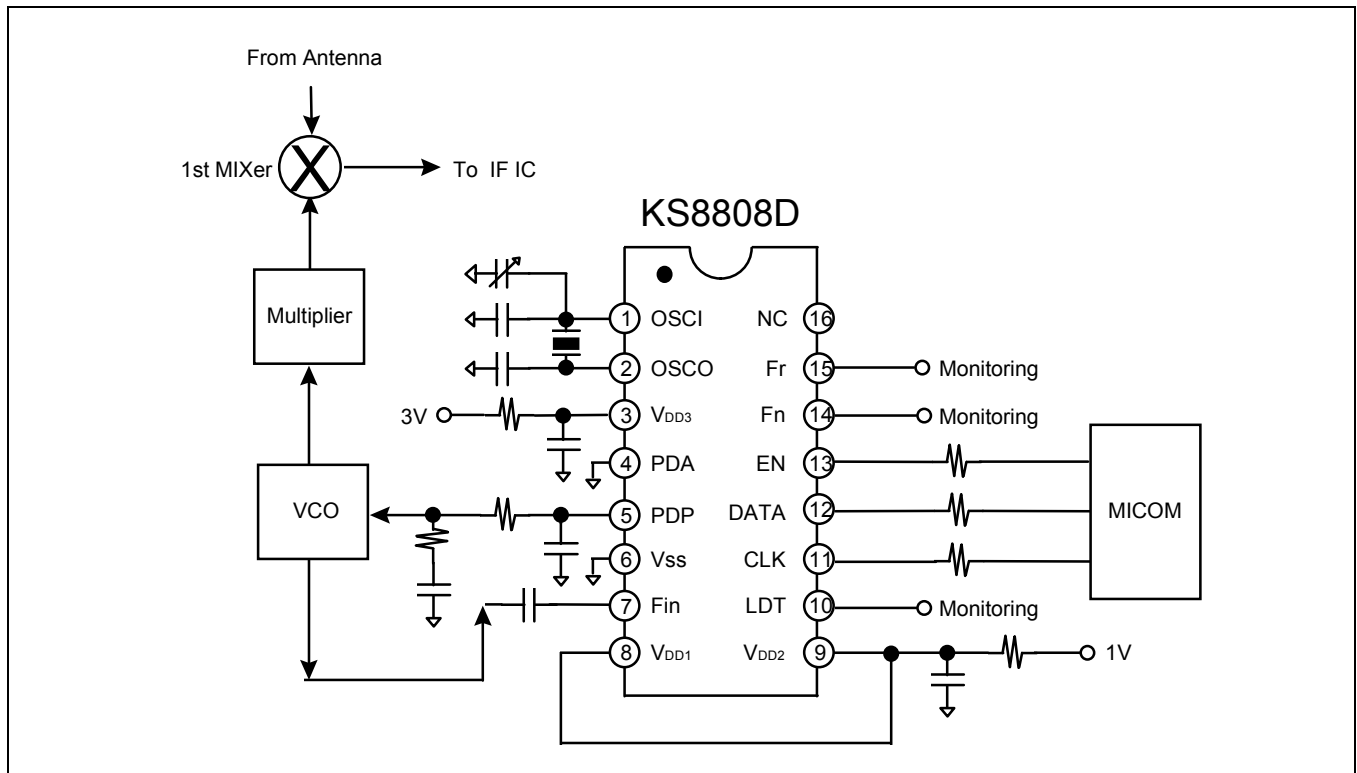
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ELECTRONICS

APPLICATION CIRCUIT



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