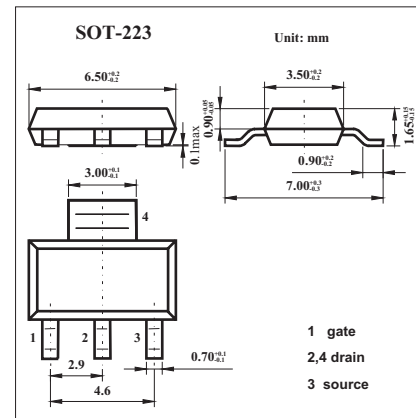
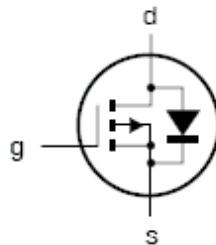


P-Channel Enhancement Mode Vertical D-MOS Transistor

KSP230

■ Features

- Direct interface to C-MOS, TTL, etc
- High-speed switching
- No secondary breakdown



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source voltage (DC)	V_{DS}	-300	V
Gate-source voltage (DC) open drain	V_{GSO}	± 20	V
Drain current (DC)	I_D	-210	mA
Peak drain current	I_{DM}	-0.75	A
Total power dissipation *	P_{tot}	1.5	W
Storage temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating junction temperature	T_j	150	$^\circ\text{C}$
thermal resistance from junction to ambient *	$R_{th\ j-a}$	83.3	K/W

*Device mounted on an epoxy printed-circuit board, 40 X 40 X 1.5 mm;
mounting pad for drain lead minimum 6 cm².

KSP230■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10\ \mu\text{A}$, $V_{GS} = 0\text{V}$	-300			V
Gate-source threshold voltage	V_{GSth}	$V_{DS} = V_{GS}$, $I_D = -1\ \text{mA}$	-1.7		-2.55	V
Drain-source leakage current	I_{DSS}	$V_{DS} = -240\text{V}$, $V_{GS} = 0\text{V}$			-100	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0$			± 100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$I_D = -170\ \text{mA}$, $V_{GS} = -10\text{V}$			17	Ω
Forward transfer admittance	$ y_{fs} $	$V_{DS} = -25\text{V}$, $I_D = -170\ \text{mA}$	100			mS
Input capacitance	C_{iss}	$V_{DS} = -25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\ \text{MHz}$		60	90	pF
Output capacitance	C_{oss}			15	30	
Reverse transfer capacitance	C_{rss}			5	15	
Turn-on time (See Fig.1and Fig.2)	t_{on}	$V_{GS} = 0\text{V to } -10\text{V}$, $I_D = -250\ \text{mA}$, $V_{DD} = -50\text{V}$,		5	10	ns
Turn-off time (See Fig.1and Fig.2)	t_{off}	$V_{GS} = -10\text{V to } 0\text{V}$, $I_D = -250\ \text{mA}$, $V_{DD} = -50\text{V}$,		15	30	

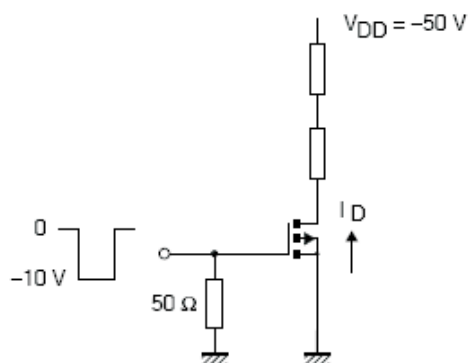


Fig.1 Switching time test circuit.

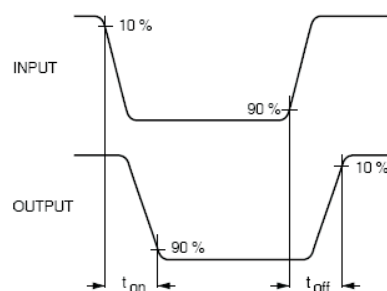


Fig.2 Input and output waveforms.