KTMicro, Inc.

Monolithic Digital Stereo FM Transmitter Radio-Station-on-a-Chip™

KT0801

▪ Features

Professional Grade System-on-a-Chip (SoC) High-Fidelity Stereo Audio FM Transmitter:
- **SNR ≥ 68 dB**
- **Stereo Separation > 50dB**
- **International compatible 76MHz ~ 108MHz**

Minimal External Component Requirement:
- **Crystal optional (in lieu of direct feeding of an external clock)**

Ultra-Low Power Consumption:
- **< 12.6 mA operation current**
- **< 1 µA standby current**

Dual Reference Clock Setup:
- **Supports both 7.6MHz and 15.2MHz**

Small Form factor:
- **24-pin 4x4x0.9 mm QFN (Pb-free and RoHS Compliant)**

Simple Interface:
- **Single 1.8V (in lieu of 1.6~3.6V regulator feed)**
- **Industry standard 2-wire I²C MCU interface compatible**

Advanced Digital Audio Signal Processing:
- **On-chip 20-bit ΔΣ Audio ADC**
- **On-chip DSP core**
- **On-chip 24dB PGA**
- **Automatic calibration against process and temperature**

On-Chip LDO (low-drop-out) regulator:
- **Accommodates 1.6V ~ 3.6V supply**

Programmable transmit level

Programmable pre-emphasis (50/75 µs)

Applications

MP3 Players
Cellular Phones
PDAs
Portable Personal Media player
Laptop Computers
Wireless Speakers

Rev. 1.0

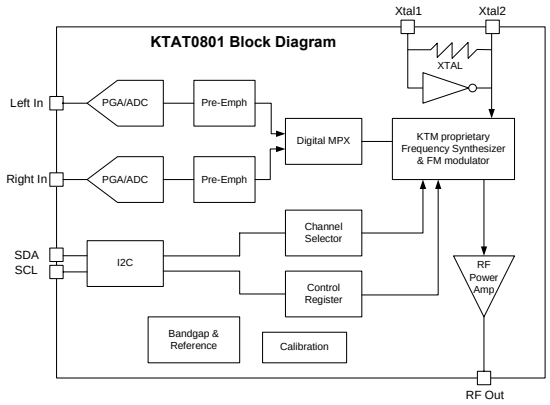

Figure 1: KT0801 System Diagram

▪ General Description

The KT Micro KT0801 Monolithic Digital FM Transmitter is designed to process high-fidelity stereo audio signal and transmit modulated FM signal over a short range. The modulated stereo FM signal can be intercepted and played back using any FM radio worldwide.

The KT0801 features dual 20-bit ΔΣ audio ADCs, a high-fidelity digital stereo audio processor and a fully integrated radio frequency (RF) transmitter. An on-chip low-drop-out regulator (LDO) allows the chip to be integrated in a wide range of low-voltage battery-operated systems with power supply ranging from 1.6V to 3.6V.

The KT0801 is configured as an I²C slave and programmed through the industry standard 2-wire MCU interface.

Thanks to its high integration level, the KT0801 is mounted in a generic 24-pin 4x4 QFN package and only requires a single low-voltage supply and a small-form-factor crystal (7.6MHz or 15.2MHz) or an external clock to operate.

No external tuning is required that makes design-in effort minimum.

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▪ Operation Condition

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
1.8V Analog Supply[1]	VDD	Relative to GND	1.6	1.8	2.0	V
IO/Regulator Supply	IOVDD	Relative to GND	1.6		3.6	V
Operating Temp	T_A	Ambient Temperature	-30	25	85	°C
Note: 1. When LDO enabled, no external voltage should be applied to this 1.8V supply.						

▪ Specifications and Features

Table 2: FM Transmitter Functional Parameters (Unless otherwise noted TA = -30~85 °C, IOVDD=1.6~3.6 V with LDO enabled, F_{in} = 1 kHz)

Parameter	Symbol	Test/Operating Condition	Min	Nom	Max	Units
FM Frequency Range	F_{tx}	Pin 19	76		108	MHz
Current Consumption	I_{VDD}	Pin 1 with PA (power amp.) at default power mode	-	10	12.6	mA
Standby Current	I_{stand}	Pin 1	-	0.1	1	µA
Signal to Noise Ratio	SNR	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	68	-	dB
Total Harmonic Distortion	THD	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	0.1		%
Left/Right Channel Balance	BAL	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-0.2	-	0.2	dB
Stereo Separation (Left<->Right)	SEP	V_{in} = 0.7 V_{p-p}, G_{in} = 0	50	60	-	dB
Sub Carrier Rejection Ratio	SCR	V_{in} = 0.7 V_{p-p}, G_{in} = 0	-	-	-60	dB
Input Swing[1]	V_{in}	Single-ended input	-	0.3	1.2	V_{RMS}
PGA Range for Audio Input	G_{in}		-12	0	12	dB
PGA Gain Step for Audio Input	G_{step}			4		dB
Required Input Common-Mode Voltage when DC-coupled	V_{cm}	Pin 4, 6	0	0.8	1.8	V
Power Supply Rejection[2]	PSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Ground Bounce Rejection[2]	GSRR	IOVDD = 1.9 ~ 3.6 V	40	-	-	dB
Input Resistance (Audio Input)	R_{in}	Pin 4, 6	120	150	180	kΩ
Input Capacitance (Audio Input)	C_{in}	Pin 4, 6	0.5	0.8	1.2	pF
Audio Input Frequency Band	F_{in}	Pin 4, 6	20	-	15k	Hz
Transmit Level	V_{out}	Spectrum analyzer (50 Ω)	93	99	104	dBµV
Channel Step	STEP		-	100		kHz
Pre-emphasis Time Constant	T_{pre}	SIG_PROC<1> = 1	-	50	-	µs
		SIG_PROC<0> = 0	-	75	-	µs
Crystal/External Clock	CLK	Dual-frequency setup	-	7.6 or 15.2	-	MHz
2-wire I^2C Clock	SCL	Pin 17	0	100	400	kHz
High Level Input Voltage	V_{IH}	Pin 3, 9, 10, 12, 13, 16, 17, 24	0.75 x IOVDD	-	IOVDD + 0.25	V
Low Level Input Voltage	V_{IL}	Pin 3, 9, 10, 12, 13, 16, 17, 24	- 0.25	-	0.25 x IOVDD	V

Notes:
1. Maximum is given on the condition of PGA gain = -12dB.
2. Fin = 20 ~ 15k Hz.

▪ Package and Pin List

A 24-pin QFN package is used. The chip IO pin-out is listed in Table 3.

Table 3 KT0801 Pin-Out

Pin Index	Name	I/O Type	Function
1	IOVDD	Power	1.6~3.3V external logic IOVDD or Regulator high supply input.
2, 14, 18, 22	VDD	Power	1.8V supply. No external voltage shall be applied with regulator enabled. All four pins shall be shorted on the PCB.
3	HF	Digital Input	"1" to enable 15.2MHz XTAL mode. Default "0", 7.6MHz XTAL mode.
4	INL	Analog Input	Left channel audio input.
5, 11, 15, 20, 21	GND	Ground	Ground.
6	INR	Analog Input	Right channel audio input.
7	NC1	N/A	Reserved. Do not connect.
8	NC2	N/A	Reserved. Do not connect.
9	SW1	Digital Input	Control bit. Chip enable, supply mode and clock source.
10	SW2	Digital Input	Control bit. Chip enable, supply mode and clock source.
12	RSTB	Digital Input	Reset (active low).
13	ADDR	Digital Input	Set the 4th I2C address bit (MSB being the 1st bit).
16	SDA	Digital I/O	Serial data I/O.
17	SCL	Digital I/O	Serial clock input.
19	PA_OUT	Analog Output	FM RF output.
23	XI	Analog I/O	Crystal input.
24	XO/RCLK	Analog I/O	Crystal input or external reference clock input.

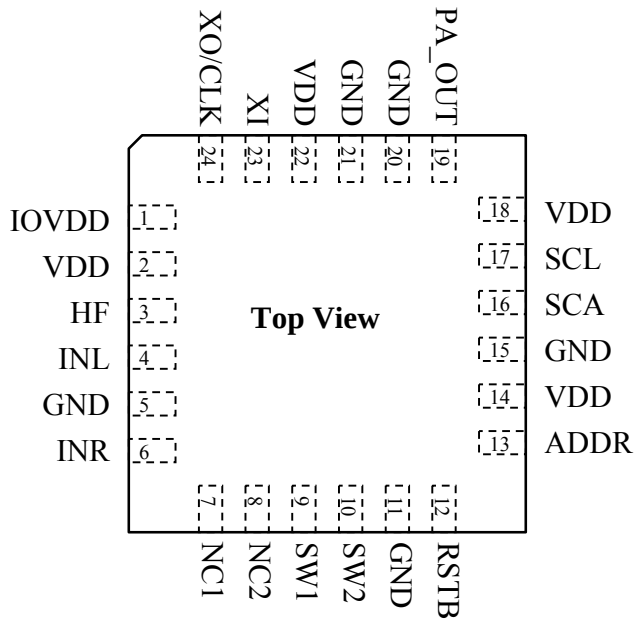


Figure 2: KT0801 Pin-out: 4x4 24-Pin QFN Package.

▪ I²C Compatible 2-Wire Serial Interface

General Descriptions

The serial interface consists of a serial controller and registers. An internal address decoder transfers the content of the data into appropriate registers. Both the write and read operations are supported according to the following protocol:

The write operation is accomplished via a 3-byte sequence:

Serial address with write command
Register address
Register data

The read operation is accomplished via a 4-byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

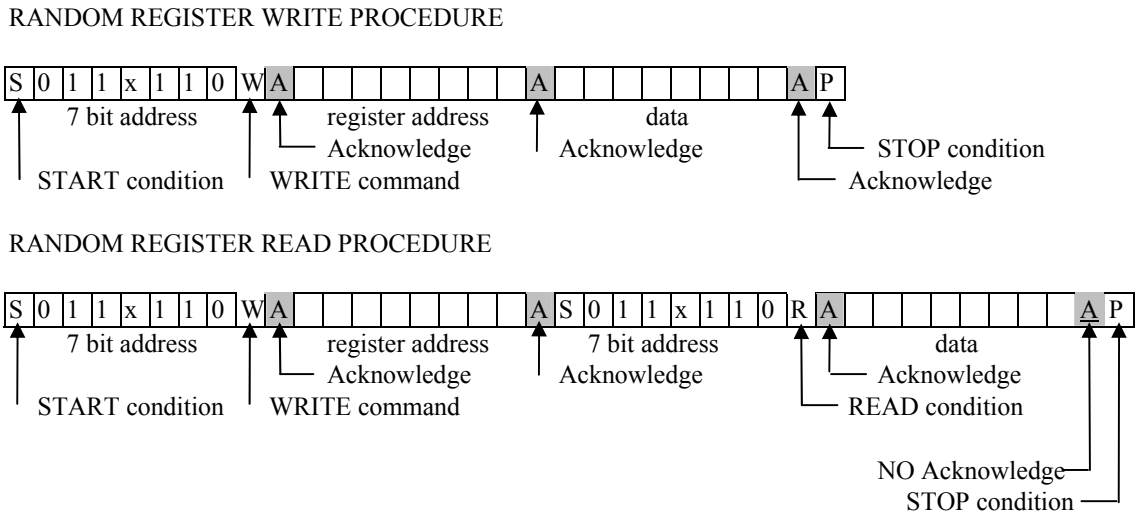


Figure 3: Serial Interface Protocol

The x is the optional 4th MSB bit address code that is set by the ADDR pin and is provided to allow a dual-transmitter-single-controller configuration that will enable multi-channel surround sound applications. ADDR must be externally tied to ground or IOVDD for low or high setup, respectively. The serial controller supports slave mode only. Any register can be addressed randomly.

Slave Mode Protocol

With reference to the clocking scheme shown in Figure 4, the serial interface operates in the following manner:

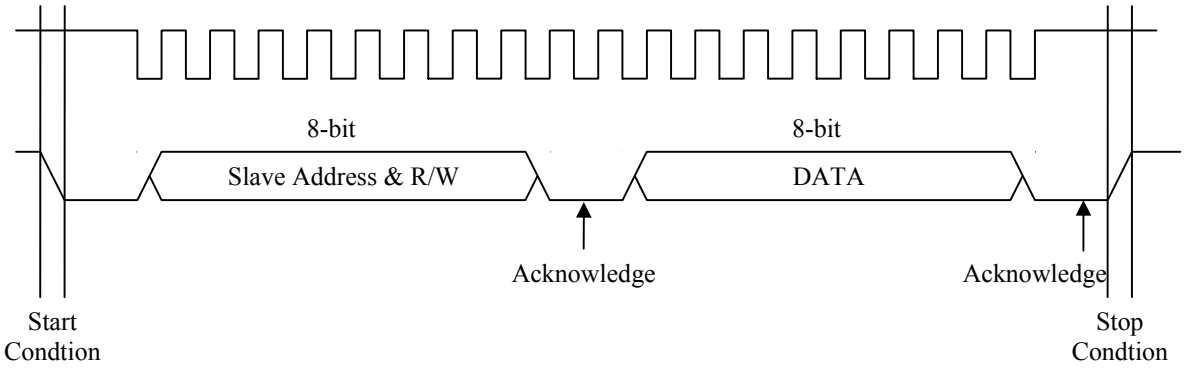


Figure 4: Serial Interface Slave Mode Protocol

A START condition is defined as a HIGH to LOW transition on the data line while the SCLK line is held high. After this has been transmitted by the controller (Master), the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the 8th bit tells whether the master is receiving data from the slave or transmitting data to the slave. When ADDR is set to "0" (i.e. tied to ground), the I^2C write address is 0x6C and the read address is 0x6D.

Data transfer with acknowledge is obligatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the SDA line LOW so that it remains stable during the HIGH period of the acknowledge clock pulse. A receiver that has been addressed is obligated to generate an acknowledge signal after each byte of data has been received.

▪ Register Bank

The register bank stores channel frequency codes, calibration parameters, operation status, mode and power controls, which can be accessed by the internal digital controller, state machines and external micro controllers through the serial interface.

All registers are 8 bits wide. Control logics are active high unless specifically noted.

CH_SEL0 (Address: 0x00, Default: 0x81)

Bits	Type	Default	Label	Description
7:0	RW	0x81	CHSEL[7:0]	FM Channel Selection[7:0]

CHSEL[10:0] definition : Channel selection code. 0 to 108 MHz with 100 kHz step. 0x000 corresponds to 0Hz; 0x001 corresponds to 100 kHz, and so on.

CH_SEL1 (Address: 0x01, Default: 0x03)

Bits	Type	Default	Label	Description
7:6	RW	0x0	RFGAIN[1:0]	Transmission Range Adjust 00: Lowest Range 01: Low Range 10: High Range 11: Highest Range

Bits	Type	Default	Label	Description
5:3	RW	0x0	PGA[2:0]	Input Audio Gain Control 111: 12dB 110: 8dB 101: 4dB 100: 0dB 000: 0dB 001: -4dB 010: -8dB 011: -12dB
2:0	RW	0x3	CHSEL[10:8]	FM Channel Selection[10:8]

SIG_PROC (Address: 0x02, Default: 0x00)

Bits	Type	Default	Label	Description
7:4	RW	0x0	NA	Reserved
3	RW	0	MUTE	Software control of Mute 1: MUTE Enable 0: MUTE Disable
2	RW	0	PLTADJ	Pilot Tone Amplitude Adjustment 1: Amplitude high 0: Amplitude low
1	RW	0	NA	Reserved
0	RW	0	PHTCNST	Pre-Emphasis Time-Constant Set 1: 50uS (Europe, Australia) 0: 75uS (USA, Japan)

PA_PWR (Address: 0x13, Default: 0x00)

Bits	Type	Default	Label	Description
7	RW	0	PA_HI_PW	PA (Power amplifier) power (combined with CH_SEL1<7:6> to set up transmission range) 1: Enable high power 0: Disable high power
6:0	RW	0x0	NA	Reserved

Chip Enable and Mode Control (Pin SW1 and SW2)

There are 2 external Pins SW1 and SW2 (Pin 9 and 10) which enable chip and define the supply voltage level and clock source of the chip. The definition is shown in Table 4.

Table 4: Pin SW1 and SW2 vs. Chip Supply and Clock Source

Input SW1/2	Chip Mode	Chip Supply	Clock Source
00	Disabled	N/A	External
01	Bypass XTAL	Lo-V (1.6~2.0V)	External
10	LDO Disabled	Lo-V (1.6~2.0V)	XTAL
11	LDO Enabled	Hi-V (1.6~3.6V)	XTAL

Application note 1: In low supply mode (1.6 ~ 2.0V) and operate with LDO disabled, tie SW2 to ground and use SW1 as the chip enable. For high supply mode and operate with LDO enabled, short SW2 to SW1 and use both as chip enable.

Application note 2: In low supply mode, IOVDD (Pin 1) shall be tied to the system supply which is equal to the logic level "High" from the MCU/system.

▪ Typical Application Circuits

The KTAT08001 can be integrated in a wide range of systems by requiring only a single power supply. Figure 5 shows a configuration with zero external components. Figure 6 and Figure 7 show two typical configurations in 1.8V and 3.3Vsystems, respectively.

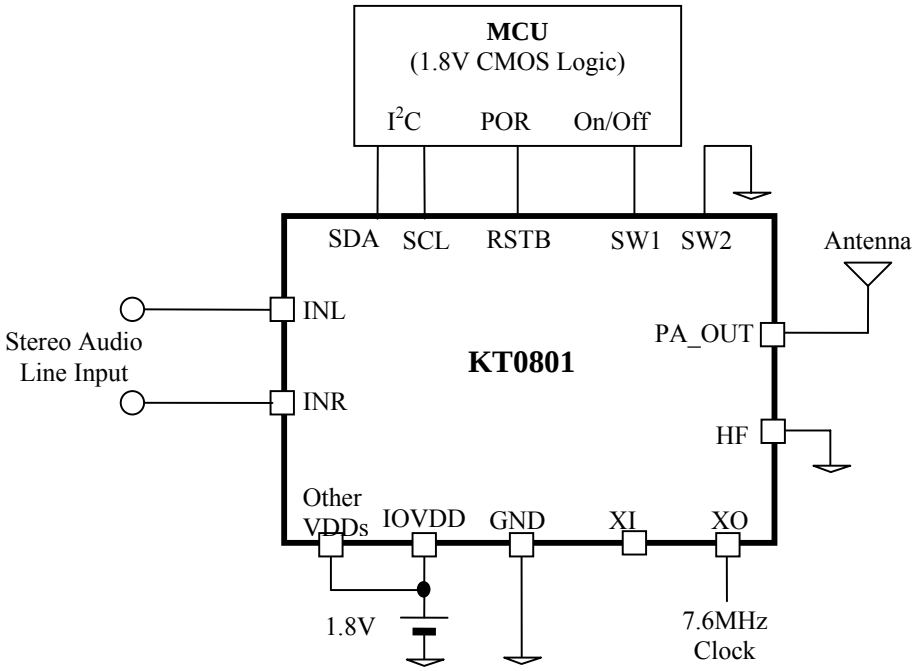


Figure 5: Zero external components configuration in 1.8V systems.

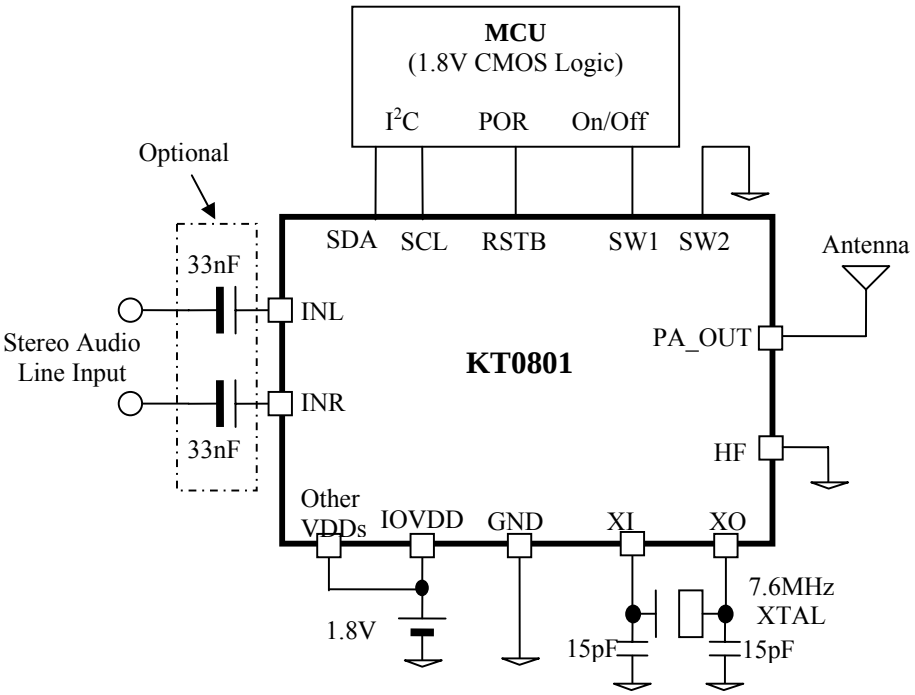


Figure 6: Typical Application configuration in 1.8V systems.

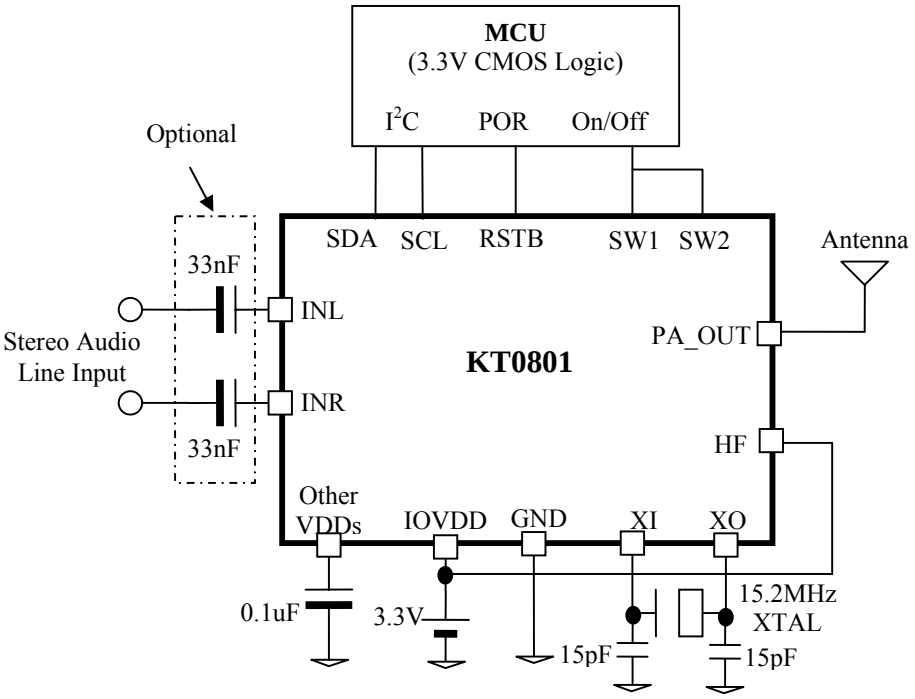
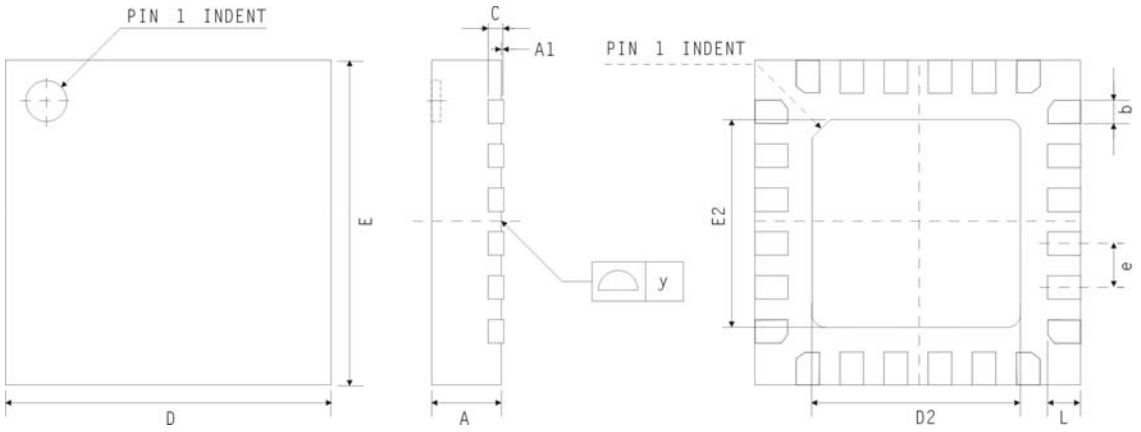


Figure 7: Typical Application configuration in 3.3V system.

▪ Package Outline



Symbols	(MILLIMETERS)		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C	0.19	0.20	0.25
D	3.95	4.00	4.05
D2	2.65	2.70	2.75
E	3.95	4.00	4.05
E2	2.65	2.70	2.75
e	-	0.5	-
L	0.30	0.40	0.50
y	0.00	-	0.076