# 10-/12-Bit Quad Voltage Output DACs

## Features

- KTA5314:4 buffered 10-Bit DACs in MSOP10L
- KTA5324:4 buffered 12-Bit DACs in MSOP10L
- Low power operation: 500uA @ 3V,
  600uA @ 5V
- 2.5V to 5.5V power supply
- Power-down to 80nA @ 3V,200nA @ 5V
- Double-buffered input logic
- Output range:0V to
- Power-on reset to 0V
- On-chip, rail-to-rail output buffer amplifiers
- Temperature range -40$^{\circ}$C to +105$^{\circ}$C

## Applications

- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
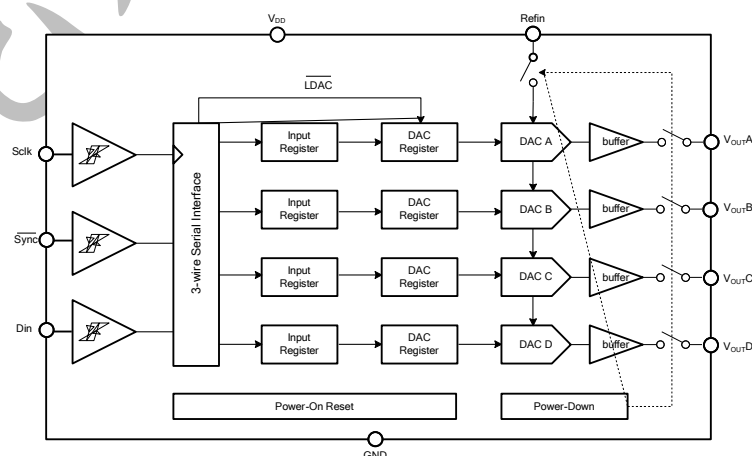- Programmable attenuators
- Industrial process controls

## General Description

The KTA5314/KTA5324 are quad 10- and 12-bit buffered voltage output DACs in MSOP10L packages that operate from a single 2.5V to 5.5V supply, consuming only 500uA at 3V. They have on-chip rail-to-rail output amplifiers with slew rate of 0.7V/us. A 3-wire serial interface compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards is used, which can operates at clock rates up to 30MHz.

The references for the four DACs are derived from one reference pin. The outputs of all DACs can be updated simultaneous. It incorporate a power-on reset circuit, and ensure that the DAC outputs power up to 0V and remains there until a valid write takes place to the device. The parts contain a power-down feature that reduces the current consumption to 200nA @ 5V (80nA @ 3V).

## Functional Block Diagram



Figure 1 Functional Block Diagram

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# Figure

# Table

# 1. Typical Application Circuit



Figure 2 KTA5314/KTA5324 Typical Application Circuit

## 2. Absolute Maximum Ratings

Table 1

=25℃,unless otherwise noted.

| Parameter[1] | Sym | Rating |
|---|---|---|
| to GND | $V_{DDabs}$ | -0.3V to+7V |
| Digital Input Voltage to GND | $V_{Digabs}$ | -0.3V to +0.3V |
| Reference Input Voltage to GND | $V_{refabs}$ | -0.3V to +0.3V |
| A through to GND | $V_{outabs}$ | -0.3V to +0.3V |
| Operating Temperature Range<br>Industrial | $T_P$ | -40℃ to +105℃ |
| Storage Temperature Range | $T_S$ | -65℃ to +150℃ |
| Junction Temperature | $T_{Jmax}$ | 150℃ |
| Reflow Soldering<br>Peak Temperature(Pb-free) | | 260℃ |
| Peak Temperature(non Pb-free) | | 220℃ |
| Time at Peak Temperature | | 10 sec to 40 sec |

✧　　1. Transient currents of up to 100mA do not cause SCR latchup.

# 3. Recommended Operation Conditions

Table 2

| Parameter | Sym | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power supply | $V_{DD}$ | 2.5 | 5.5 | V |
| Current dissipation | $I_{DD}$ | 400u | 600u | A |
| Ambient Temperature | $T_a$ | -40 | 105 | ℃ |

# 4. Specifications

Table 3

$V_{DD}$=2.5V to 5.5V; $V_{REF}$=2V; $R_L$=2K$\Omega$ ; $C_L$=200pF to GND; $T_a$=25℃; unless otherwise noted.

| Parameter | Sym | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DC Performance[1,2]** | | | | | | |
| KTA5314 | | | | | | |
| Resolution | $Res_N$ | | | 10 | | Bits |
| Relative Accuracy | INL | | | ± 0.5 | | LSB |
| Differential Nonlinearity | DNL | Monotonic Guaranteed | | ± 0.05 | | LSB |
| KTA5324 | | | | | | |
| Resolution | $Res_N$ | | | 12 | | Bits |
| Relative Accuracy | INL | | | ± 2 | | LSB |
| Differential Nonlinearity | DNL | Monotonic Guaranteed | | ± 0.2 | | LSB |
| Offset Error | | | | ± 0.4 | | %of FSR |
| Gain Error | | | | ± 0.15 | | %of FSR |
| Lower Dead Band | | Lower dead band exists only if offset error is negative | | 20 | | mV |
| DC Power Supply Rejection Ratio[3] | PSRR | | | -60 | | dB |
| DC Crosstalk[3] | | $\Omega$ | | 200 | | uV |
| **Reference Input[3]** | | | | | | |
| Input Range | | | 0.25 | | $V_{DD}$ | V |
| Input Impedance | | | | 45 | | K$\Omega$ |
| Reference Feedthrough | | Frequency=10KHz | | -80 | | dB |
| **Output Characteristics[3]** | | | | | | |
| Minimum Output Voltage[4] | | | | 0 | | V |
| Maximum Output Voltage[4] | | | | $V_{DD}$ | | V |
| DC Output Impedance | | | | 0.5 | | $\Omega$ |
| Short Circuit Current | | | | 25 | | mA |
| Power-Up Time | | | | 5 | | uS |
| **Logic Input[3]** | | | | | | |
| Input Low Voltage | | $V_{DD}$=3V | | | 0.6 | V |
| Input High Voltage | | $V_{DD}$=3V | | | 2.1 | V |
| Pin Capacitance | | | | 3 | | pF |
| **Power Requirements** | | | | | | |
| Power supply (Normal Mode)[4] | $V_{DD}$ $I_{DD}$ | | 2.5 | | 5.5 | V |

| Parameter | Sym | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| =4.5V to 5.5V | | | | 600 | | uA |
| =2.5V to 3.6V | | | | 500 | | uA |
| (Power-Down Mode) | | | | | | |
| =4.5V to 5.5V | | | | 0.2 | | uA |
| =2.5V to 3.6V | | | | 0.08 | | uA |

1 DC specifications tested with the outputs unloaded.

2 Linearity is tested using a reduced code range KTA5314(Code 28 to Code 995); KTA5324(Code 115 to Code 3981).

3 Guaranteed by design and characterization, not production tested.

4 For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage,

and offset plus gain error must be positive.

5   specification is valid for all DAC codes; interface inactive; all DACs active; load currents excluded.

# 5. AC Characteristics

Table 4

$V_{DD}$=2.5V to 5.5V; $V_{REF}$=2V; $R_L$=2K$\Omega$ ; $C_L$=200pF to GND; $T_a$=25$^\circ$C; unless otherwise noted.

| Parameter[1] | Sym | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage Setting Time | | | | | | |
| KTA5314 | | 1/4 scale to 3/4 scale change(0x100 to 0x300) | | 7 | | uS |
| KTA5324 | | 1/4 scale to 3/4 scale change(0x100 to 0x300) | | 8 | | uS |
| Slew Rate | | | | 0.7 | | V/uS |
| Major-Code Transition Glitch Energy | | 1 LSB change around major carry | | 40 | | nV-sec |
| Digital Feedthrough | | | | 1 | | nV-sec |
| Digital Crosstalk | | | | 1 | | nV-sec |
| DAC-to-DAC Crosstalk | | | | 3 | | nV-sec |
| Multiplying Bandwidth | | | | 200 | | kHz |
| Total Harmonic Distortion | | | | -70 | | dB |

1 Guaranteed by design and characterization, not production tested.

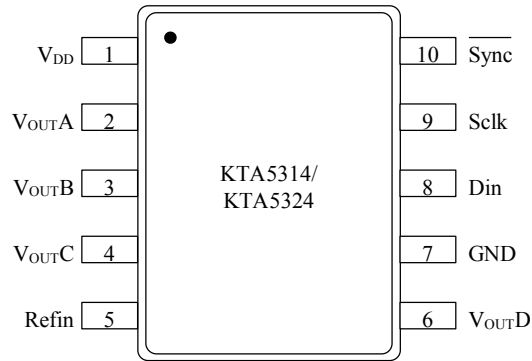# 6. Pin Configurations And Function Descriptions

## 6.1 Pin Configurations



Figure 3. MSOP10L Pin Configuration

## 6.2 Pin Function Descriptions

Table 5

| Pin Name | Pin No. | Function | Description |
|---|---|---|---|
| | 1 | Power | Power Supply Input. These parts can be operated from 2.5V to 5.5V and the supply can be decoupled to GND. |
| | 2 | O | Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation. |
| | 3 | O | Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation. |
| | 4 | O | Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation. |
| Refin | 5 | I | Reference Input Pin for All Four DACs. It has an input range from 0.25V to . |
| | 6 | O | Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation. |
| GND | 7 | Ground | Ground Reference Point for All Circuitry on the Part. |
| Din | 8 | I | Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The Din input buffer is powered down after each write cycle. |
| Sclk | 9 | I | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30MHz. The Sclk input buffer is powered down after each write cycle. |
| | 10 | I | Active Low Control Input. This is the frame synchronization signal for the input data. When goes low, it enables the input shift register and data is transferred in on the falling edges of the following 16clocks. If is taken high before the falling edge of Sclk, the rising edge of acts as an interrupt and the write sequence is ignored by the device. |

I：Input, O：Output

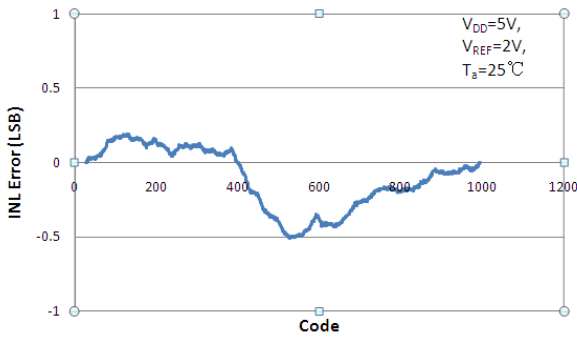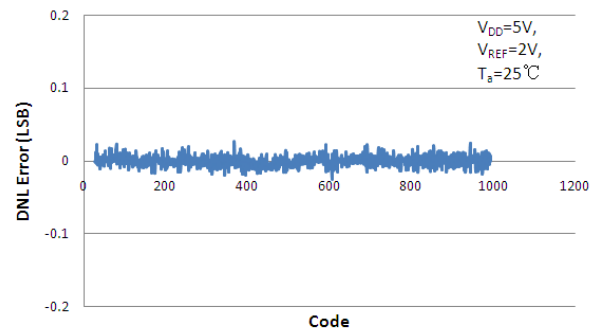## 7. Typical Performance Characteristic

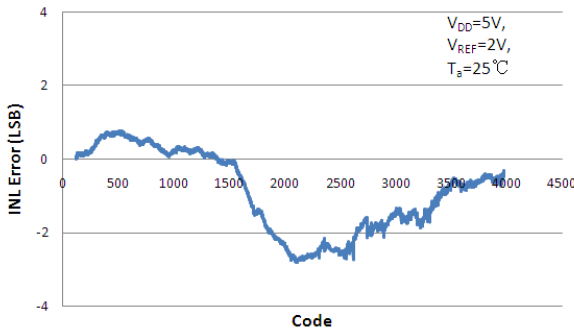Figure 4. KTA5314 Typical INL Plot

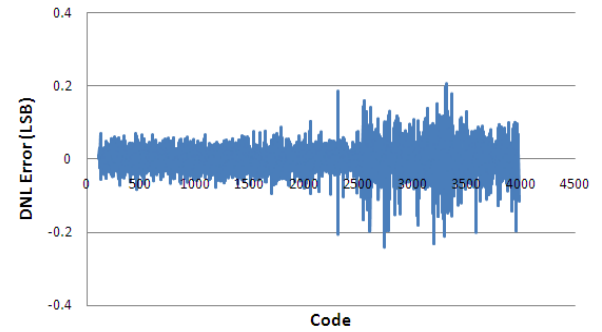Figure 6. KTA5314 Typical DNL Plot

Figure 5. KTA5324 Typical INL Plot

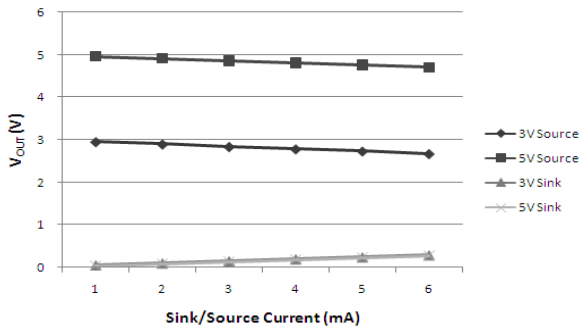Figure7. KTA5324 Typical DNL Plot
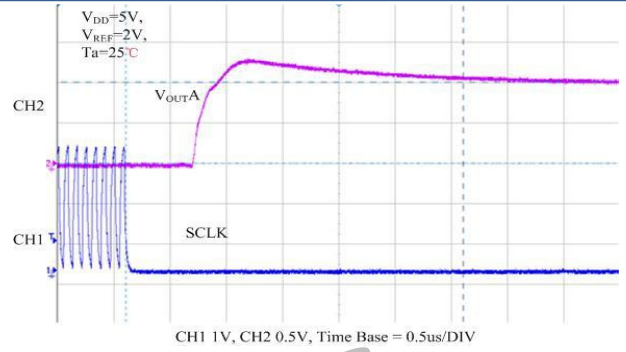
Figure8. Vout Source and Sink Current Capability



Figure10. Exiting Power-down to Midscale
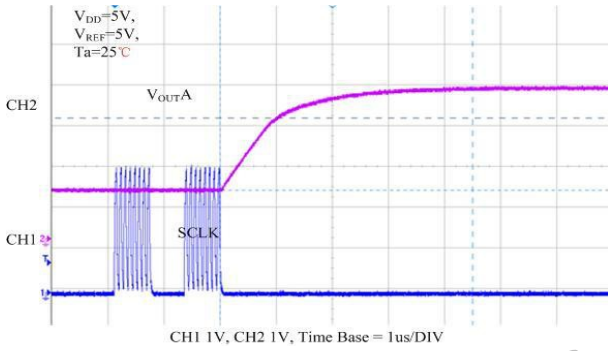


Figure9. Half-scale setting (0.25 to 0.75 Scale Code

Change)

# 8. Theory Of Operation

## 8.1 Functional Description

The KTA5314/KTA5324 are quad, resistor-string DACs fabricated on a CMOS process with resolutions of 10 and 12 bits, respectively. Each contains four output buffer amplifiers and is written to via a 3-wire serial interface. They operate from single supplies of 2.5V to 5.5V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/us. The four DACs share a single reference input pin. The devices have programmable power-down modes, in which all DACs can be turned off completely with a high impedance output.

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the Refin pin provides the reference voltage for the DAC. The input coding to the DAC is straight binary, the ideal output voltage is given by

$$\rule{2cm}{1pt}$$ ................................................... formula 1

Where D=decimal equivalent of the binary code that is loaded to the DAC register:

0—1023 for KTA5314(10 bits)

0—4095for KTA5324(12bits)

N=DAC resolution.

There is a single reference input pin for the four DACs. The reference input is not buffered. The user can have a reference voltage as low as 0.25V or as high as VDD because there is no restriction due to the headroom or footroom requirements of any reference amplifier. It is recommended to use a buffered reference in the external

circuit. The input impedance is typical 45k$\Omega$.

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to          when the reference is       . It is capable of driving a load of 2k$\Omega$   to GND or       , in parallel with 500pF to GND or       . The slew rate is 0.7V/us with a half-scale settling time to $\pm$ 0.5LSB(at 12 bits) of 8us.

The KTA5314/KTA5324 are provided with a power-on reset function, so that they power up in a defined state. The power-on state uses normal operation and an output voltage set to 0V. Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device.

The KTA5314/KTA5324 are controlled over a versatile, 3-wire serial interface that operates at clock rates up to 30MHz and are compatible with SPI,QSPI,MICROWIRE, and DSP interface standards.

## 8.2 The 3-wire serial interface

### 8.2.1 Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, Sclk. The 16-bit word consists of four control bits followed by 10 or 12 bits of DAC data, depending on the device type. Data is loaded MSB first (Bit15) and the first two bits determine whether the data is for DAC A ,DAC B ,DAC C, or DCA D. Bit 13 and Bit 12 control the operating mode of the DAC. Bit 13 is      , and determines whether the part is in normal or power-down mode. Bit 12 is      , and controls when DAC registers and outputs are updated.

Table 6 Address Bits

| A1 | A0 | DAC Addressed |
|---|---|---|
| 0 | 0 | DAC A |
| 0 | 1 | DAC B |
| 1 | 0 | DAC C |
| 1 | 1 | DAC D |

Control Bits

　 0: All four DACs go into power-down mode, consuming only 200nA @ 5V. The DAC outputs enter a high impedance state.

　 1: Normal operation.

　　 0: All four DAC registers and, therefore, all DAC outputs updated simultaneously on completion of the write sequence.

　 1: Only addressed input register is updated. There is no change in the content of the DAC registers.

The KTA5324 uses all 12 bits of DAC data; the KTA5314 uses 10 bits and ignores the 2 LSB Bits. The data format is straight binary, with all 0s corresponding to 0V output and all 1s corresponding to full-scale output (

　 ).

The      input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while      is low. To start the serial data transfer, take      low. After      goes low, serial data shifts into the device's input shift register on the falling edges of Sclk for 16 clock pulses. Any data and clock pulses after the      falling edge of Sclk are ignored because the Sclk and Din input buffers are powered down. No further serial data transfer occurs until      is taken high and low again.      can be taken high after the falling edge of the      Sclk pulse.

After the end of the serial data transfer, data automatically transfers from the input shift register to the input register of the selected DAC. If      is taken high before the      falling edge of Sclk, the data transfer is aborted and the DAC input registers are not updated.

When data has been transferred into three of the DAC input registers, all DAC registers and all DAC outputs are simultaneously updated by setting      low when writing to the remaining DAC input register.

## 8.2.2 Low Power Serial Interface

To reduce the power consumption of the device even further, the interface fully powers up only when the device is being written to, that is , on the falling edge of        . As soon as the 16-bit control word has been written to the part, the Sclk and Din input buffers are powered down. They power up again only following a falling edge of        .

## 8.2.3 Double-Buffered Interface

The KTA5314/KTA5324 DACs have double-buffered interfaces consisting of two banks of registers‐input

registers and DAC registers. The input register is directly connected to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the        bit. When the        bit is set high, the DAC register is latched and hence the input register can change state without affecting the contents of the DAC register. However, when the        bit is set low, all DAC registers are update after a complete write sequence.

This is useful if the user requires simultaneous updating of all DAC outputs. The user can write to three of the input registers individually and then, by setting the        bit low when writing to the remaining DAC input register, all outputs update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been update since the last time that        was brought low. Normally, when        is brought low, the DAC registers are filled with the contents of the input register. In the case of the KTA5314/KTA5324 the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

## 8.3 Power-Down Mode

The KTA5314/KTA5324 have low power consumption, dissipation only 1.5mW with a 3V supply and 3mW with a 5V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, selected by a 0 on Bit 13 (        ) of the control word.

When the        bit is set to 1, all DACs work normally with a typical power consumption of 600uA at 5V (500uA at 3V ). However, in power-down mode, the supply current falls to 200nA at 5V (80nA at 3V) when all DACs are powered down. Not only does the supply current drop, but also the output stage is internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the output is three-stated while the part is in power-down mode, and provides a defined input condition for whatever is connected to the output of the DAC amplifier.

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 5us. This is the time from the falling edge of the        Sclk pulse to when the output voltage deviates from its power down voltage.

# 9. Application Information

## 9.1 Typical Application Circuit

The KTA5314/KTA5324 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0V to      . More typically, these devices are used with a fixed, precision reference voltage.

If an output range of 0V to      is required, the simplest solution is to connect the reference input to      . As this supply is not very accurate and can be noisy, the KTA5314/KTA5324 can be powered from the reference voltage; for example, using a 5V reference. The current required is 600uA supply current and approximately 112uA into the reference input. This is with no load on the DAC outputs. When the DAC outputs are loaded, the reference also needs to supply the current to the loads.

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## 9.2 Decoding Multiple KTA5314/KTA5324

The        pin on the KTA5314/KTA5324 can be used in applications to decode a number of DACs. In this application, all the DACs in the system receive the same serial clock and serial data, but        can only be active to one of the devices at any one time, allowing access to only one DAC in this system. The 74HC139 can be used as a 2-to-4-line decoder to address any of the DACs in the system. To prevent timing errors, the enable input must be brought to its inactive state while the coded address inputs are changing state.

## 9.3 Power Supply Bypassing and Grounding

  In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the KTA5314/KTA5324 is mounted is designed so that the analog and digital sections are separated and confined to certain areas of the board. If the KTA5314/KTA5324 are in a system where multiple devices require an AGND-to-DGND connection, the connection is made at one point only. The star ground point is established as close as possible to the device. The KTA5314/KTA5324 has ample supply bypassing of 10uF in parallel with 0.1uF on the supply located as close to the package as possible, ideally right up against the device. The 10uF capacitors are the tantalum bead type. The 0.1uF capacitor has low effective series resistance (ESR) and effective series inductance (ESI).

The power supply lines of the KTA5314/KTA5324 use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks are shielded with digital ground to avoid radiating noise to other parts of the board, and are never run near the reference inputs .Avoid crossover of digital and analog signals. Traces on opposite sides of the board run at right angles to each other. This reduces the effects of feedthrough through the board..
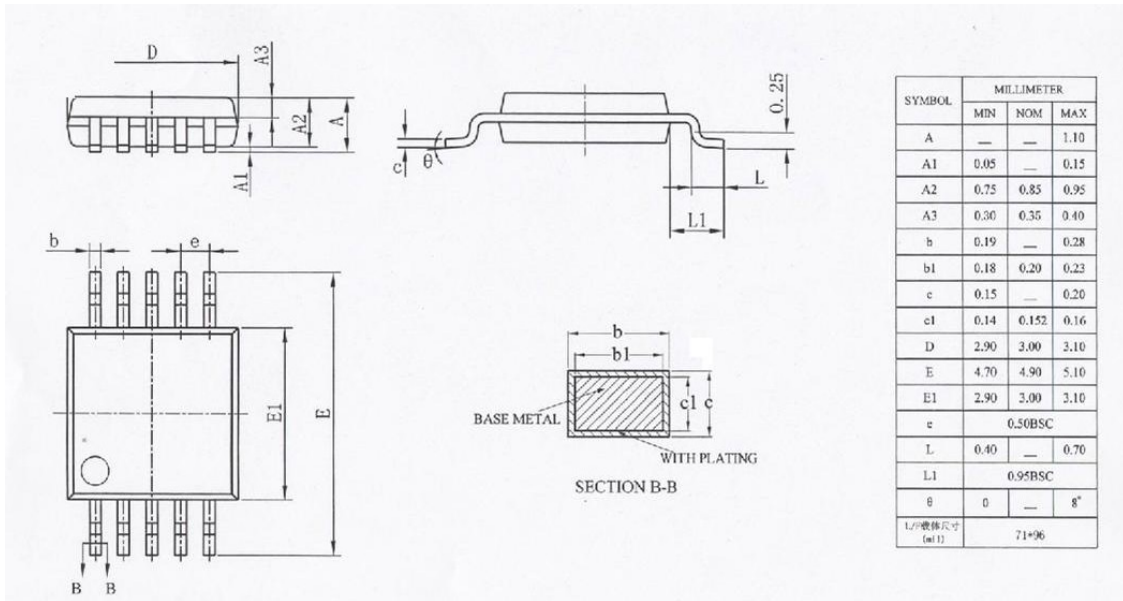
## 10. Outline Dimensions



Figure 11 MSOP10L Dimensions shown in millimeters

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.10 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| A3 | 0.30 | 0.35 | 0.40 |
| b | 0.19 | | 0.28 |
| b1 | 0.18 | 0.20 | 0.23 |
| c | 0.15 | | 0.20 |
| c1 | 0.14 | 0.152 | 0.16 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.70 | 4.90 | 5.10 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50BSC | | |
| L | 0.40 | — | 0.70 |
| L1 | 0.95BSC | | |
| θ | 0 | — | 8° |
| L/F整体尺寸 (mil) | 71*96 | | |

# 11.Ordering Guide

Table 7

| Model | Temperature Range(℃) | Package Description | Marking |
|---|---|---|---|
| KTA5314 | | MSOP10L | |
| KTA5324 | | MSOP10L | |

## 12. Revision History

Table 8

| Revision | Date | Author | Modification |
|----------|------|--------|--------------|
| V1.0 | 2013-06-01 | Liuxq | Initial |
| V2.0 | 2015-05-27 | Yinxm | Revise Fonts |
| | | | |