

Module Interface of KW PAN1200

Last Update : 2008-06-03

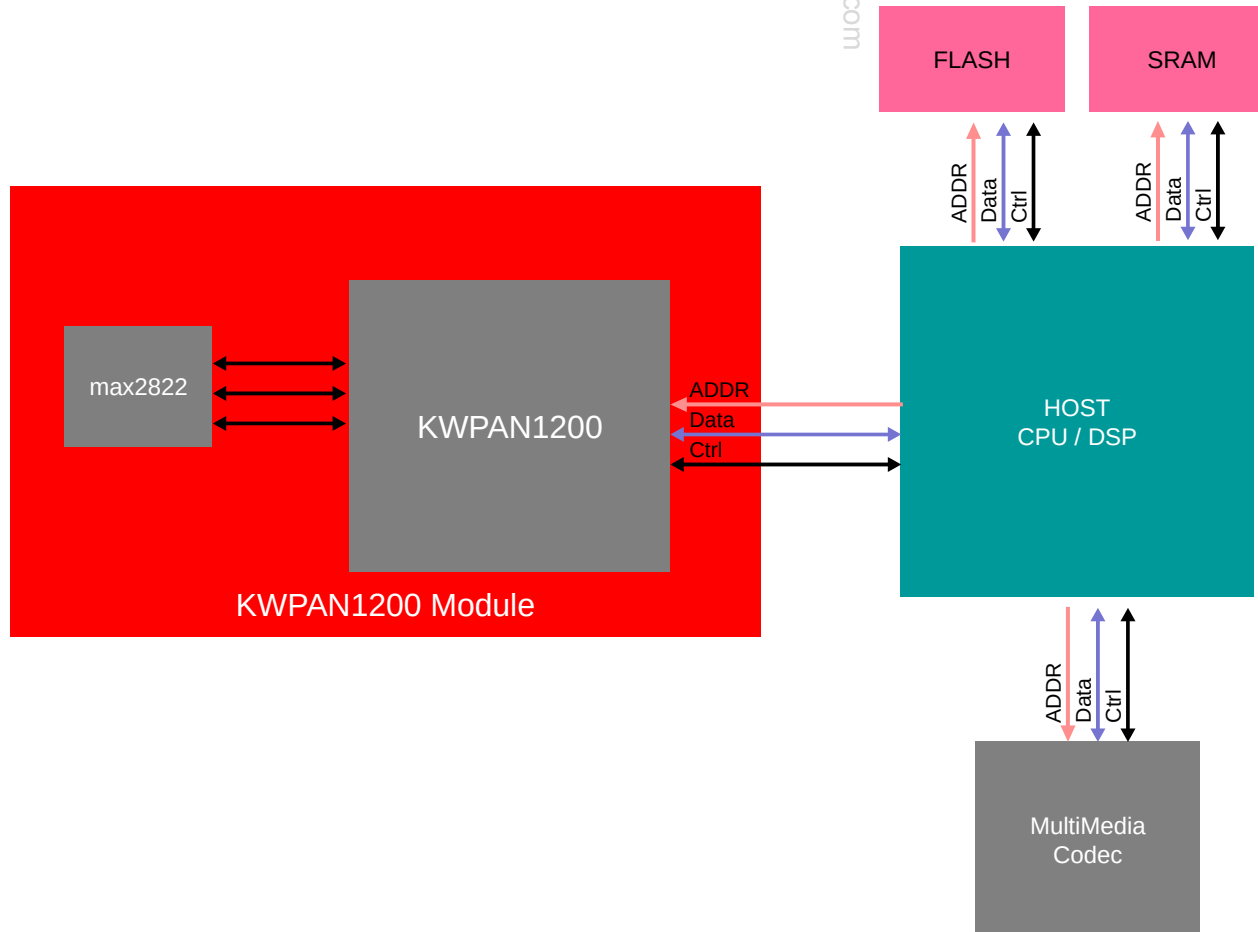


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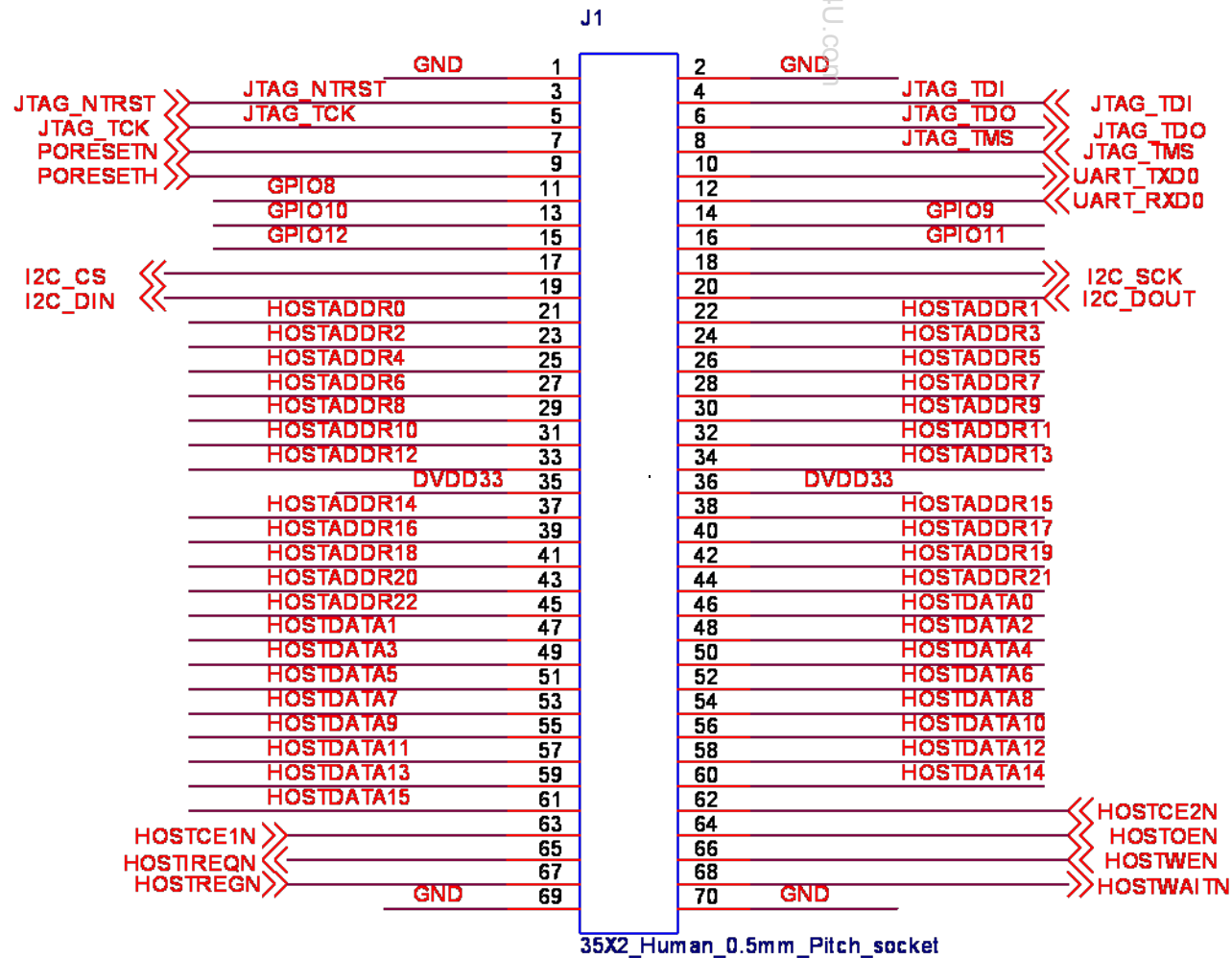
1. Application Block

KWPAN1200



2. Schematics

KWPAN1200



3. PIN Assignment

KWPAN1200

NO	NAME	NO	NAME	NO	NAME	NO	NAME
1,2	GND	19	I2C_DIN	36	DVDD33	53	HOSTDATA7
3	JTAG_NTRST	20	I2C_DOUT	37	HOSTADDR14	54	HOSTDATA8
4	JTAG_TDI	21	HOSTADDR0	38	HOSTADDR15	55	HOSTDATA9
5	JTAG_TCK	22	HOSTADDR1	39	HOSTADDR16	56	HOSTDATA10
6	JTAG_TDO	23	HOSTADDR2	40	HOSTADDR17	57	HOSTDATA11
7	PORESETN	24	HOSTADDR3	41	HOSTADDR18	58	HOSTDATA12
8	JTAG_TMS	25	HOSTADDR4	42	HOSTADDR19	59	HOSTDATA13
9	PORESETH	26	HOSTADDR5	43	HOSTADDR20	60	HOSTDATA14
10	UART_TXD0	27	HOSTADDR6	44	HOSTADDR21	61	HOSTDATA15
11	GPIO8	28	HOSTADDR7	45	HOSTADDR22	62	HOSTCE2N
12	UART_RXD0	29	HOSTADDR8	46	HOSTDATA0	63	HOSTCE1N
13	GPIO9	30	HOSTADDR9	47	HOSTDATA1	64	HSTOEN
14	GPIO10	31	HOSTADDR10	48	HOSTDATA2	65	HOSTIREQN
15	GPIO11	32	HOSTADDR11	49	HOSTDATA3	66	HOSTWEN
16	GPIO12	33	HOSTADDR12	50	HOSTDATA4	67	HOSTREGN
17	I2C_CS	34	HOSTADDR13	51	HOSTDATA5	68	HOSTWAITN
18	I2C_SCK	35	DVDD33	52	HOSTDATA6	69,70	GND

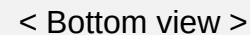
4. PIN Descriptions

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Name	No.	I/O	Description	Internal Resistor
HostAddr [0:22]	21,22,23,24,25,26,27,28,29, 30,31,32,33,34,37,38,39,40, 41,42,43,44,45	3SI O	23-bit input host address bus.	Input: pull-up Output: Tri-State
HostData [0:15]	46,47,48,49,50,51,52,53,54, 55,56,57,58,59,60,61	3SI	16-bit bidirectional data bus.	Input: pull-up Output: Tri-State
HostCE1n	62	SI	Chip Select 1, active-low	pull-up
HostCE2n	63	SI	Chip Select 2, active-low	pull-up
HostOEn	64	SI	Output Enable, active-low	pull-up
HostIREQn	65	O	IREQ signal, active-low	-
HostWEn	66	SI	Write Enable, active-low	pull-up
HostREGn	67	SI	Indicate Attribute Memory Access, active-low	pull-up
HostWAITn	68	O	Wait signal, active-low	-
GPIO [8:12]	11,13,14,15,16	3IO	General-purpose I/O	Input: pull-up Output: Tri-State
PORESETN	7	SI	System reset, active-low	pull-up
PORESETH	9	SI	System reset, active-high	pull-down
UART_TXD0	10	O	Transmitter output to External UART transceiver.	-
UART_RXD0	12	I	Transmitter Input to External UART transceiver.	-
I2C_CS	17	O	3-wire serial interface Clock (for MAC address)	-
I2C_SCK	18	O	3-wire serial interface Chip Select (for MAC address)	-
I2C_DIN	19	I	3-wire serial interface Data In (for MAC address)	-
I2C_DOUT	20	O	3-wire serial interface Data Out (for MAC address)	-
JTAG_NTRST	3	SI	Test mode Reset	pull-up
JTAG_TDI	4	SI	Test Data In	pull-up
JTAG_TCK	5	I	Test Clock	-
JTAG_TDO	6	O	Test Data Out	-
JTAG_TMS	8	SI	Test mode Select	pull-up
GND	1,2,69,70	G	Digital Ground	-
DVDD33	35,36	P	3.3V Digital Voltage Supply	-

*3SIO : Schmitt Trigger, SI:Schmitt trigger input, O:Output, 3IO: 3-state Bidirectional Input/Output

KWPN1200



Location	Function	ITEM	Vendor
Module	Antenna	RF-S200-117	커넥스전자
	HOST I/F	Human Plug 0.5-H2.5-70p	휴먼전자
MainBoard	Antenn	RF-S200-118	커넥스전자
	HOST I/F	Human Socket 0.5-H2.5-70p	휴먼전자