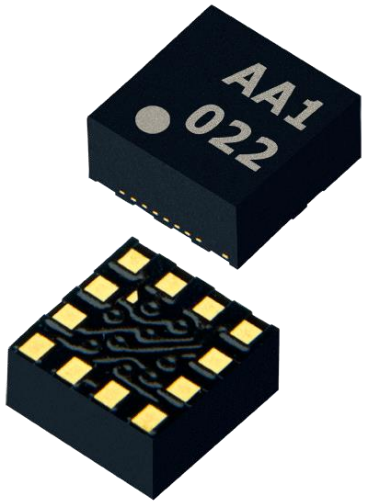
Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KX022-1020** **Rev. 4.0** **Jan-2014**

Product Description



The KX022 is a tri-axis +/-2g, +/-4g or +/-8g silicon micromachined accelerometer with integrated 256 byte buffer, orientation, tap/double tap, and activity detecting algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 2 x 2 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. I^2C or SPI digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional Tap™ detection and activity monitoring algorithms.

Features

- 2 x 2 x 0.9 mm LGA
- User-selectable g Range and Output Data Rate
- User-selectable 8-bit low resolution or 16-bit high resolution mode
- Digital High-Pass Filter Outputs
- Embedded FIFO/FILO buffer
- Low Power Consumption with FlexSet™ Performance Optimization
- Internal voltage regulator
- Enhanced integrated Directional Tap/Double-Tap™, and Device-orientation Algorithms
- User-configurable wake-up function
- Digital I^2C up to 3.4MHz
- Digital SPI up to 10MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

36 Thornwood Dr. – Ithaca, NY 14850
tel: 607-257-1080 – fax:607-257-1146
www.kionix.com - info@kionix.com

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36 Thornwood Dr. – Ithaca, NY 14850
tel: 607-257-1080 – fax:607-257-1146
www.kionix.com - info@kionix.com

36 Thornwood Dr. – Ithaca, NY 14850
tel: 607-257-1080 – fax:607-257-1146
www.kionix.com - info@kionix.com

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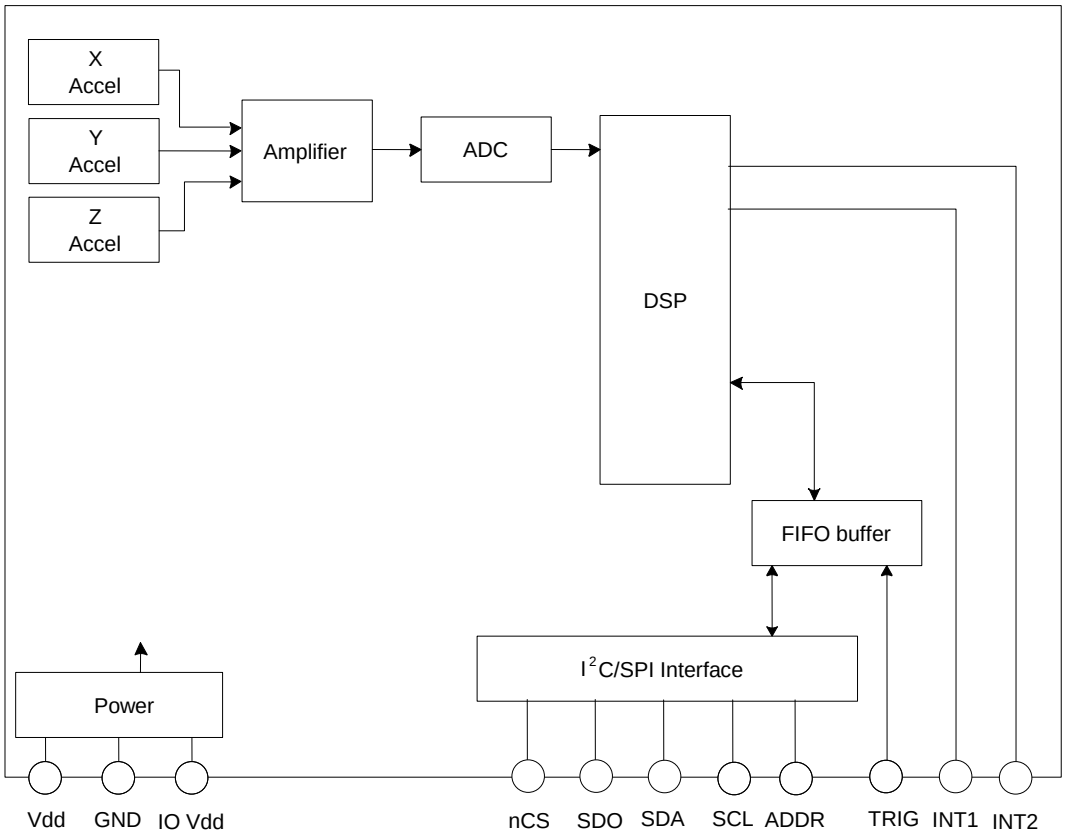
Functional Diagram



Product Specifications

Table 1. Mechanical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg		±25	±90
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.2	
Sensitivity[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	15401	16384	17367
	GSEL1=0, GSEL0=1 (± 4g)		7700	8192	8684
	GSEL1=1, GSEL0=0 (± 8g)		3850	4096	4342
Sensitivity (Buffer 8-bit mode)[1,2]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	60	64	68
	GSEL1=0, GSEL0=1 (± 4g)		30	32	34
	GSEL1=1, GSEL0=0 (± 8g)		15	16	17
Sensitivity Variation from RT over Temp.		%/ºC		0.01	
Self Test Output change on Activiation		g	0.35	0.5	0.65
Mechanical Resonance (-3dB)[3]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise (RMS at 50Hz with low-pass filter = ODR/9)[4]		mg		0.75	

Notes:

1. Resolution and acceleration ranges are user selectable via I^2C or SPI.
2. Sensitivity is proportional to BRES in BUF_CNTRL2.
3. Resonance as defined by the dampened mechanical sensor.
4. Noise varies with Output Data Rate (ODR) and Current Consumption settings. Contact Kionix Engineering for additional details on FlexSet™ Performance Optimization.

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tel: 607-257-1080 – fax:607-257-1146
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Table 2. Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	1.71	2.5	3.6
I/O Pads Supply Voltage (V_{IO})		V	1.7		V_{dd}
Current Consumption	High Power Mode (RES = 1)	µA		145	
	Low Power Mode[1] (RES = 0)			10	
	Standby			0.9	
Output Low Voltage (V_{io} < 2V)[2]		V	-	-	0.2 * V_{io}
Output Low Voltage (V_{io} > 2V)[2]		V	-	-	0.4
Output High Voltage		V	0.8 * V_{io}	-	-
Input Low Voltage		V	-	-	0.2 * V_{io}
Input High Voltage		V	0.8 * V_{io}	-	-
Input Pull-down Current		µA		0	
Start Up Time[3]		ms	2.0		650
Power Up Time[4]		ms		10	
I^2C Communication Rate		MHz			3.4
SPI Communication Rate		MHz			10
Output Data Rate (ODR)[5]		Hz	0.781	50	1600
Bandwidth (-3dB)[6]	RES = 0	Hz		800	
	RES = 1	Hz		ODR/2	

Notes:

1. Current varies with Output Data Rate (ODR) as shown the the chart below, and with Noise level settings. Contact Kionix Engineering for additional details on FlexSet™ Performance Optimization.
2. For I^2C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 set to valid outputs. Time varies with Output Data Rate (ODR); see chart below
4. Power up time is from Vdd valid to device boot completion.
5. User selectable through I^2C or SPI.
6. User selectable and dependent on ODR and RES.

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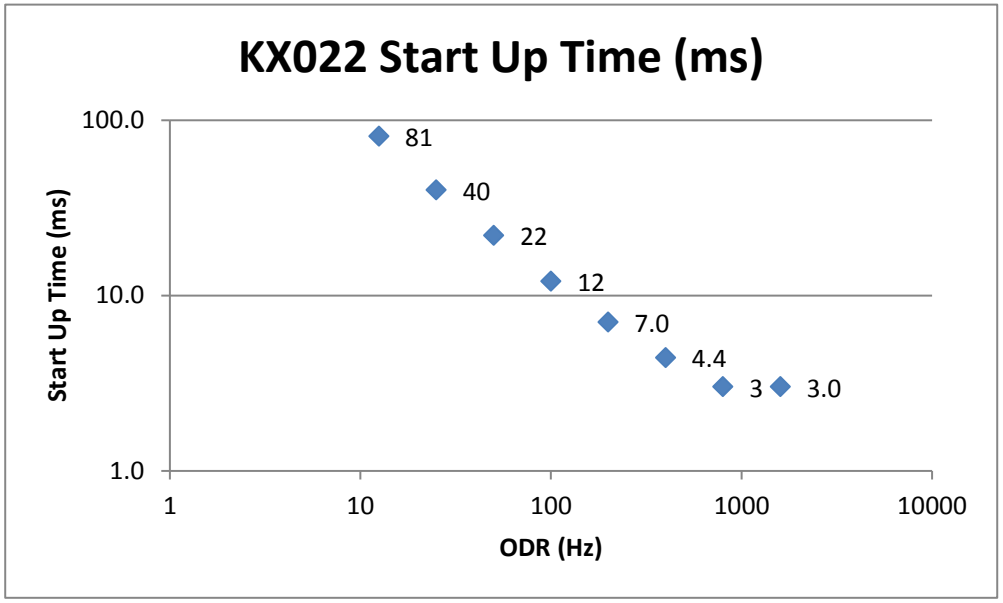
Start Up Time Profile

KX022 Start Up Time	
ODR (Hz)	Time (ms)
1600	3.0
800	3.0
400	4.4
200	7.0
100	12
50	22
25	40
12.5	81



Current Profile

KX022 Representative Current Profile		
ODR (Hz)	RES	Current (uA)
0	Standby	0.9
0.781	0	1.8
1.563	0	2.0
3.125	0	2.2
6.25	0	3.0
12.5	0	5
25	0	7
50	0	13
100	0	21
200	0	43
400	0	83
800	1	146
1600	1	146

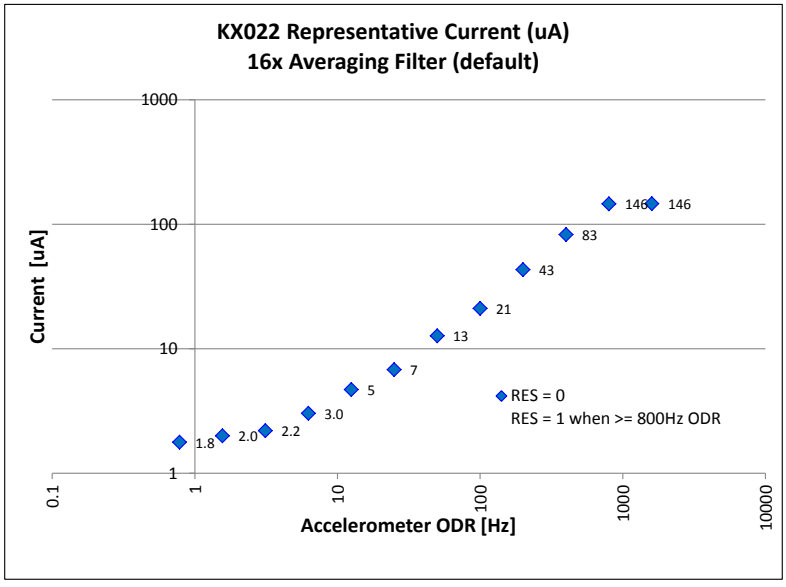


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Table 3 Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

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Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8\frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal V_{dd} and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output@+1g - Output@-1g)}{2g}$$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25ºC), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the OUTX, OUTY, OUTZ registers = 00h, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 00h. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I^2C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic. Plus, there are two programmable state machines which allow the user to create unique embedded functions based on changes in acceleration.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non volatile memory (OTP). Additionally, all functional register default values are also programmed into the non volatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

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Application Schematic

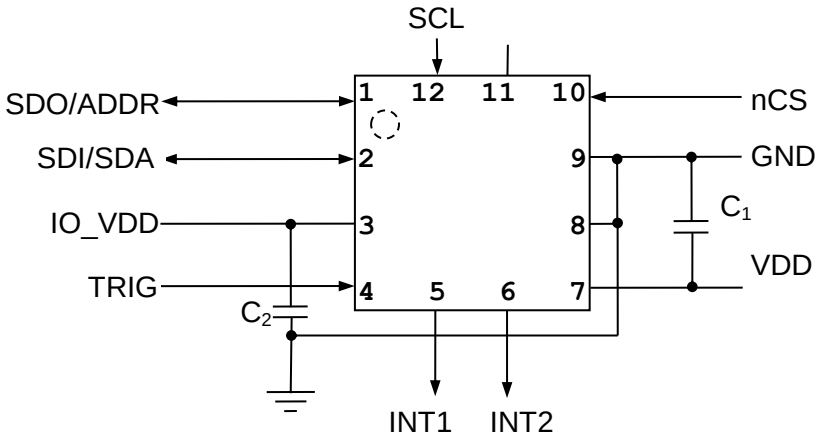

Table 4. KX022 Pin Descriptions

Pin	Name	Description
1	SDO/ADDR	Serial Data Out pin during 4 wire SPI communication and part of the device address during I2C communication.
2	SDI/SDA	SPI Data input / I2C Serial Data
3	IO Vdd	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
4	TRIG	Trigger pin for FIFO buffer control – Connect to GND when not using external trigger option
5	INT1	Physical Interrupt 1
6	INT2	Physical Interrupt 2
7	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
8	GND	Ground
9	GND	Ground
10	nCS	SPI enable / I2C mode select (0 = SPI enabled, I2C communication disabled / 1 = SPI disabled, I2C communication enabled)
11	NC	Not Internally Connected
12	SCLK/SCL	SPI and I^2C Serial Clock

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Test Specifications

***Special Characteristics**:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

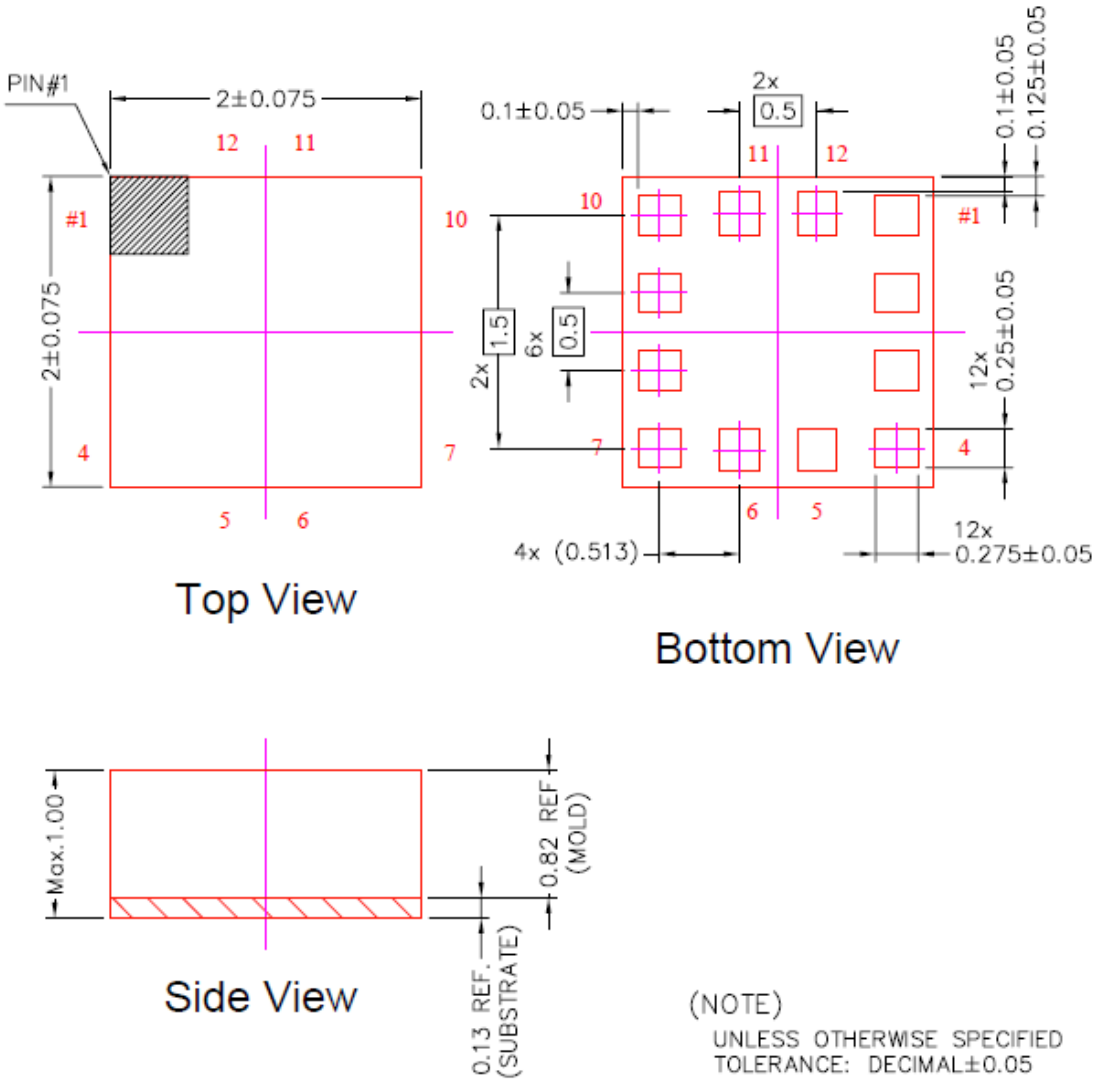
Table 5. Test Specifications

Parameter	Specification	Test Conditions
Zero-g Offset @ RT (2g range)	0 +/- 329 counts (<1% of FS)	25C, Vdd = 2.5 V
Sensitivity @ RT (2g range)	16384 +/- 656 counts/g (4%)	25C, Vdd = 2.5 V

Package Dimensions and Orientation

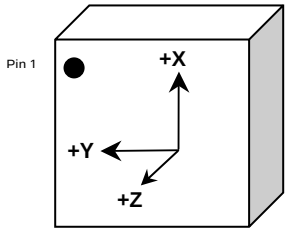
Dimensions

2 x 2 x 0.9 mm LGA



All dimensions and tolerances conform to ASME Y14.5M-1994

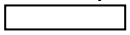
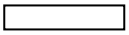
Orientation

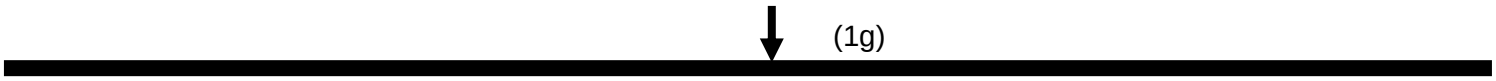


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 2g)

Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	16384	64	0	0	-16384	-64	0	0	0	0	0	0
Y (counts)	0	0	-16384	-64	0	0	16384	64	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	16384	64	-16384	-64
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



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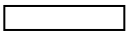
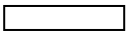
Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (± 4g)

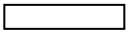
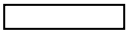
Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	8192	32	0	0	-8192	-32	0	0	0	0	0	0
Y (counts)	0	0	-8192	-32	0	0	8192	32	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	8192	32	-8192	-32
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 8g)

Position	1		2		3		4		5		6	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	4096	16	0	0	-4096	-16	0	0	0	0	0	0
Y (counts)	0	0	-4096	-16	0	0	4095	16	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	4096	16	-4096	-16
X-Polarity	**+**		**0**		**-**		**0**		**0**		**0**	
Y-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

 (1g)

Earth's Surface

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KX022 Digital Interface

The Kionix KX022 digital accelerometer has the ability to communicate via the I^2C and SPI digital serial interface protocols. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

I^2C Serial Interface

As previously mentioned, the KX022 has the ability to communicate on an I^2C bus. I^2C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX022 always operates as a Slave device during standard Master-Slave I^2C operation.

I^2C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I^2C bus is considered free when both lines are high.

The I2C interface is compliant with high-speed mode, fast mode and standard mode I2C protocols.

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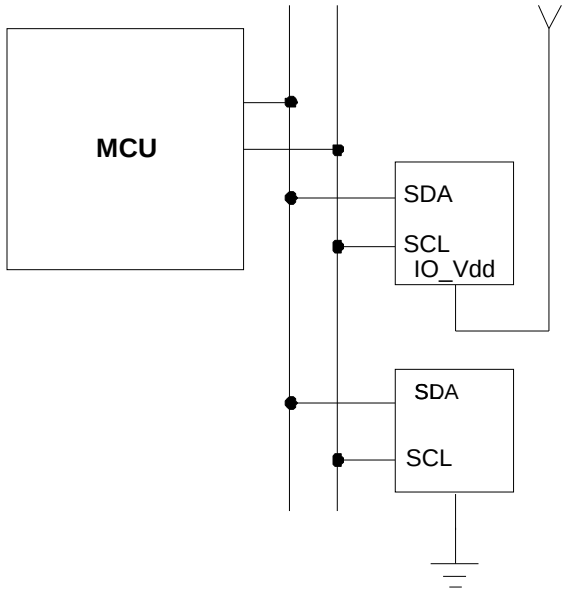

Figure 1. Multiple KX022 I²C Connection

I2C Address

Description	Address Pad	7 bit Address	Address	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
I2C Wr	VDD	1Fh	3Eh	0	0	1	1	1	1	1	0
I2C Rd	VDD	1Fh	3Fh	0	0	1	1	1	1	1	1
I2C Wr	VSS	1Eh	3Ch	0	0	1	1	1	1	0	0
I2C Rd	VSS	1Eh	3Dh	0	0	1	1	1	1	0	1

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The KX022's Slave Address is comprised of a programmable part and a fixed part, which allows for connection of multiple KX022's to the same I²C bus. The Slave Address associated with the KX022 is 001111X, where the programmable bit, X, is determined by the assignment of ADDR (pin 1) to GND or IO_Vdd. Figure 1 above shows how two KX022's would be implemented on an I²C bus.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free. Note that if the KX022 is accessed through I^2C protocol before the startup is finished a NACK signal is sent.

Writing to a KX022 8-bit Register

Upon power up, the Master must write to the KX022's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KX022 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KX022 to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KX022 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KX022 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KX022 is now stored in the appropriate register. The KX022 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page. When the auto-increment feature reaches register address 0x7F (Buffer Read), it stops and does not advance to register address 0x80. A new read command must be issued for registers above 0x7F. The part then continues to auto-increment until it reaches address 0xFF.

Reading from a KX022 8-bit Register

When reading data from a KX022 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KX022 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KX022 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KX022 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KX022 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 7 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5. HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode								FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P	
Slave						ACK		ACK		ACK		

n bytes + ack.

Sequence 6. HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

I²C Timing Diagram

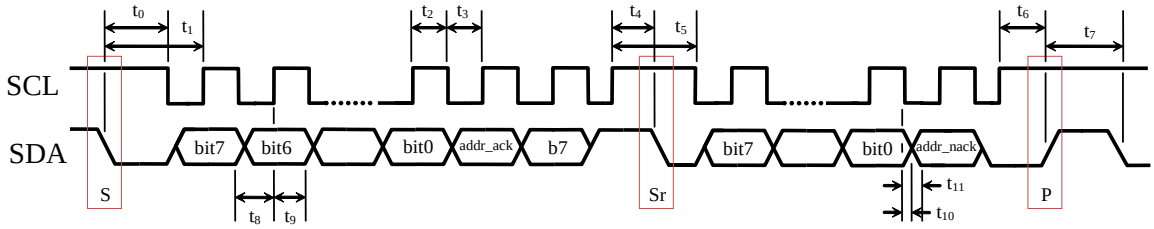

Table 8. I²C Timing (Fast Mode)

Number	Description	MIN	MAX	Units
t_0	SDA low to SCL low transition (Start event)	50	-	ns
t_1	SDA low to first SCL rising edge	100	-	ns
t_2	SCL pulse width: high	100	-	ns
t_3	SCL pulse width: low	100	-	ns
t_4	SCL high before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: high during a S/Sr/P event	100	-	ns
t_6	SCL high before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: high	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is transmitting)	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is transmitting)	0	-	ns
Note	Recommended I²C CLK	2.5	-	us

SPI Communications

4-Wire SPI Interface

The KX022 also utilizes an integrated 4-Wire Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KX022 always operates as a Slave device during standard Master-Slave SPI operation.

4-wire SPI is a synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDI or MOSI) and the Data Input (SDO or MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 2 below.

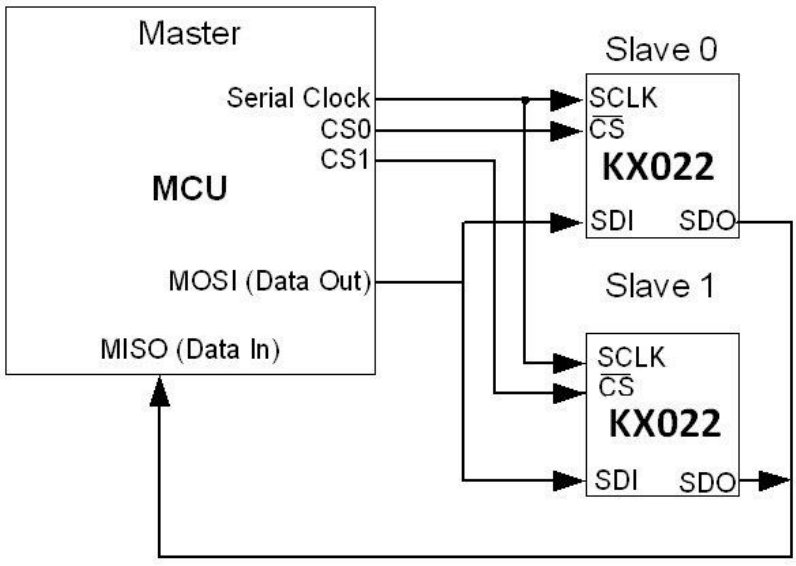

Figure 2 KX022 4-wire SPI Connections

4-Wire SPI Timing Diagram

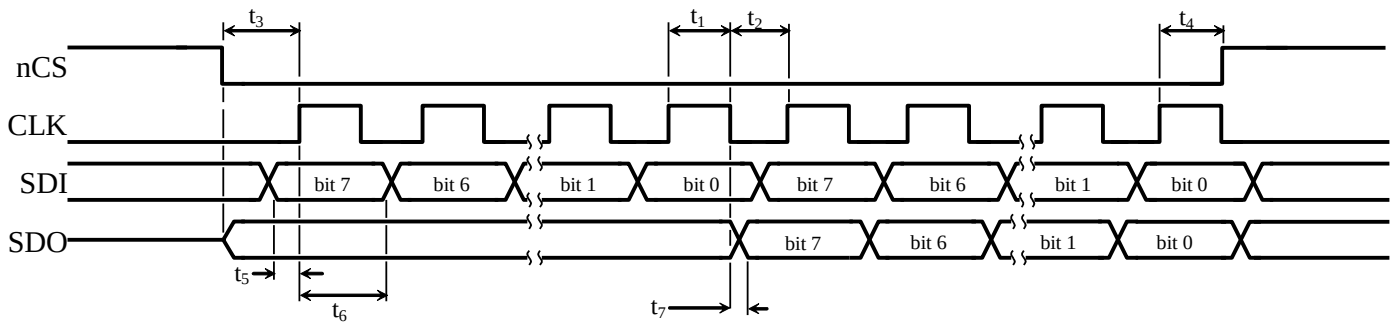

Table 9. 4-Wire SPI Timing

Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	40		ns
t_2	CLK pulse width: low	40		ns
t_3	nCS low to first CLK rising edge	20		ns
t_4	nCS low after the final CLK rising edge	30		ns
t_5	SDI valid to CLK rising edge	10		ns
t_6	CLK rising edge to SDI invalid	10		ns
t_7	CLK falling edge to SDO valid		35	ns

Notes

1. t_7 is only present during reads.
2. Timings are for Vdd of 1.8V to 3.6V with 1KΩ pull-up resistor and maximum 20pF load capacitor on SDO.

Read and Write Registers

The registers embedded in the KX022 have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. This operation occurs over 16 clock cycles. All commands are sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 3 below shows the timing diagram for carrying out an 8-bit register write operation.

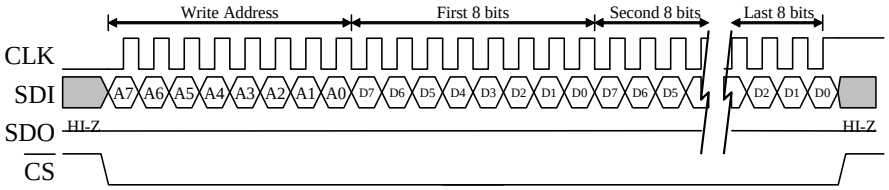

Figure 3 Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 4 shows the timing diagram for an 8-bit register read operation.

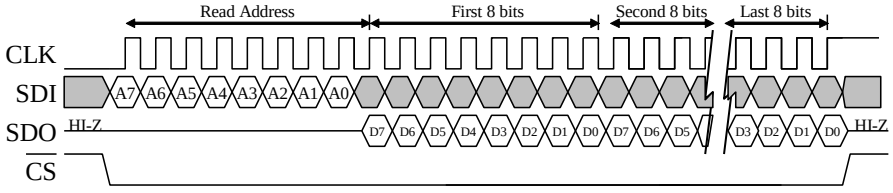

Figure 4 Timing Diagram for 8-Bit Register Read Operation

3-Wire SPI Interface

The KX022 also utilizes an integrated 3-Wire Serial Peripheral Interface (SPI) for digital communication. 3-wire SPI is a synchronous serial interface that uses two control lines and one data line. With respect to the Master, the Serial Clock output (SCLK), the Data Output/Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. This allows multiple Slave devices to share a master SPI port as shown in Figure 6 below.

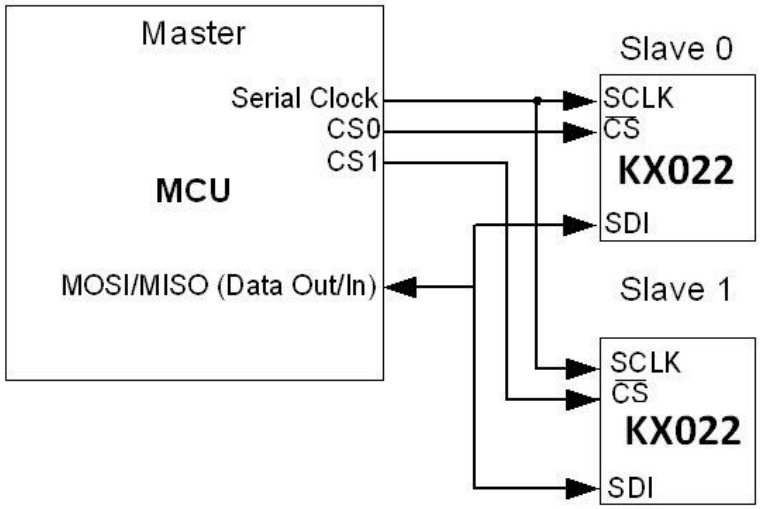

Figure 5 KX022 3-wire SPI Connections

3-Wire SPI Timing Diagram

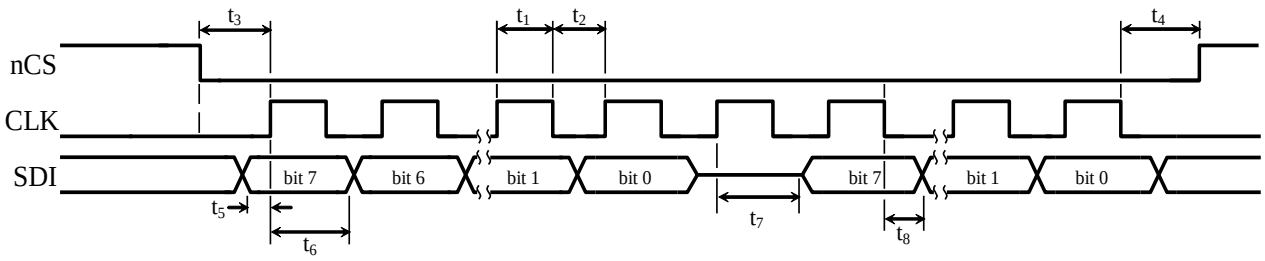

Table 10. 3-Wire SPI Timing

Number	Description	MIN	MAX	Units
t_1	CLK pulse width: high	40	-	ns
t_2	CLK pulse width: low	40	-	ns
t_3	nCS low to first CLK rising edge	20	-	ns
t_4	nCS low after the final CLK falling edge	20	-	ns
t_5	SDI valid to CLK rising edge	10	-	ns
t_6	CLK rising edge to SDI input invalid	10	-	ns
t_7	CLK extra clock cycle rising edge to SDI output	tbd	-	ns
t_8	CLK falling edge to SDI output becomes valid	-	35	ns

Notes

1. t_7 and t_8 are only present during reads.
2. Timings are for Vdd of 1.8V to 3.6V with 1KΩ pull-up resistor and maximum 20pF load capacitor on SDI.

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Read and Write Registers

The registers embedded in the KX022 have 8-bit addresses. Upon power up, the Master must write to the accelerometer's control registers to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the appropriate control register. The first byte initiates the write to the appropriate register, and is followed by the user-defined, data byte. The MSB (Most Significant Bit) of the register address byte will indicate "0" when writing to the register and "1" when reading from the register. A read operation occurs over 17 clock cycles and a write operation occurs over 16 clock cycles. All commands are sent MSB first, and the host must return nCS high for at least one clock cycle before the next address transmission. Figure 6 below shows the timing diagram for carrying out an 8-bit register write operation.

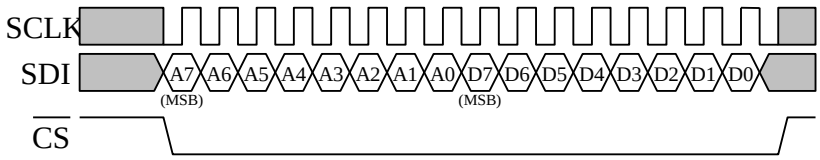

Figure 6 Timing Diagram for 8-Bit Register Write Operation

In order to read an 8-bit register, an 8-bit register address must be written to the accelerometer to initiate the read. The MSB of this register address byte will indicate "0" when writing to the register and "1" when reading from the register. Upon receiving the address, the accelerometer returns the 8-bit data stored in the addressed register. For 3-wire read operations, one extra clock cycle between the address byte and the data output byte is required. Therefore, this operation occurs over 17 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least one clock cycle before the next data request. Figure 7 shows the timing diagram for an 8-bit register read operation.

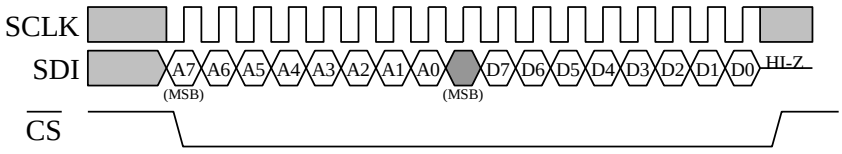

Figure 7 Timing Diagram for 8-Bit Register Read Operation

KX022 Embedded Registers

The KX022 has 57 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 11 below provides a listing of the accessible 8-bit registers and their addresses.

Address	Register Name	R/W
00h	XHPL	R
01h	XHPH	R
02h	YHPL	R
03h	YHPH	R
04h	ZHPL	R
05h	ZHPH	R
06h	XOUTL	R
07h	XOUTH	R
08h	YOUTL	R
09h	YOUTH	R
0Ah	ZOUTL	R
0Bh	ZOUTH	R
0Ch	COTR	R
0Dh	Kionix Reserved	
0Eh	Kionix Reserved	
0Fh	Who_AM_I	R/W
10h	TSCP	R
11h	TSPP	R
12h	INS1	R
13h	INS2	R
14h	INS3	R
15h	STAT	R
16h	Kionix Reserved	
17h	INT_REL	R
18h	CNTL1*	R/W
19h	CNTL2*	R/W
1Ah	CNTL3*	R/W
1Bh	ODCNTL*	R/W
1Ch	INC1*	R/W
1Dh	INC2*	R/W
1Eh	INC3*	R/W
1Fh	INC4*	R/W
20h	INC5*	R/W
21h	INC6*	R/W
22h	TILT_TIMER*	R/W
23h	WUFC*	R/W
24h	TDTRC*	R/W

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25h	TDTC*	R/W
26h	TTH*	R/W
27h	TTL*	R/W
28h	FTD*	R/W
29h	STD*	R/W
2Ah	TLT*	R/W
2Bh	TWS*	R/W
2Ch	Kionix Reserved	
2Dh	Kionix Reserved	
2Eh	Kionix Reserved	
2Fh	Kionix Reserved	
30h	ATH*	R/W
31h	Kionix Reserved	
32h	TILT_ANGLE_LL*	R/W
33h	TILT_ANGLE_HL*	R/W
34h	HYST_SET*	R/W
35h	LP_CNTL*	R/W
36h	Kionix Reserved	
37h	Kionix Reserved	
38h	Kionix Reserved	
39h	Kionix Reserved	
3Ah	BUF_CNTL1*	R/W
3Bh	BUF_CNTL2*	R/W
3Ch	BUF_STATUS_1	R
3Dh	BUF_STATUS_2	R
3Eh	BUF_CLEAR	W
3Fh	BUF_READ	R
60h	SELF_TEST	R/W

* Note: - When changing the contents of these registers, the PC1 bit in CTRL_REG1 must first be set to “0”.
- Reserved registers should not be written.

Table 11. KX022 Register Map

KX022 Register Descriptions

Accelerometer Outputs

These registers contain up to 16-bits of valid acceleration data for each axis. Depending on the setting of the RES bit in CTRL_REG1, the user may choose to read only the 8 MSB thus reading an effective 8-bit resolution . When BRES = 0 in BUF_CNTL2 the 8 MSB is the only data recorded in the buffer. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per 12 below. The register acceleration output binary data is represented in 2's complement format. For example, if N = 16 bits, then the Counts range is from -32768 to 32767, and if N = 8 bits, then the Counts range is from -128 to 127.

16-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111 1111	32767	+2.0000g	+3.9999g	+7.9998g
0111 1111 1111 1110	32766	+1.9999g	+3.9998g	+7.9995g
…	…	…	…	…
0000 0000 0001	1	+0.0006g	+0.0001g	+0.0002g
0000 0000 0000	0	0.000g	0.0000g	0.0000g
0011 1111 1111 1111	-1	-0.0006g	-0.0001g	-0.0002g
…	…	…	…	…
1000 0000 0000 0001	-8191	-1.9999g	-3.9999g	-7.9998g
1000 0000 0000 0000	-8192	-2.0000g	-4.0000g	-8.000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111	127	+1.984g	+3.968g	+7.936g
0111 1110	126	+1.968g	+3.936g	+7.872g
…	…	…	…	…
0000 0001	1	+0.016g	+0.032g	+0.064g
0000 0000	0	0.000g	0.000g	0.000g
1111 1111	-1	-0.016g	-0.032g	-0.064g
…	…	…	…	…
1000 0001	-127	-1.984g	-3.968g	-7.936g
1000 0000	-128	-2.000g	-4.000g	-8.000g

Table 12. Acceleration (g) Calculation

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XHP_L

X-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
XHPD7	XHPD6	XHPD5	XHPD4	XHPD3	XHPD2	XHPD1	XHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x00h		

XHP_H

X-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
XHPD15	XHPD14	XHPD13	XHPD12	XHPD11	XHPD10	XHPD9	XHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x01h		

YHP_L

Y-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
YHPD7	YHPD6	YHPD5	YHPD4	YHPD3	YHPD2	YHPD1	YHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x02h		

YHP_H

Y-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
YHPD15	YHPD14	YHPD13	YHPD12	YHPD11	YHPD10	YHPD9	YHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x03h		

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ZHP_L

Z-axis high pass filter accelerometer output least significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3

R	R	R	R	R	R	R	R
ZHPD7	ZHPD6	ZHPD5	ZHPD4	ZHPD3	ZHPD2	ZHPD1	ZHPD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x04h		

ZHP_H

Z-axis high pass filter accelerometer output most significant byte. Data is updated at the ODR frequency determined by OWUF in CNTL3.

R	R	R	R	R	R	R	R
ZHPD15	ZHPD14	ZHPD13	ZHPD12	ZHPD11	ZHPD10	ZHPD9	ZHPD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x05h		

XOUT_L

X-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
XOUTD7	XOUTD6	XOUTD5	XOUTD4	XOUTD3	XOUTD2	XOUTD1	XOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x06h		

XOUT_H

X-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
XOUTD15	XOUTD14	XOUTD13	XOUTD12	XOUTD11	XOUTD10	XOUTD9	XOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x07h		

YOUT_L

Y-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD7	YOUTD6	YOUTD5	YOUTD4	YOUTD3	YOUTD2	YOUTD1	YOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x08h		

YOUT_H

Y-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD15	YOUTD14	YOUTD13	YOUTD12	YOUTD11	YOUTD10	YOUTD9	YOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x09h		

ZOUT_L

Z-axis accelerometer output least significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4	ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Ah		

ZOUT_H

Z-axis accelerometer output most significant byte. Data is updated at the ODR frequency determined by OSA in ODCNTL.

R	R	R	R	R	R	R	R
YOUTD15	YOUTD14	YOUTD13	YOUTD12	YOUTD11	YOUTD10	YOUTD9	YOUTD8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Bh		

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COTR

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55h unless the COTC bit in CNTL2 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register and the COTC bit in CNTL2 is cleared.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
					I^2C Address: 0x0Ch			

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x14h.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010100
					I^2C Address: 0x0Fh			

Tilt Position Registers

These two registers report previous and current position data that is updated at the user-defined ODR frequency and is protected during register read. Table 13 describes the reported position for each bit value.

TSCP

Current Tilt Position Register.

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
					I^2C Address: 0x10h			

TSPP

Previous Tilt Positon Register.

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
					I^2C Address: 0x11h			

Bit	Description
LE	Left State (X-)
RI	Right State (X+)
DO	Down State (Y-)
UP	Up State (Y+)
FD	Face-Down State (Z-)
FU	Face-Up State (Z+)

Table 13. KX022 Tilt Position

Interrupt Source Registers

These three registers report interrupt state changes. This data is updated when a new interrupt event occurs and each application's result is latched until the interrupt release register is read. The programmable interrupt engine can be configured to report data in an unlatched manner via the interrupt control registers.

INS1

This register indicates the triggering axis when a tap/double tap interrupt occurs. Data is updated at the ODR settings determined by OTDT<2:0> in CNTL3.

R	R	R	R	R	R	R	R
0	0	TLE	TRI	TDO	TUP	TFD	TFU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x12h		

Bit	Description
TLE	X Negative (X-) Reported
TRI	X Positive (X+) Reported
TDO	Y Negative (Y-) Reported
TUP	Y Positive (Y+) Reported
TFD	Z Negative (Z-) Reported
TFU	Z Positive (Z+) Reported

Table 14. KX022 Directional Tap™ Reporting

INS2

This Register tells witch function caused an interrupt.

R	R	R	R	R	R	R	R
0	BFI	WMI	DRDY	TDTS1	TDTS0	WUFS	TPS
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x13h		

BFI *– indicates buffer full interrupt. Automatically cleared when buffer is read.*
BFI = 0 – Buffer is not full
BFI = 1 – Buffer is full

WMI *– Watermark interrupt, bit is set to one when FIFO has filled up to the value stored in the sample bits.This bit is automatically cleared when FIFO/FILO is read and the content returns to a value below the value stored in the sample bits.*
WMI = 0 – Buffer watermark has not been exceeded
WMI = 1 – Buffer watermark has been exceeded

DRDY *– indicates that new acceleration data (0x06h to 0x0Bh) is available. This bit is cleared when acceleration data is read or the interrupt release register INT_REL is read.*
DRDY = 0 - new acceleration data not available
DRDY = 1 - new acceleration data available

TDTS(1,0) *– status of tap/double tap, bit is released when interrupt release register INT_REL is read.*

TDTS1	TDTS0	Event
0	0	No Tap
0	1	Single Tap
1	0	Double Tap
1	1	Do not exist

WUFS *– Status of Wake up. This bit is cleared when the interrupt release register INT_REL is read.*
WUFS = 1 – Motion has activated the interrupt
WUFS = 0 – No motion

TPS *– Tilt Position status. This bit is cleared when the interrupt release register INT_REL is read.*
TPS = 0 – Position not changed
TPS = 1 – Position changed

INS3

This register reports the axis and direction of detected motion.

R	R	R	R	R	R	R	R
0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x14h		

Bit	Description
XNWU	X Negative (X-) Reported
XPWU	X Positive (X+) Reported
YNWU	Y Negative (Y-) Reported
YPWU	Y Positive (Y+) Reported
ZNWU	Z Negative (Z-) Reported
ZPWU	Z Positive (Z+) Reported

Table 15. KX022 Motion Detection™ Reporting

STATUS_REG

This register reports the status of the interrupt.

R	R	R	R	R	R	R	R
0	0	0	INT	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x15h		

INT *reports the combined (OR) interrupt information of all features. When BFI and WMI in INS2 are 0, the INT bit is released to 0 when INT_REL is read. If WMI or BFI is 1, INT bit remains at 1 until they are cleared by FIFO/FILO buffer read.*

0 = no interrupt event

1 = interrupt event has occurred

INT_REL

Latched interrupt source information (INS1,INS2, INS3 except WMI/BFI and INT when WMI/BFI is zero) is cleared and physical interrupt latched pin is changed to it's inactive state when this register is read. Read value is dummy.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x17h		

CNTL1

Read/write control register that controls the main feature set.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PC1	RES	DRDYE	GSEL1	GSEL0	TDTE	WUFE	TPE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x18h			

PC1 *controls the operating mode of the KX022. When in RES = 0, please allow 1.2/ODR delay time when transistioning from stand-by PC1 = 0 to operating mode PC1 = 1 to allow new settings to load.*

0 = stand-by mode

1 = operating mode

RES *determines the performance mode of the KX022. The noise varies with ODR, RES and different LP_CNTL settings possibly reducing the effective resolution. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

0 = low current.

1 = high current. Bandwidth (Hz) = ODR/2

DRDYE *enables the reporting of the availability of new acceleration data as an interrupt. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

0 = availability of new acceleration data is not reflected as an interrupt

1 = availability of new acceleration data is reflected as an interrupt

GSEL1, GSEL0 *selects the acceleration range of the accelerometer outputs per Table 16. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

GSEL1	GSEL0	Range
0	0	+/-2g
0	1	+/-4g
1	0	+/-8g

Table 16. Selected Acceleration Range

TDTE *enables the Directional Tap™ function that will detect single and double tap events. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
TDTE = 0 – disable
TDTE = 1 - enable

WUFE *enables the Wake Up (motion detect) function. 0= disabled, 1= enabled. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
0 = Wake Up function disabled
1 = Wake Up function enabled

TPE *enables the Tilt Position function that will detect changes in device orientation. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
TPE = 0 – disable
TPE = 1 - enable

CNTL2

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SRST	COTC	LEM	RIM	DOM	UPM	FDM	FUM	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I²C Address: 0x19h			

SRST *initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished.*
SRST = 0 – no action
SRST = 1 – start RAM reboot routine

COTC *Command test control.*

DCST = 0 – no action
DCST = 1 – sets STR register to 0xAAh and when STR is read, sets this bit to 0 and sets STR to 0x55h

TLEM, TRIM, TDOM, TUPM, TFDM *these bits control the tilt axis mask.* Per Table 17, if a direction's bit is set to one (1), tilt in that direction will generate an interrupt. If it is set to zero (0), tilt in that direction will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

Bit	Description
TLEM	X Negative (X-)
TRIM	X Positive (X+)
TDOM	Y Negative (Y-)
TUPM	Y Positive (Y+)
TFDM	Z Negative (Z-)
TFUM	Z Positive (Z+)

Table 17. Tilt Direction™ Axis Mask

CNTL3

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
OTP1	OTP0	OTDT2	OTDT1	OTDT0	OWUF2	OWUF1	OWUF0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10011000
					I^2C Address: 0x1Ah			

OTPA, OTPB *sets the output data rate for the Tilt Position function per Table 18. The default Tilt Position ODR is 12.5Hz.*

OTP1	OTP0	Output Data Rate
0	0	1.563Hz
0	1	6.25Hz
1	0	12.5Hz
1	1	50Hz

Table 18. Tilt Position Function Output Data Rate

OTDTA, OTDTB *sets the output data rate for the Directional Tap™ function per Table 19. The default Directional Tap™ ODR is 400Hz.*

OTDT2	OTDT1	OTDT0	Output Data Rate
0	0	0	50Hz
0	0	1	100Hz
0	1	0	200Hz
0	1	1	400Hz
1	0	0	12.5Hz
1	0	1	25Hz
1	1	0	800Hz
1	1	1	1600Hz

Table 19. Directional Tap™ Function Output Data Rate

OWUF2, OWUF1, OWUF0 *sets the output data rate for the general motion detection function and the high-pass filtered outputs per Table 20. The default Motion Wake Up ODR is 0.781Hz.*

OWUF2	OWUF1	OWUF0	Output Data Rate
0	0	0	0.781Hz
0	0	1	1.563Hz
0	1	0	3.125Hz
0	1	1	6.250Hz
1	0	0	12.5Hz
1	0	1	25Hz
1	1	0	50Hz
1	1	1	100Hz

Table 20. Motion Wake Up Function Output Data Rate

36 Thornwood Dr. – Ithaca, NY 14850
tel: 607-257-1080 – fax:607-257-1146
www.kionix.com - info@kionix.com

ODCNTL

This register is responsible for configuring ODR (output data rate) and filter settings.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
IIR_BYPASS	LPRO	RESERVED	RESERVED	OSA3	OSA2	OSA1	OSA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000010
					I^2C Address: 0x1Bh			

IIR_BYPASS *filter bypass mode*

IIR_BYPASS = 0 – filtering applied
IIR_BYPASS = 1 – filter bypassed

LPRO *low-pass filter roll off control*

LPRO = 0 – filter corner frequency set to ODR/9
LPRO = 1 – filter corner frequency set to ODR/2

OSA3, OSA2, OSA1, OSA0 *acceleration output data rate. The default ODR is 50Hz.*

OSA3	OSA2	OSA1	OSA0	Output Data Rate
0	0	0	0	12.5Hz*
0	0	0	1	25Hz*
0	0	1	0	50Hz*
0	0	1	1	100Hz*
0	1	0	0	200Hz*
0	1	0	1	400Hz*
0	1	1	0	800Hz
0	1	1	1	1600Hz
1	0	0	0	0.781Hz*
1	0	0	1	1.563Hz*
1	0	1	0	3.125Hz*
1	0	1	1	6.25Hz*

Table 21. Accelerometer Output Data Rates (ODR)

* Low power mode available, all other data rates will default to full power mode

INC1

This register controls the settings for the physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	IEN1	IEA1	IEL1	Reserved	STPOL	SPI3E	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
					I^2C Address: 0x1Ch			

IEN *enables/disables the physical interrupt pin*
IEN = 0 – physical interrupt pin is disabled
IEN = 1 – physical interrupt pin is enabled

IEA *sets the polarity of the physical interrupt pin*
IEA = 0 – polarity of the physical interrupt pin is active low
IEA = 1 – polarity of the physical interrupt pin is active high

IEL *sets the response of the physical interrupt pin*
IEL = 0 – the physical interrupt pin latches until it is cleared by reading INT_REL
IEL = 1 – the physical interrupt pin will transmit one pulse with a period of 50 us

STPOL *sets the polarity of Self Test*
STPOL = 0 – Negative
STPOL = 1 – Positive

SPI3E *sets the 3-wire SPI interface*
SPI3E = 0 – disabled
SPI3E = 1 – enabled

INC2

This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I^2C Address: 0x1Dh			

XNWU *– x negative (x-): 0 = disabled, 1 = enabled*
XPWU *– x positive (x+): 0 = disabled, 1 = enabled*
YNWU *– y negative (y-): 0 = disabled, 1 = enabled*

YPWU *– y positive (y+): 0 = disabled, 1 = enabled*
ZNWU *– z negative (z-): 0 = disabled, 1 = enabled*
ZPWU *– z positive (z+): 0 = disabled, 1 = enabled*

INC3

This register controls which axis and direction of tap/double tap can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	TLEM	TRIM	TDOM	TUPM	TFDM	TFUM	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I^2C Address: 0x1Eh			

TLEM *– x negative (x-): 0 = disabled, 1 = enabled*
TRIM *– x positive (x+): 0 = disabled, 1 = enabled*
TDOM *– y negative (y-): 0 = disabled, 1 = enabled*
TUPM *– y positive (y+): 0 = disabled, 1 = enabled*
TFDM *– z negative (z-): 0 = disabled, 1 = enabled*
TFUM *– z positive (z+): 0 = disabled, 1 = enabled*

INC4

This register controls routing of an interrupt reporting to physical interrupt piin INT1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	BFI1	WMI1	DRDYI1	Reserved	TDTI1	WUFI1	TPI1	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x1Fh			

BFI1 *– Buffer full interrupt reported on physical interrupt pin INT1*
WMI1 *- Watermark interrupt reported on physical interrupt pin INT1*
DRDYI1 *– Data ready interrupt reported on physical interrupt pin INT1*
TDTI1 *- Tap/Double Tap interrupt reported on physical interrupt pin INT1*
WUFI1 *– Wake-Up (motion detect) interrupt reported on physical interrupt pin INT1*
TPI1 *– Tilt position interrupt reported on physical interrupt pin INT1*

INC5

This register controls the settings for the physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	Reserved	IEN2	IEA2	IEL2	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
					I^2C Address: 0x20h			

IEN2 *enables/disables the physical interrupt pin*
IEN2 = 0 – physical interrupt pin is disabled
IEN2 = 1 – physical interrupt pin is enabled

IEA2 *sets the polarity of the physical interrupt pin*
IEA2 = 0 – polarity of the physical interrupt pin is active low
IEA2 = 1 – polarity of the physical interrupt pin is active high

IEL2 *sets the response of the physical interrupt pin*
IEL2 = 0 – the physical interrupt pin latches until it is cleared by reading INT_REL
IEL2 = 1 – the physical interrupt pin will transmit one pulse with a period of 50 us

INC6

This register controls routing of interrupt reporting to physical interrupt pin INT2.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	BFI2	WMI2	DRDYI2	Reserved	TDTI2	WUFI2	TPI2	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x21h			

BFI2 *– Buffer full interrupt reported on physical interrupt pin INT2*
WMI2 *- Watermark interrupt reported on physical interrupt pin INT2*
DRDYI2 *– Data ready interrupt reported on physical interrupt pin INT2*
TDTI2 *- Tap/Double Tap interrupt reported on physical interrupt pin INT2*
WUFI2 *– Wake-Up (motion detect) interrupt reported on physical interrupt pin INT2*
TPI2 *– Tilt position interrupt reported on physical interrupt pin INT2*

TILT_TIMER

This register is the initial count register for the tilt position state timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 18. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TSC7	TSC6	TSC5	TSC4	TSC3	TSC2	TSC1	TSC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x22h			

WUFC

This register is the initial count register for the motion detection timer (0 to 255 counts). Every count is calculated as 1/ODR delay period, where the ODR is user-defined per Table 20. A new state must be valid as many measurement periods before the change is accepted. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WUFC7	WUFC6	WUFC5	WUFC4	WUFC3	WUFC2	WUFC1	WUFC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x23h			

TDTRC

This register is responsible for enableing/disabling reporting of Tap/Double Tap. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	DTRE	STRE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000011
					I^2C Address: 0x24h			

DTRE *enables/disables the double tap interrupt*

DTRE = 0 – do not update/trigger interrupts on doubple tap events

DTRE = 1 –update interrupts on double tap events

STRE *enables/disables single tap interrupt*

STRE = 0 – do not update/trigger interrupts on single tap events

STRE = 1 –update interrupts on single tap events

TDTC

This register contains counter information for the detection of a double tap event. When the Directional TapTM ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional TapTM ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional TapTM ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional TapTM ODR is user-defined per Table 19. TDTC represents the minimum time separation between the first tap and the second tap in a double tap event. The Kionix recommended default value is 0.3 seconds (0x78h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TDTC7	TDTC6	TDTC5	TDTC4	TDTC3	TDTC2	TDTC1	TDTC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01111000
					I^2C Address: 0x25h			

TTH

This register represents the 8-bit jerk high threshold to determine if a tap is detected. Though this is an 8-bit register, the the register value is internally multiplied by two in order to set the high threshold. This multiplication results in a range of 0d to 510d with a resolution of two counts. The Performance Index (PI) is the jerk signal that is expected to be less than this threshold, but greater than the TTL threshold during single and double tap events. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0". The Kionix recommended default value is 203 (0xCBh) and the Performance Index is calculated as:

$$X' = X(\text{current}) - X(\text{previous})$$
$$Y' = Y(\text{current}) - Y(\text{previous})$$
$$Z' = Z(\text{current}) - Z(\text{previous})$$

$$PI = |X'| + |Y'| + |Z'|$$

Equation 1. Performance Index

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TTH7	TTH6	TTH5	TTH4	TTH3	TTH2	TTH1	TTH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	11001011
					I^2C Address: 0x26h			

TTL

This register represents the 8-bit (0d– 255d) jerk low threshold to determine if a tap is detected. The Performance Index (PI) is the jerk signal that is expected to be greater than this threshold and less than the TTH threshold during single and double tap events. The Kionix recommended default value is 26 (0x1Ah). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TTL7	TTL6	TTL5	TTL4	TTL3	TTL2	TTL1	TTL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00011010
					I^2C Address: 0x27h			

FTD

This register contains counter information for the detection of any tap event. When the Directional TapTM ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional TapTM ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional TapTM ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional TapTM ODR is user-defined per Table 19. In order to ensure that only tap events are detected, these time limits are used. A tap event must be above the performance index threshold for at least the low limit (FTDL0 – FTDL2) and no more than the high limit (FTDH0 – FTDH4). The Kionix recommended default value for the high limit is 0.05 seconds and for the low limit is 0.005 seconds (0xA2h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
FTDH4	FTDH3	FTDH2	FTDH1	FTDH0	FTDL2	FTDL1	FTDL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10100010
					I^2C Address: 0x28h			

STD

This register contains counter information for the detection of a double tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the two taps in a double tap event can be above the PI threshold (TTL). The Kionix recommended default value for STD is 0.09 seconds (0x24h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
STD7	STD6	STD5	STD4	STD3	STD2	STD1	STD0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100100
					I²C Address: 0x29h			

TLT

This register contains counter information for the detection of a tap event. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. In order to ensure that only tap events are detected, this time limit is used. This register sets the total amount of time that the tap algorithm will count samples that are above the PI threshold (TTL) during a potential tap event. It is used during both single and double tap events. However, reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of the TWS. The Kionix recommended default value for TLT is 0.1 seconds (0x28h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TLT7	TLT6	TLT5	TLT4	TLT3	TLT2	TLT1	TLT0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00101000
					I²C Address: 0x2Ah			

TWS

This register contains counter information for the detection of single and double taps. When the Directional Tap™ ODR is 400Hz or less, every count is calculated as 1/ODR delay period. When the Directional Tap™ ODR is 800Hz, every count is calculated as 2/ODR delay period. When the Directional Tap™ ODR is 1600Hz, every count is calculated as 4/ODR delay period. The Directional Tap™ ODR is user-defined per Table 19. It defines the time window for the entire tap event, single or double, to occur. Reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of this tap window. The Kionix recommended default value for TWS is 0.4 seconds (0xA0h). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TWS7	TWS6	TWS5	TWS4	TWS3	TWS2	TWS1	TWS0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	10100000
					I²C Address: 0x2Bh			

ATH

This register sets the threshold for wake-up (motion detect) interrupt is set. The KX022 will ship from the factory with this value set to correspond to a change in acceleration of 0.5g. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ATH7	ATH6	ATH5	ATH4	ATH3	ATH2	ATH1	ATH0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001000
					I^2C Address: 0x30h			

TILT_ANGLE_LL

This register sets the low level threshold for tilt angle detection. The KX022 ships from the factory with tilt angle set to a low threshold of 26° from horizontal. A different default tilt angle can be requested from the factory. Note that the minimum suggested tilt angle is 10°. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00001100
					I^2C Address: 0x32h			

TILT_ANGLE_HL

This register sets the high level threshold for tilt angle detection.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
HL7	HL6	HL5	HL4	HL3	HL2	HL1	HL0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00101010
					I^2C Address: 0x33h			

HYST_SET

This register sets the Hysteresis that is placed in between the Screen Rotation states. The KX022 ships from the factory with HYST_SET set to +/-15° of hysteresis. A different default hysteresis can be requested from the factory. Note that when writing a new value to this register the current values of RES0 and RES1 must be preserved. These values are set at the factory and must not change. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
RES1	RES0	HYST5	HYST4	HYST3	HYST2	HYST1	HYST0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010100
					I^2C Address: 0x34h			

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LP_CNTL

Low Power Control sets the number of samples of accelerometer output to be averaged. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reserved	AVC2	AVC1	AVC0	Reserved	Reserved	Reserved	Reserved	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01001011
					I^2C Address: 0x35h			

AVC<2:0> *– Averaging Filter Control, the default seting is 16 samples averaged*

000 = No Averaging
001 = 2 Samples Averaged
010 = 4 Samples Averaged
011 = 8 Samples Averaged
100 = 16 Samples Averaged (default)
101 = 32 Samples Averaged
110 = 64 Samples Averaged
111 = 128 Samples Averaged

BUF_CNTL1

Read/write control register that controls the buffer sample threshold.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
-	SMP6	SMP5	SMP4	SMP3	SMP2	SMP1	SMP0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x3Ah			

***SMP_TH[6:0] Sample Threshold**; determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BUF_RES=1, the maximum number of samples is 41; when BUF_RES=0, the maximum number of samples is 84.*

Buffer Model	Sample Function
Bypass	None
FIFO	Specifies how many buffer sample are needed to trigger a watermark interrupt.
Stream	Specifies how many buffer samples are needed to trigger a watermark interrupt.
Trigger	Specifies how many buffer samples before the trigger event are retained in the buffer.
FILO	Specifies how many buffer samples are needed to trigger a watermark interrupt.

Table 22. Sample Threshold Operation by Buffer Mode

BUF_CNTL2

Read/write control register that controls sample buffer operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
BFE	BRES	BFIE	0	0	0	BM1	BM0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x3Bh			

BUFE *controls activation of the sample buffer.*
BUFE = 0 – sample buffer inactive
BUFE = 1 – sample buffer active

BRES *determines the resolution of the acceleration data samples collected by the sample buffer.*
BUF_RES = 0 – 8-bit samples are accumulated in the buffer
BUF_RES = 1 – 16-bit samples are accumulated in the buffer

BFIE *buffer full interrupt enable bit*
BFIE = 0 – buffer full interrupt disabled
BFIE = 1 – buffer full interrupt updated in INS2

BUF_M1, BUF_M0 *selects the operating mode of the sample buffer per Table 23.*

BUF_M1	BUF_M0	Mode	Description
0	0	FIFO	The buffer collects 84 sets of 8-bit low resolution values or 41 sets of 16-bit high resolution values and then stops collecting data, collecting new data only when the buffer is not full.
0	1	Stream	The buffer holds the last 84 sets of 8-bit low resolution values or 41 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data.
1	0	Trigger	When a trigger event occurs, the buffer holds the last data set of SMP[6:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.
1	1	FILO	The buffer holds the last 84 sets of 8-bit low resolution values or 41 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data. Reading from the buffer in this mode will return the most recent data first.

Table 23. Selected Buffer Mode

BUF_STATUS_1

This register reports the status of the sample buffer.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMP_LEV7	SMP_LEV6	SMP_LEV5	SMP_LEV4	SMP_LEV3	SMP_LEV2	SMP_LEV1	SMP_LEV0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x3Ch		

***SMP_LEV[7:0] Sample Level**; reports the number of data bytes that have been stored in the sample buffer. When BUF_RES=1, this count will increase by 6 for each 3-axis sample in the buffer; when BUF_RES=0, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.*

BUF_STATUS_2

This register reports the status of the sample buffer trigger function.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BUF_TRIG	0	0	0	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x3Dh		

***BUF_TRIG** reports the status of the buffer's trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.*

BUF_CLEAR

Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x3Eh		

BUF_READ

Buffer output register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x3Fh		

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SELF_TEST

When 0xCA is written to this register, the MEMS self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Writing 0x00 to this register will return the accelerometer to normal operation.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	0	0	1	0	1	0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x60h			

KX022 Embedded Applications

Orientation Detection Feature

The orientation detection feature of the KX022 will report changes in face up, face down, +/- vertical and +/- horizontal orientation. This intelligent embedded algorithm considers very important factors that provide accurate orientation detection from low cost tri-axis accelerometers. Factors such as: hysteresis, device orientation angle and delay time are described below as these techniques are utilized inside the KX022

Hysteresis

A 45° tilt angle threshold seems like a good choice because it is halfway between 0° and 90°. However, a problem arises when the user holds the device near 45°. Slight vibrations, noise and inherent sensor error will cause the acceleration to go above and below the threshold rapidly and randomly, so the screen will quickly flip back and forth between the 0° and the 90° orientations. This problem is avoided in the KX022 by choosing a 30° threshold angle. With a 30° threshold, the screen will not rotate from 0° to 90° until the device is tilted to 60° (30° from 90°). To rotate back to 0°, the user must tilt back to 30°, thus avoiding the screen flipping problem. This example essentially applies +/- 15° of hysteresis in between the four screen rotation states. Table 24 shows the acceleration limits implemented for ϕ_T =30°.

Orientation	X Acceleration (g)	Y Acceleration (g)
0°/360°	$-0.5 < a_x < 0.5$	$a_y > 0.866$
90°	$a_x > 0.866$	$-0.5 < a_y < 0.5$
180°	$-0.5 < a_x < 0.5$	$a_y < -0.866$
270°	$a_x < -0.866$	$-0.5 < a_y < 0.5$

Table 24. Acceleration at the four orientations with +/- 15° of hysteresis

The KX022 allows the user to change the amount of hysteresis in between the four screen rotation states. By simply writing to the HYST_SET register, the user can adjust the amount of hysteresis up to

+/- 45°. The plot in Figure 2 shows the typical amount of hysteresis applied for a given digital count value of HYST_SET.

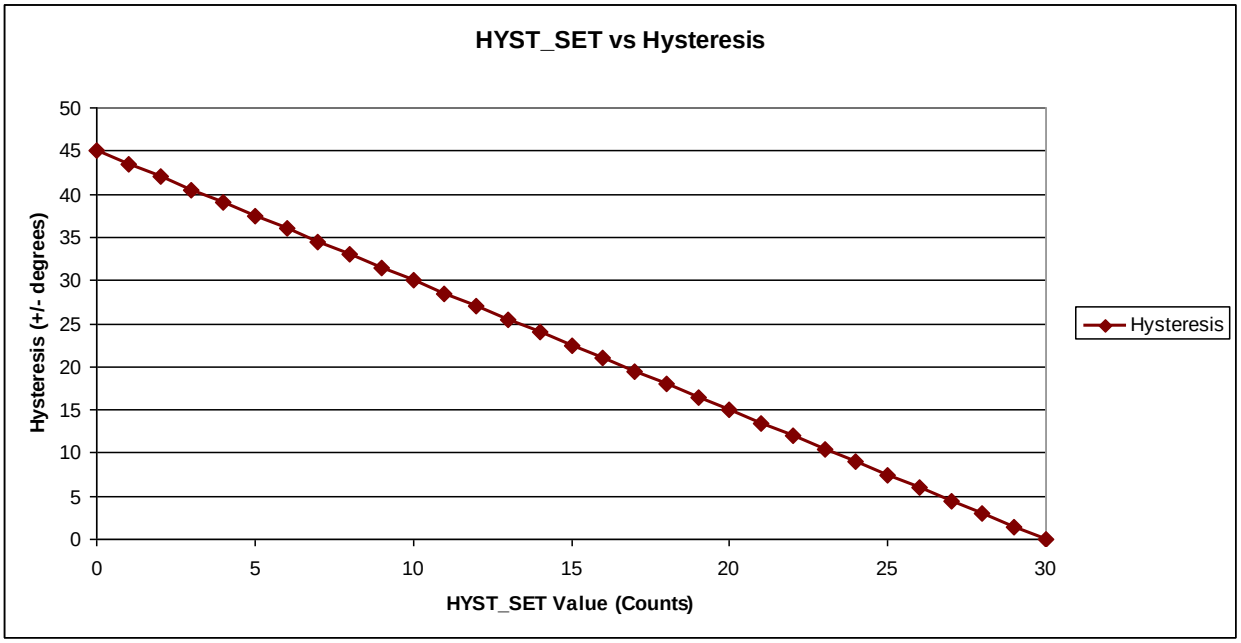

Figure 8. HYST_SET vs Hysteresis

Device Orientation Angle (aka Tilt Angle)

To ensure that horizontal and vertical device orientation changes are detected, even when it isn't in the ideal vertical orientation – where the angle θ in Figure 9 is 90°, the KX022 considers device orientation angle in its algorithm.

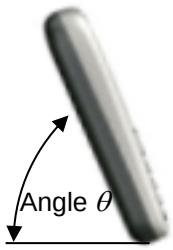

Figure 9. Device Orientation Angle

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As the angle in Figure 9 is decreased, the maximum gravitational acceleration on the X-axis or Y-axis will also decrease. Therefore, when the angle becomes small enough, the user will not be able to make the screen orientation change. When the device orientation angle approaches 0° (device is flat on a desk or table), $a_x = a_y = 0g$, $a_z = +1g$, and there is no way to determine which way the screen should be oriented, the internal algorithm determines that the device is in either the face-up or face-down orientation, depending on the sign of the z-axis. The KX022 will only change the screen orientation when the orientation angle is above the factory-defaulted/user-defined threshold set in the TILT_ANGLE_LL register. Equation 2 can be used to determine what value to write to the TILT_ANGLE_LL register to set the device orientation angle.

$$\text{TILT\_ANGLE\_LL (counts)} = \sin\theta * (32\ (\text{counts/g}))$$

Equation 2. Tilt Angle Threshold

Tilt Timer

The 8-bit register, TILT_TIMER can be used to qualify changes in orientation. The KX022 does this by incrementing a counter with a size that is specified by the value in TILT_TIMER for each set of acceleration samples to verify that a change to a new orientation state is maintained. A user defined output data rate (ODR) determines the time period for each sample. Equation 3 shows how to calculate the TILT_TIMER register value for a desired delay time.

$$\text{TILT\_TIMER (counts)} = \text{Delay Time (sec)} \times \text{ODR (Hz)}$$

Equation 3. Tilt Position Delay Time

Motion Interrupt Feature Description

The Motion interrupt feature of the KX022 reports qualified changes in the high-pass filtered acceleration based on the Wake Up (ATH) threshold. If the high-pass filtered acceleration on any axis is greater than the user-defined wake up threshold (ATH), the device has transitioned from an inactive state to an active state. When configured in the unlatched mode, the KX022 will report when the motion event finished and the device has returned to an inactive state. Equation 4 shows how to calculate the ATH register value for a desired wake up threshold. Note that this calculation varies based on the configured g-range of the part.

$$\text{ATH (counts)} = \text{Wake Up Threshold (g)} \times \text{Sensitivity (counts/g)}$$

Equation 4. Wake Up Threshold

An 8-bit raw unsigned value represents a counter that permits the user to qualify each active/inactive state change. Note that each WUFC Timer count qualifies 1 (one) user-defined ODR period (OWUF). Equation 5 shows how to calculate the WUFC register value for a desired wake up delay time.

WUFC (counts) = Wake Up Delay Time (sec) x OWUF (Hz)

Equation 5. Wake Up Delay Time

Figure 10 below shows the latched response of the motion detection algorithm with WUF Timer (WUFC) = 10 counts.

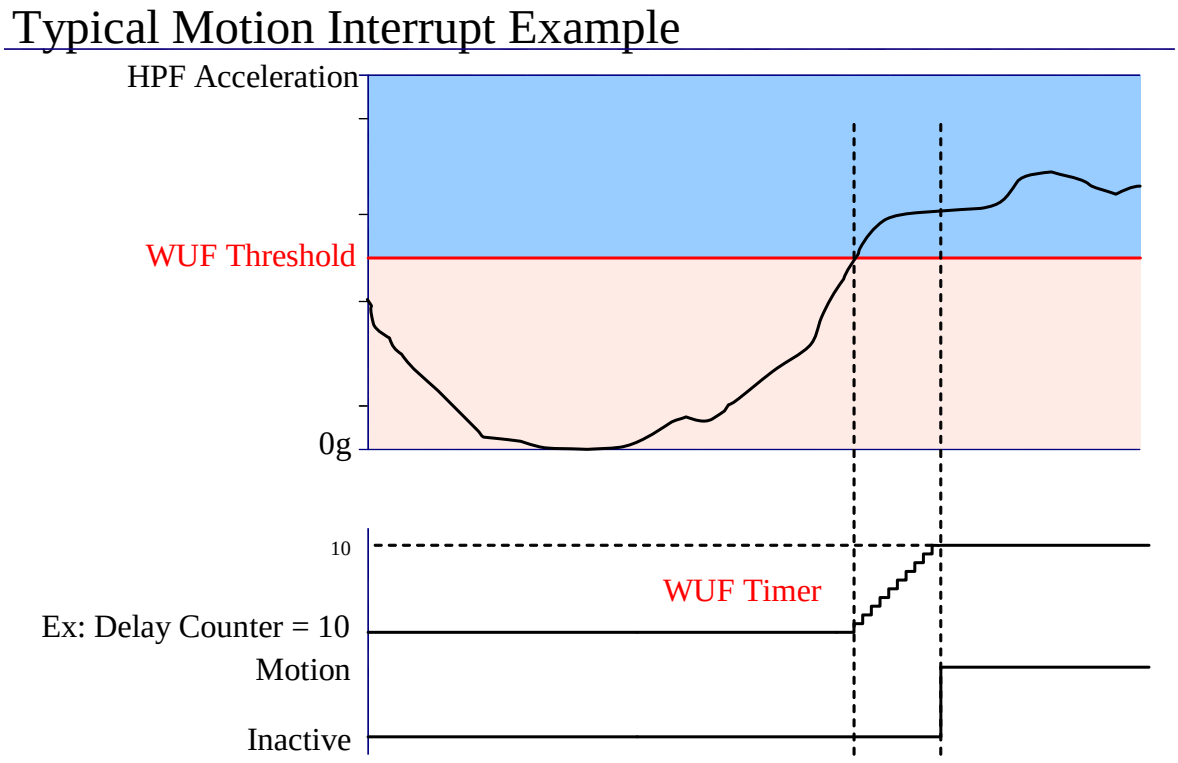

Figure 10. Latched Motion Interrupt Response

Figure 11 below shows the unlatched response of the motion detection algorithm with WUF Timer (WUFC) = 10 counts.

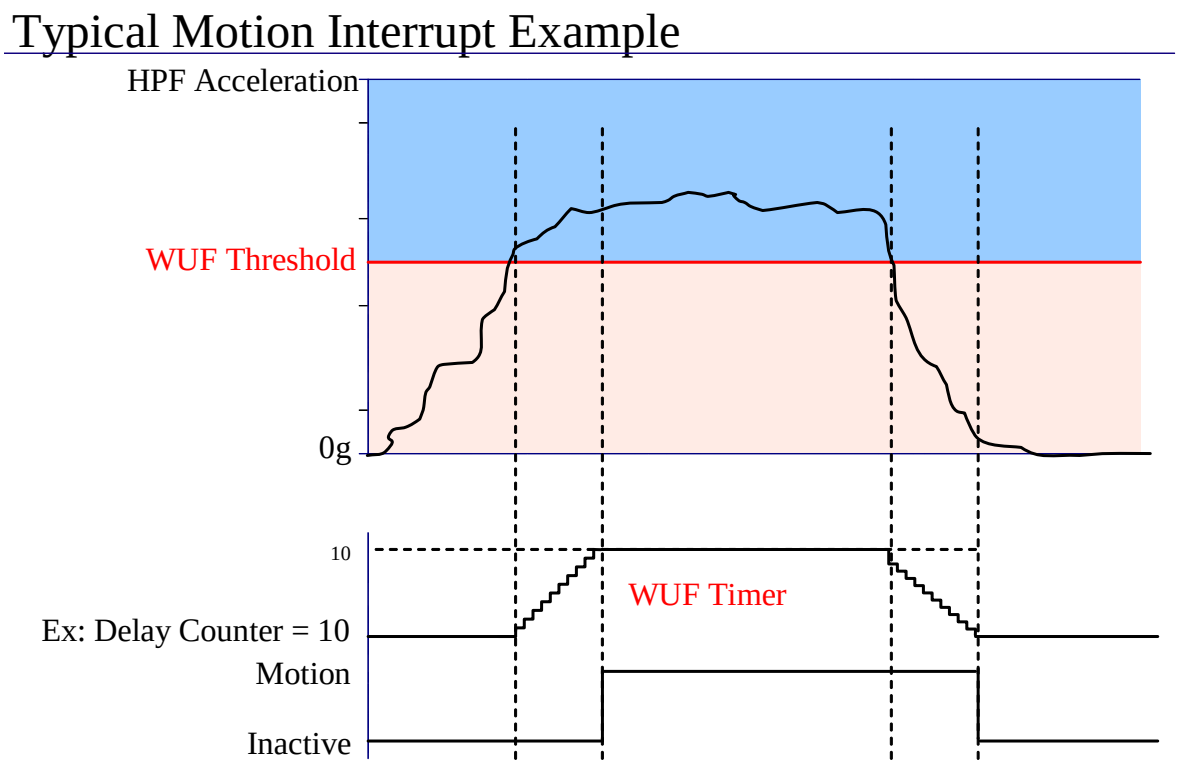

Figure 11. Unlatched Motion Interrupt Response

Directional Tap Detection Feature Description

The Directional Tap Detection feature of the KX022 recognizes single and double tap inputs and reports the acceleration axis and direction that each tap occurred. Eight performance parameters, as well as a user-selectable ODR are used to configure the KX022 for a desired tap detection response.

Performance Index

The Directional Tap™ detection algorithm uses low and high thresholds to help determine when a tap event has occurred. A tap event is detected when the previously described jerk summation exceeds the low threshold (TTL) for more than the tap detection low limit, but less than the tap detection high limit as contained in FTD. Samples that exceed the high limit (TTH) will be ignored. Figure 12 shows an example of a single tap event meeting the performance index criteria.

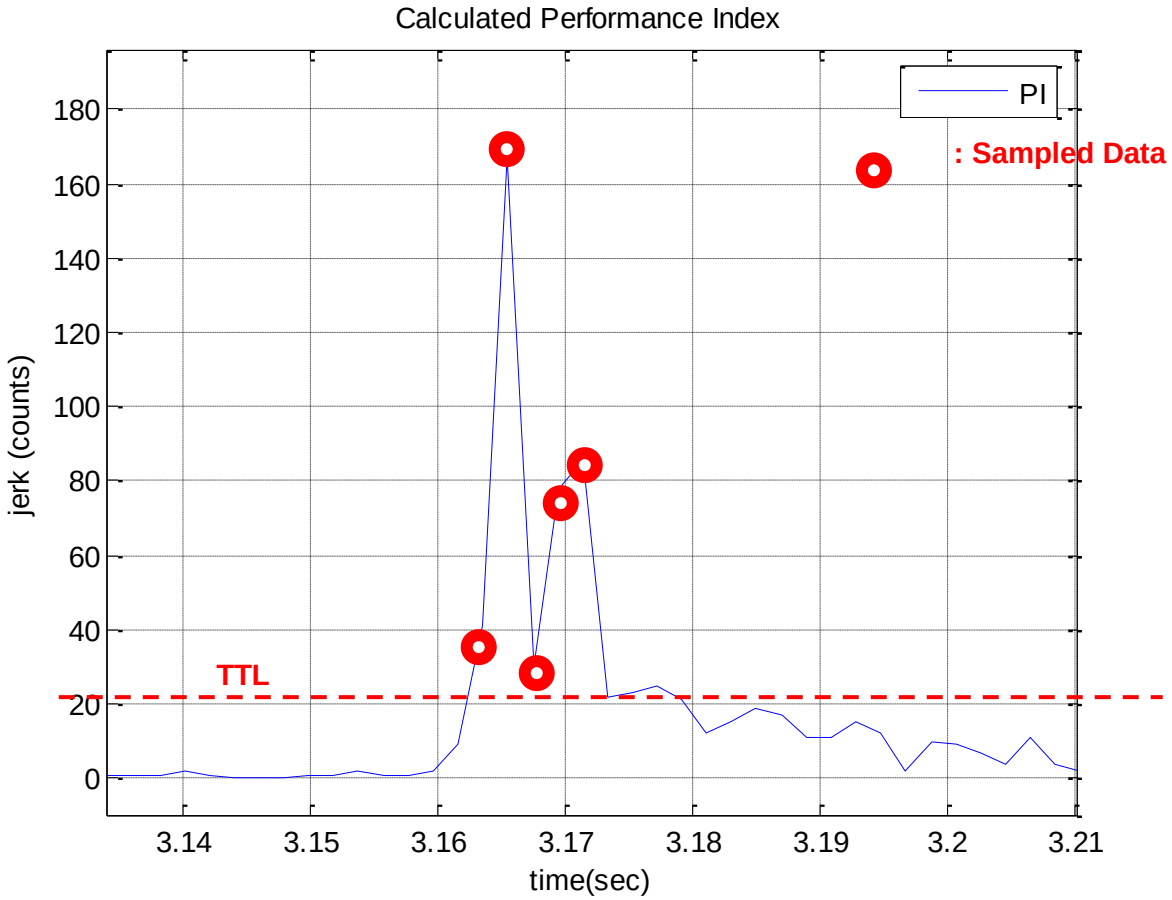

Figure 12. Jerk Summation vs Threshold

Single Tap Detection

The latency timer (TLT) sets the time period that a tap event will only be characterized as a single tap. A second tap has to occur outside of the latency timer. If a second tap occurs inside the latency time, it will be ignored as it occurred too quickly. The single tap will be reported at the end of the TWS. Figure 13 shows a single tap event meeting the PI, latency and window requirements.

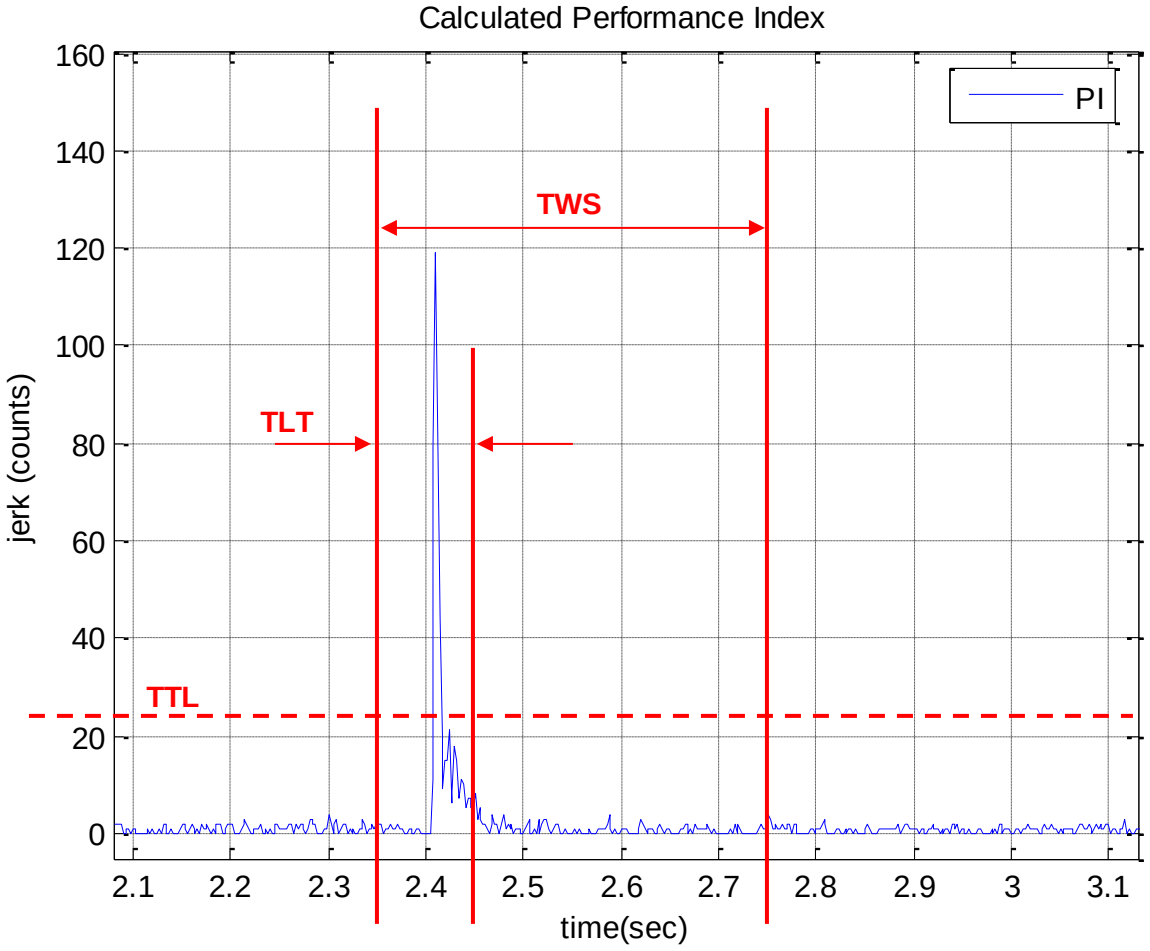

Figure 13. Single Directional Tap™ Timing

Double Tap Detection

An event can be characterized as a double tap only if the second tap crosses the performance index (TTL) outside the TDTC. This means that the TDTC determines the minimum time separation that must exist between the two taps of a double tap event. Similar to the single tap, the second tap event must exceed the performance index for the time limit contained in FTD. The double tap will be reported at the end of the second TLT. Figure 14 shows a double tap event meeting the PI, latency and window requirements.

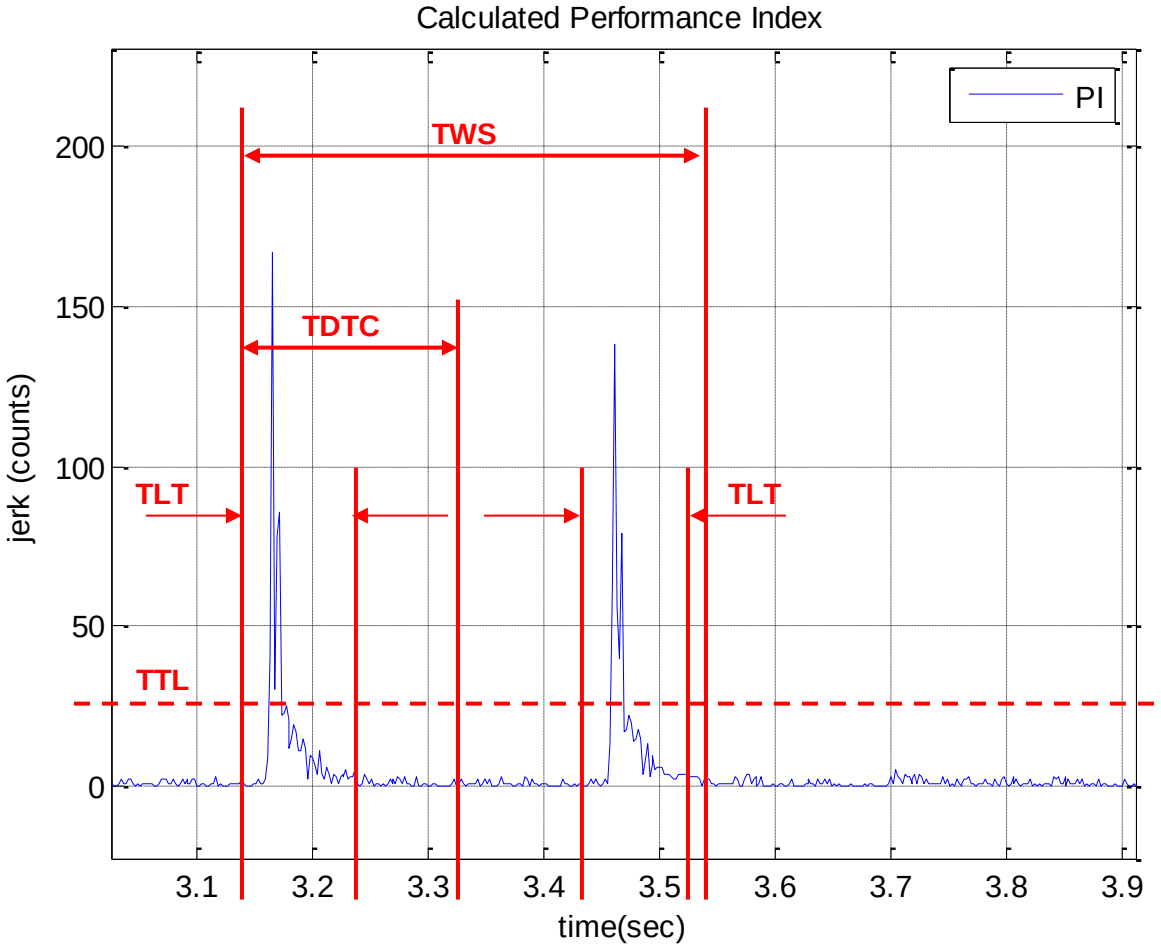

Figure 14. Double Directional Tap™ Timing

Sample Buffer Feature Description

The sample buffer feature of the KX022 accumulates and outputs acceleration data based on how it is configured. There are 4 buffer modes available, and samples can be accumulated at either low (8-bit) or high (16-bit) resolution. Acceleration data is collected at the ODR specified by OSAA:OSAD in the Output Data Control Register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 6).

BUF_RES=0:
SMPX = SMP_LEV[7:0] / 3 – SMP_TH[6:0]

BUF_RES=1:
SMPX = SMP_LEV[7:0] / 6 – SMP_TH[6:0]

Equation 6. Samples Above Sample Threshold

Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished

through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

Trigger Mode

Data Accumulation

When a physical interrupt is caused by one of the digital engines, the trigger event is asserted and SMP[6:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs and there are at least SMP[6:0] samples in the buffer, BUF_TRIG in BUF_STATUS_REG2 is asserted.

FILO Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the newest byte of the newest sample first (Z_H or Z based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 15 represents a high-resolution 3-axis sample within the buffer. Figures 16-24 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8.

Regardless of the selected mode, the buffer fills sequentially, one byte at a time. Figure 15 shows one 6-byte data sample. Note the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Byte	
	0	X_L	←-- FIFO read pointer
	1	X_H	
	2	Y_L	
	3	Y_H	
	4	Z_L	
	5	Z_H	←-- FILO read pointer
buffer write pointer --→	6		

Figure 15. One Buffer Sample

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 16 the location of the FILO read pointer versus that of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	← FILO read pointer
buffer write pointer →	3		
	4		
	5		
	6		
	7		← Sample Threshold
	8		
	9		

Figure 16. Buffer Filling

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The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 17 the location of the FILO read pointer versus that of the FIFO read pointer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	← FILO read pointer
buffer write pointer →	7		← Sample Threshold
	8		
	9		

Figure 17. Buffer Approaching Sample Threshold

In FIFO, Stream, and FILO modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold/FILO read pointer
buffer write pointer →	8		
	9		

Figure 18. Buffer at Sample Threshold

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In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 19 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	← Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer →	7	Data8	← Sample Threshold
	8		
	9		

Figure 19. Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 20. This results in the buffer holding SMP_TH[6:0] samples prior to the trigger event, and SMPX samples after the trigger event.

Index	Sample	
0	Data1	← Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	

Figure 20. Additional Data After Trigger Event

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In FIFO, Stream, FILO, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream and FILO modes begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	← FILO read pointer

Figure 21. Buffer Full

After the buffer has been filled in FILO or Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 22 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	← FILO read pointer

Figure 22. Buffer Full – Additional Sample Accumulation in Stream or FILO Mode

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 23.

	Index	Sample	
	0	Data1	← FIFO read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
	7	Data8	← Sample Threshold
	8	Data9	← FILO read pointer
buffer write pointer →	9		

Figure 23. FIFO Read from Full Buffer

In FILO mode, reading one sample from the buffer will remove the newest sample and leave the older samples untouched, as seen in Figure 24.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold
	8	Data8	← FILO read pointer
buffer write pointer →	9		

Figure 24. FILO Read from Full Buffer

36 Thornwood Dr. – Ithaca, NY 14850
tel: 607-257-1080 – fax:607-257-1146
www.kionix.com - info@kionix.com

Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KX022-1020** **Rev. 4.0** **Jan-2014**

Revision History

REVISION	DESCRIPTION	DATE
1.0	Initial Release	12-Sept-2013
1.1	Added LP_CNTL Accelerometer Output Averaging Register, Updated Test Spec limits Table 5 and I2C timing Table 8	02-Oct-2013
2.0	Added reference to FlexSet™ Performance Optimization, Updated reference to OSA in ODCNTL for XOUT_L register.	19-Nov-2013
3.0	Updated default values for TSPP, TSCP, ODCNTL	03-Dec-2013
4.0	Added Min and Max Self Test limits to Table 1, improved high/low power mode descriptions.	08-Jan-2014

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