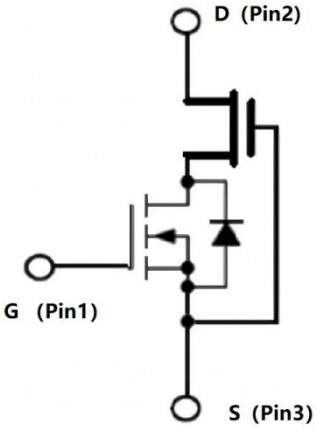
650V GaN FET Datasheet

1. Description

The KX1N65R250PD3, 650V, 245mΩ Gallium Nitride (GaN) FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.



Features

- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_G and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all GaN FETs for low loss during dead-times.
- Low Q_{RR} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements
- Improved safety & reliability due to cooler operation temperature

Applications

- High-frequency compact chargers with QR or ACF flyback topologies.
- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits
- High-efficiency/High-frequency LLC or other soft-switching topologies.

Key Performance Parameters	
V_{DSS}(V)	650
$V_{DSS(PK)}$(V) 1)	800
$R_{DS(ON)}$(mΩ) typ 2)	245
V_{th}(V)	1.8
Qoss(nC) typ	23
Q_G(nC) typ	22.8
Q_{RR}(nC) typ	18.8

1) Duty < 1%, spike duration < 1μs, nonrepetitive

2) Dynamic on-resistance, see below figures

Package Information	
Part #	KX1N65R250PD3
Package	DFN8x8-3
Size	8.0mm*8.0mm *1.0mm(H)

2. Maximum Ratings

Name	Parameter	Value	Unit
V_{DSS}	Maximum drain-to-source voltage (T_J = -55°C to 150°C)	650	V
$V_{DSS(PK)}$	Maximum drain-to-source peak voltage [a]	800	V
V_{GSS}	Maximum gate-to-source voltage	±20	V
P_D	Maximum power dissipation (T_C = 25°C)	65	W
I_{DS}	Maximum continuous drain current (T_C = 25°C)	9.2	A
	Maximum continuous drain current (T_C = 100°C)	7.35	A
$I_{DS\ (Pulse)}$	Maximum pulse drain current (T_C = 25°C) [b]	36	A
T_J	Operating Junction temperature	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [c]	260	°C

[a] Duty cycle < 1%, spike duration < 1μs

[b] Pulse width = 10μs

[c] Reflow MSL3

3. Thermal Characteristics

Name	Parameter	Typ	Unit
$R_{\Theta JC}$	Junction-to-case thermal resistance	2	°C/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance [d]	55	°C/W

[d] Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm2 copper area and 70μm thickness)

4. Device Characteristics

Static characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DSS}	Maximum drain-to-source voltage	650	-	-	V	V_{GS} = 0V
$V_{GS(th)}$	Gate threshold voltage	1.0	2	2.5	V	V_{DS} = V_{GS}, I_D = 0.5mA
$R_{DS(ON)}$	Drain-source on resistance a)	230	245	280	mΩ	V_{GS} = 10V, I_D = 8A
		-	530	570	mΩ	V_{GS} = 10V, I_D = 8A, T_J = 150°C
I_{DSS}	Off-state drain-to-source leakage current	-	1	25	μA	V_{DS} = 650V, V_{GS} = 0V
		-	10		μA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-source leakage current	-		100	nA	V_{GS} = 20V, V_{DS} = 0V
		-		-100	nA	V_{GS} = -20V, V_{DS} = 0V
R_G	Gate resistance	-	1	-	Ω	f = 1 MHz; open drain

Dynamic characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{ISS}	Input capacitance	-	905	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz
C_{OSS}	Output capacitance	-	10.6	-	pF	
C_{RSS}	Reverse switching capacitance	-	0.81	-	pF	
$C_{O(er)}$	Output capacitance, energy related b	-	48	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related c	-	58	-	pF	
Q_{OSS}	Output charge	-	23	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V, I_D=8A
$t_{D(ON)}$	Turn on delay time	-	13.9	-	ns	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 8A, R_{Gon} = R_{Goff} = 10Ω (See Figure 14)
t_R	Rise time	-	22	-	ns	
$t_{D(OFF)}$	Turn off delay time	-	44.6	-	ns	
t_F	Fall time	-	24.9	-	ns	

Gate charge characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
Q_G	Total gate charge	-	22.8	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 8A
Q_{GS}	Gate-source charge	-	3.85	-	nC	
Q_{GD}	Gate-drain charge	-	7.15	-	nC	
V_{Plat}	Gate Plateau Voltage	-	3.12	-	V	V_{DS} = 400V, I_D = 8A

a) Dynamic ON-resistance

Reverse Device Characteristics，T_J = 25°C unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
I_S	Reverse current	-	-	7.35	A	V_{GS}=0V, T_C=100°C, ≤20% duty cycle
V_{SD}	Reverse voltage [a]	-	1.9		V	V_{GS} = 0V, I_S = 5A
T_{RR}	Reverse recovery time	-	27.6	-	ns	I_S = 8A, V_{DD} = 400V, di/dt = 200A/μs
Q_{RR} [b]	Reverse recovery charge	-	18.8	-	nC	I_S = 8A, V_{DD} = 400V, di/dt = 200A/μs
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [b]	-	-	1200	A/μs	Circuit implementation and parameters on page 10 &11
I_{RDMC1}	Reverse diode switching current, repetitive (dc) [c, e]	-	-	11	A	Circuit implementation and parameters on page 10 &11
I_{RDMC2}	Reverse diode switching current, repetitive (ac) [c, e]	-	-	15	A	
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]	-	-	2400	A/μs	Circuit implementation and parameters on page 10 &11
I_{RDMT}	Reverse diode switching current, transient [d,e]	-	-	18	A	Circuit implementation and parameters on page 10 &11

[a] Including the effect of Dynamic ON-resistance

[b] Including Q_{OSS}

[c] Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency

[d] ≤300 pulses per second for a total duration ≤20 minutes

[e] I_{RDM} values can be increased by increasing R_G and C_{SN} on page 10 &11

5. Typical Characteristics (T_C = 25°C unless specified)

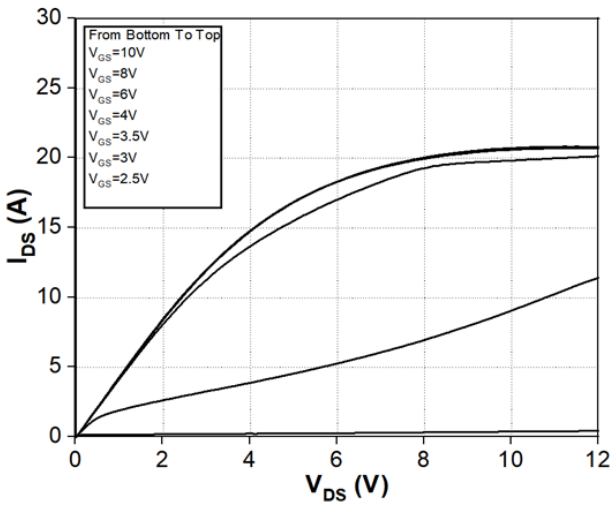


Figure 1. Typical Output Characteristics at T_J = 25°C

(Parameter: V_{GS})

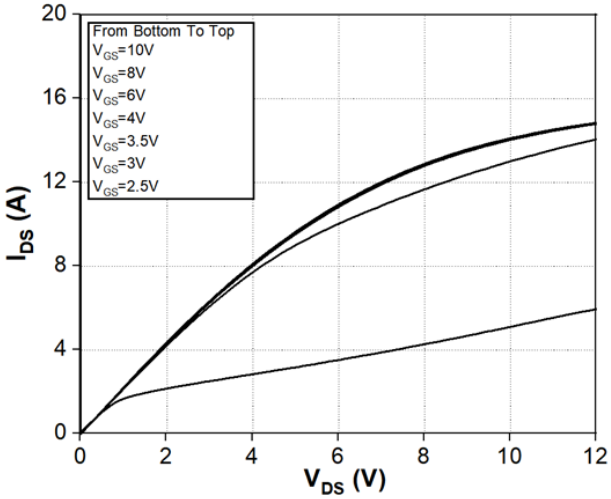


Figure 2. Typical Output Characteristics T_J=150°C

(Parameter： V_{GS})

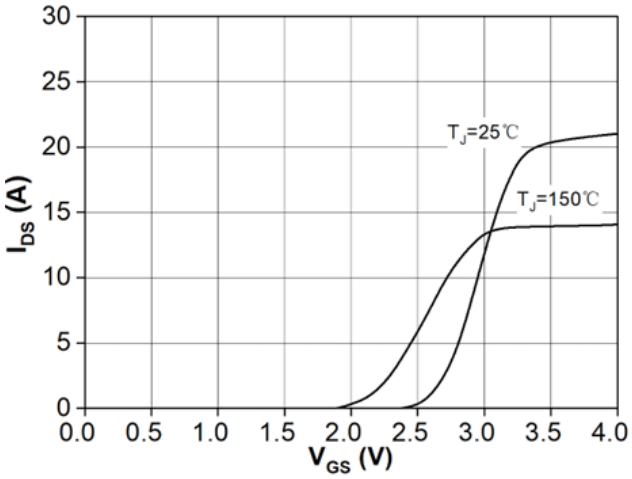


Figure 3. Typical Transfer Characteristics

(V_{DS}=10V, parameter: T_j)

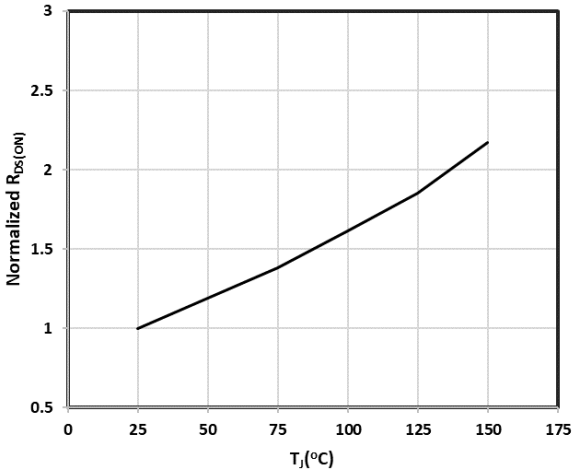


Figure 4. Normalized On-resistance

(V_{GS} =10V， I_D=8A)

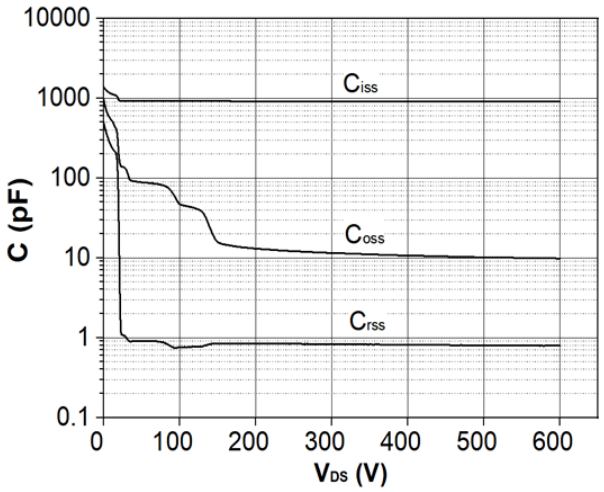


Figure 5. Typical Capacitance

(V_{GS} = 0V, f = 1MHz)

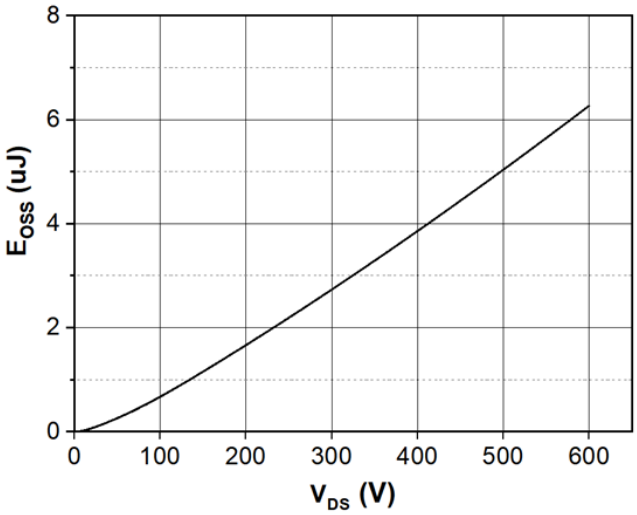


Figure 6. Typical C_{OSS} Stored Energy

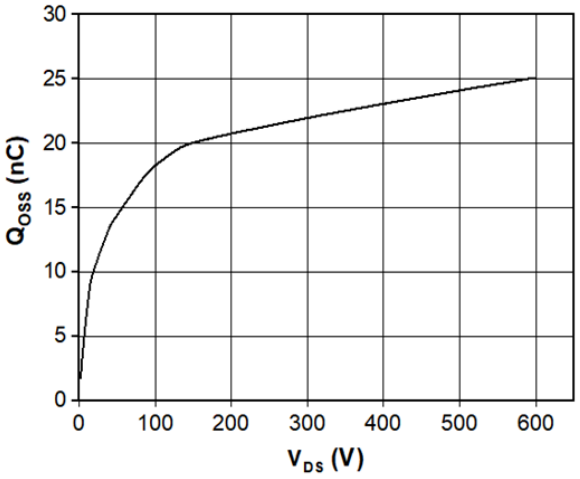


Figure 7. Typical Q_{OSS}

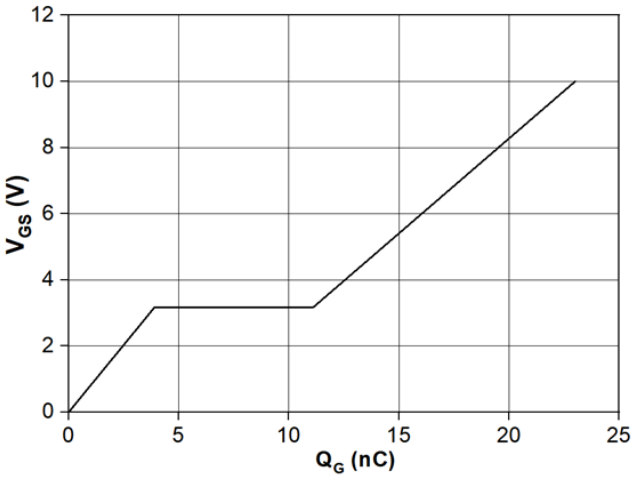


Figure 8. Typical Gate Charge

I_{DS}=8A, V_{DS}=400V

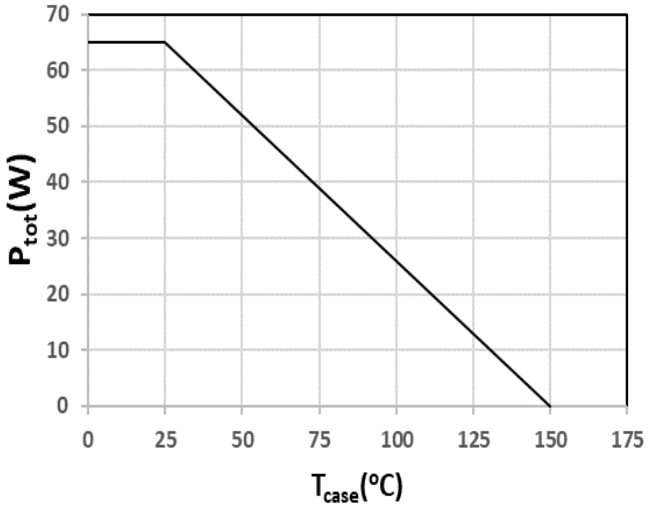


Figure 9. Power Dissipation

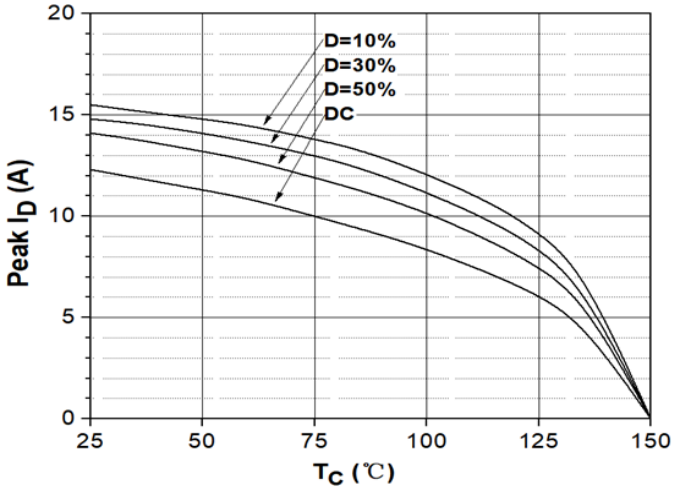


Figure 10. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V

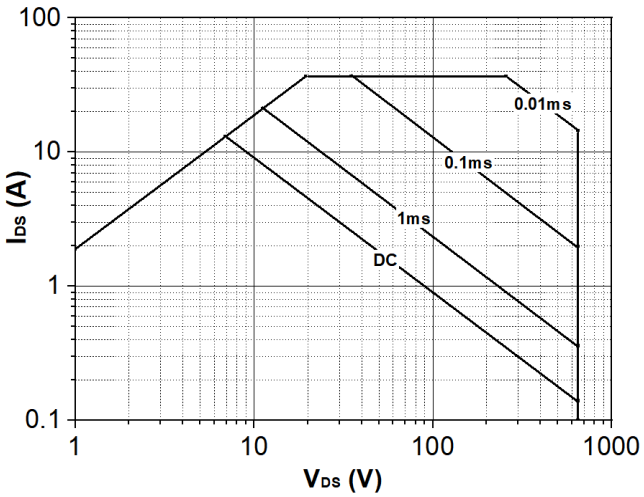


Figure 11. Safe Operating Area T_C=25°C

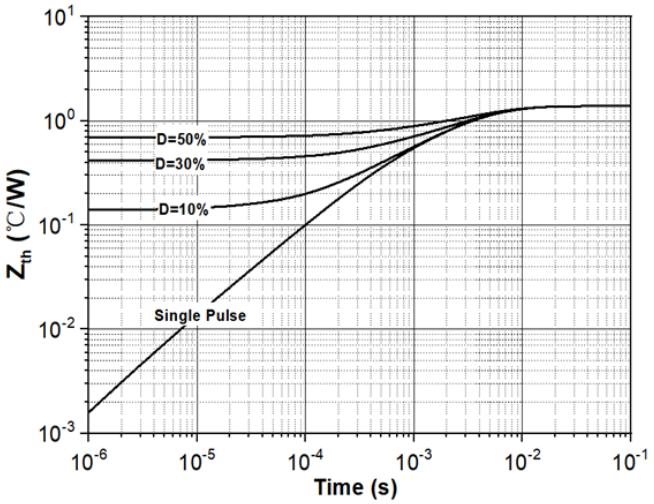


Figure 12. Transient Thermal Resistance

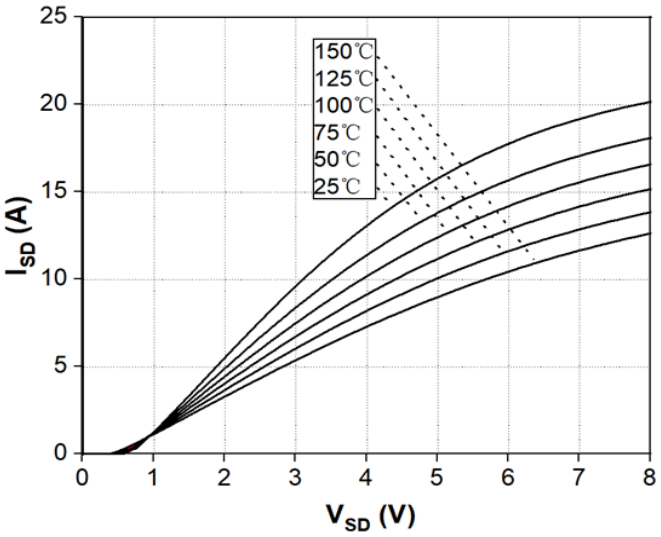


Figure 13. Forward Characteristics of Rev. Diode

$I_S=f(V_{SD})$, Parameter T_J

Test Circuits and Waveforms

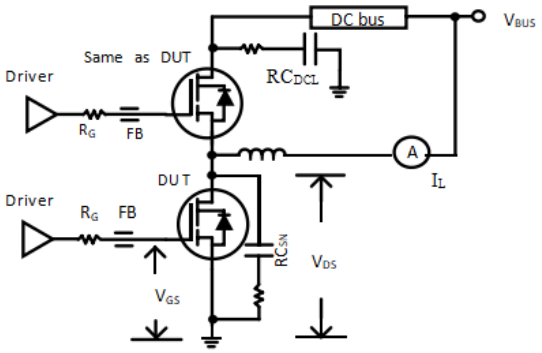


Figure 14. Switching Time Test Circuit

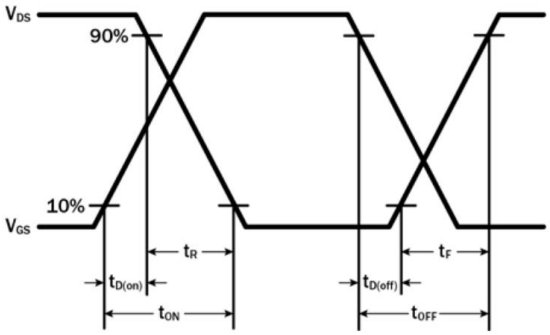


Figure 15. Switching Time Waveform

(See circuit implementation on page 10 &11
for methods to ensure clean switching)

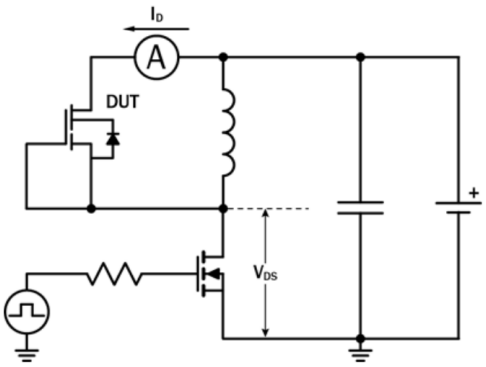


Figure 16. Diode Characteristics Test Circuit

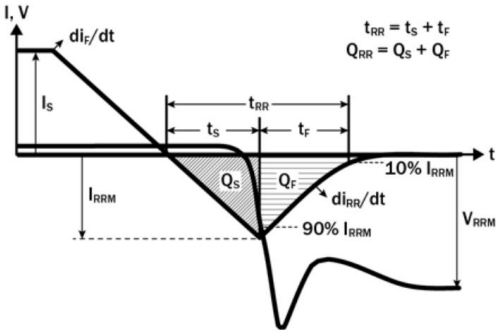


Figure 17. Diode Recovery Waveform

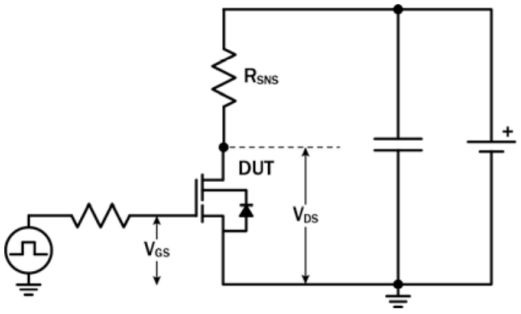


Figure 18. Dynamic RDS(on)eff Test Circuit

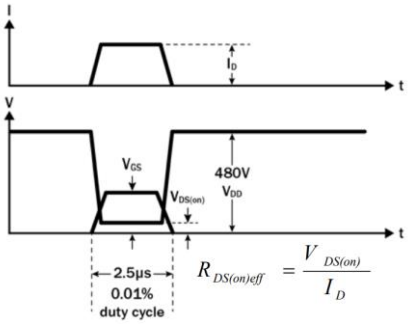


Figure 19. Dynamic RDS(on)eff Waveform

6. Circuit Implementation

(1) Flyback Schematic

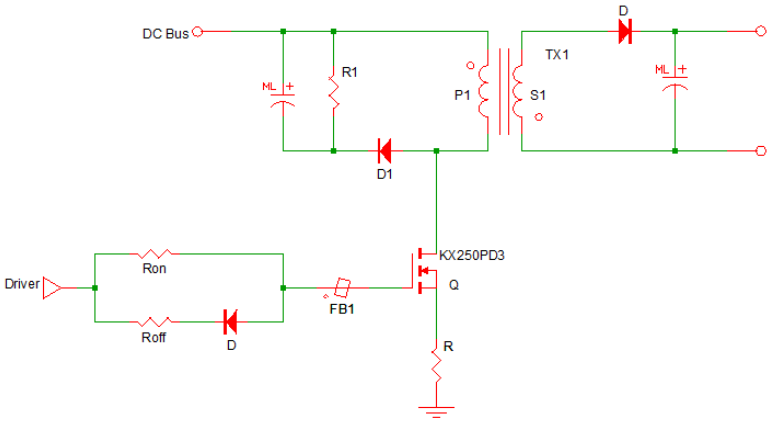


Figure 20. Simplified flyback schematic

Recommended gate drive: (0V, 12V)

Ferrite Bead (FB)	RON	ROFF
60-300Ω @100MHz	100-330Ω	2-10Ω

Recommended gate drive: (0V, 6V)

Ferrite Bead (FB)	RON	ROFF
60-300Ω @100MHz	10-120Ω	2-5Ω

(2) Half-bridge Schematic

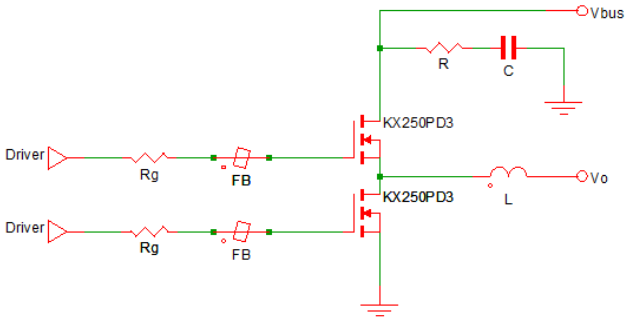


Figure 21. Simplified half-bridge schematic

Recommended gate drive: (0V, 12V) with $R_{G(tot)}$ = 30 Ω [a)]

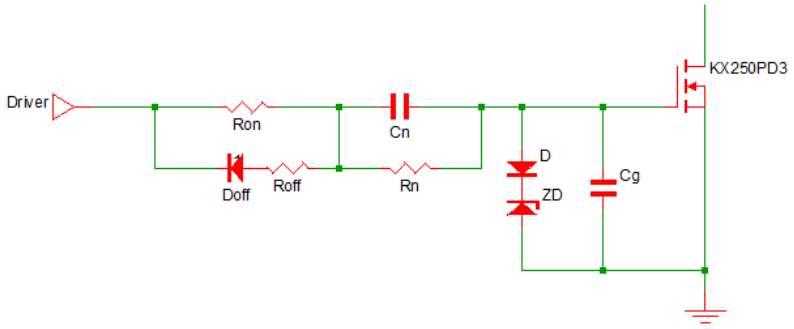
Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) [b)]
200-300Ω @100MHz	4.7-10nF + 5Ω

Notes:

[a)] For bridge topologies only. R_G could be smaller in single ended topologies.

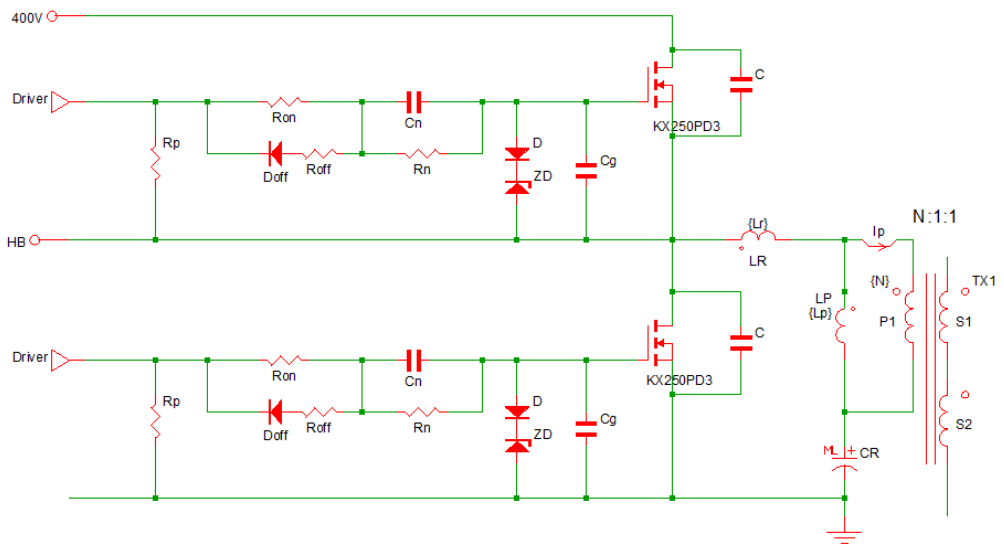
[b)] RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitors should be located away from the RC_{DCL}.

(3) Negative Gate Controlled Schematic (Recommended)



Symbol	Rec. Value	Rec.Package	Function
Cn	47~330nF	0402 / 0603	Hold negative voltage for turning off
Rn	~10KΩ	0402 / 0603	Keep the driving voltage
D	20V/1A Diode	SOD323	Zener Clamp the negative gate voltage
ZD	8V2,7V5	SOD323	Zener Clamp the positive gate voltage
Cg	~1nF	0402 / 0603	Gate negaitve voltage overshotting buffer
Ron	47~300Ω	0402 / 0603	Control turn-on speed
Roff	2~5Ω	0402 / 0603	Control turn-off speed
Doff	20V/1A Diode	SOD323	Enable independent turn-off speed control

(4) Negative Gate Controlled LLC Schematic



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Ron	47~300Ω	0402 / 0603	Control turn-on speed
Roff	2~5Ω	0402 / 0603	Control turn-off speed
Doff	20V/1A Diode	SOD323	Enable independent turn-off speed control
Rp	>20KΩ	0402 / 0603	control IC configuration
C	10~100pF	0402 / 0603	Hold negative voltage for turning off

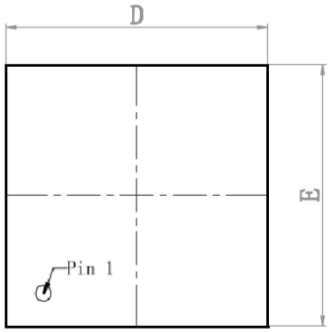
7. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific
PCB layout guidelines and probing techniques.

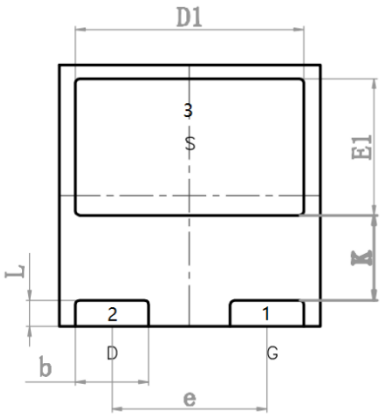
DO	DO NOT
Place gate driver close to the GaN device and separate input traces from output traces	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor
Minimize trace length of the PCB layout for both drive loop and power loop	Use a traditional differential voltage probe for V_{GS} of high side device

8. Package Dimensions

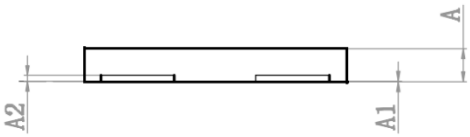
Dimension / Symbol	MIN	NOM	MAX	Dimension / Symbol	MIN	NOM	MAX
A	0.90	1.00	1.10	K	---	2.50	---
A1	0.00	---	0.05	b	2.15	2.25	2.35
A2	---	0.20	---	L	0.70	0.80	0.90
D	7.90	8.00	8.10	e	---	4.75	---
D1	6.90	7.00	7.10				
E	7.90	8.00	8.10	DFN 8x8-3（KuanXin: KX1N65R***PD3）			
E1	4.10	4.20	4.30	Unit:	mm	Date:	Jul.,2022



Top View



Bottom View



Side View

9. Revision History

Revision No.	Date	Description of Change(s)
Rev0.1	2022-07-18	Draft
Rev0.8	2022-09-24	Update the test data
Rev0.9	2022-12-29	Update the 3rd party test data
Rev1.0	2023-01-08	Add room for thermal resistance
Rev1.1	2023-08-01	Add negative Gate control schematic