650V GaN FET Datasheet

1. Description

The KX1NR250PD8 FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

DFN 8 x 8

Features

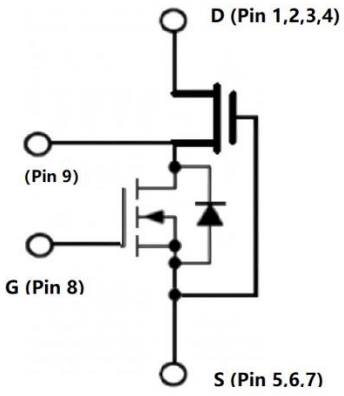
- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_G and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all GaN FETs for low loss during dead-times.
- Low Q_{RR} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements
- Improved safety & reliability due to cooler operation temperature

Applications

- High-frequency compact chargers with QR or ACF flyback topologies.
- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits
- High-efficiency/High-frequency LLC or other soft-switching topologies.



Key Performance Parameters	
V_{DSS}(V)	650
$V_{DSS(PK)}$(V) 1)	800
$R_{DS(ON)}$(mΩ)typical 2)	250
Qoss(nC)	23.3
Q_G(nC)	19
Q_{RR}(nC)	2

Package Information	
Part #	KX1N65R250PD8
Package	DFN8x8
Size	8.0mm*8.0mm *0.85mm(H)

1) Duty < 1%, spike duration < 1µs, nonrepetitive

2) Dynamic on-resistance

2. Maximum Ratings

Name	Parameter	Value	Unit
V_{DSS}	Maximum drain-to-source voltage (T_J = -55°C to 150°C)	650	V
$V_{DSS(PK)}$	Maximum drain-to-source peak voltage [a]	800	V
V_{GSS}	Maximum gate-to-source voltage	±20	V
P_D	Maximum power dissipation (T_C = 25°C)	65	W
I_{DS}	Maximum continuous drain current (T_C = 25°C)	9.2	A
	Maximum continuous drain current (T_C = 100°C)	7.35	A
$I_{DS\ (Pulse)}$	Maximum pulse drain current (T_C = 25°C) [b]	20	A
T_J	Operating Junction temperature	-55 to +150	°C
T_S	Storage temperature	-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [c]	260	°C

[a] Duty cycle < 1%, spike duration < 1μs

[b] Pulse width = 10μs

[c] Reflow MSL3

3. Thermal Characteristics

Name	Parameter	Typ	Unit
$R_{\Theta JC}$	Junction-to-case thermal resistance	4	°C/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance [d]	60	°C/W

[d] Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm2 copper area and 70μm thickness)

4. Device Characteristics

Static characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DSS}	Maximum drain-to-source voltage	650	-	-	V	V_{GS} = 0V
$V_{GS(th)}$	Gate threshold voltage	1.0	1.9	2.5	V	V_{DS} = V_{GS}, I_D = 0.25mA
$R_{DS(ON)}$	Drain-source on resistance a)	-	255	300	mΩ	V_{GS} = 6V, I_D = 4A
		-	450	-	mΩ	V_{GS} = 6V, I_D = 4A, T_J = 150°C
I_{DSS}	Off-state drain-to-source leakage current	-	0.8	10	μA	V_{DS} = 650V, V_{GS} = 0V
		-		-	μA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-source leakage current	-	43	100	nA	V_{GS} = 20V, V_{DS} = 0V
		-	- 41	-100	nA	V_{GS} = -20V, V_{DS} = 0V
R_G	Gate resistance		2.5		Ω	f = 1 MHz; open drain

Dynamic characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{ISS}	Input capacitance	-	873	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz
C_{OSS}	Output capacitance	-	9.9	-	pF	
C_{RSS}	Reverse switching capacitance	-	1.1	-	pF	
Q_{OSS}	Output charge	-	23.3	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
$t_{D(ON)}$	Turn on delay time	-	16.8	-	ns	V_{DS} = 400V, V_{GS} = 0V to 8V, I_D = 4A, R_G = 30Ω
t_R	Rise time	-	21.8	-	ns	
$t_{D(OFF)}$	Turn off delay time	-	40	-	ns	
t_F	Fall time	-	23	-	ns	

Gate charge characteristics (Tested at Tj = 25 °C, unless otherwise noted)

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
Q_G	Total gate charge	-	19	-	nC	V_{DS} = 400V, V_{GS} = 0V to 8V, I_D = 4A
Q_{GS}	Gate-source charge	-	3.3	-	nC	
Q_{GD}	Gate-drain charge	-	7.1	-	nC	
V_{Plat}	Gate Plateau Voltage	-	2.8	-	V	V_{DS} = 400V I_D = 4A

[a] Dynamic ON-resistance

Reverse Device Characteristics，T_J = 25°C unless specified

Name	Parameter	Min	Typ	Max	Unit	Test Conditions
I_S	Reverse current	-	-	7	A	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle
$I_{S\ (Pulse)}$	Reverse pulse current	-	-	11.3	A	V_{GS} = 0V, V_{SD} = 6V, pulse width ≤ 100μs, T_J = 125°C
V_{SD}	Reverse voltage [a]	-	1.8	2.2	V	V_{GS} = 0V, I_S = 4A
t_{RR}	Reverse recovery time	-	8	-	ns	I_S = 4A, V_{DD} = 400V, di/dt = 1000A/μs
$Q_{RR\ b)}$	Reverse recovery charge	-	2	-	nC	I_S = 4A, V_{DD} = 400V, di/dt = 1000A/μs

[a] Including the effect of Dynamic ON-resistance

[b] Including Q_{OSS}

5. Typical Characteristics (T_C = 25°C unless specified)

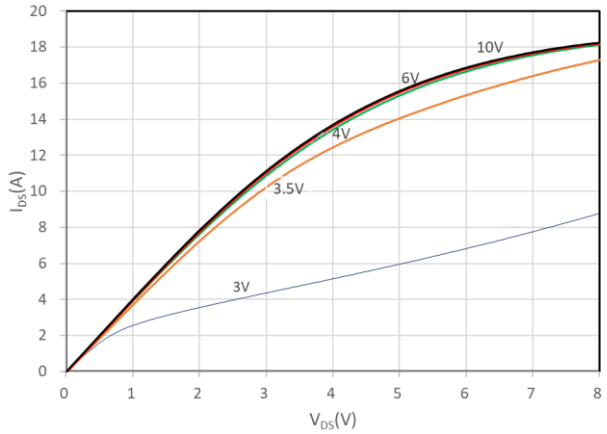


Figure 1. Typical Output Characteristics at T_J = 25°C (Parameter: V_{GS})

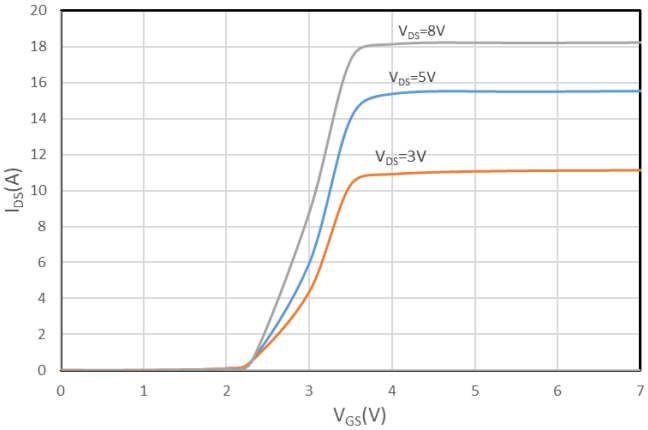


Figure 2. Typical transfer Characteristics (pulse width < 100 μs)

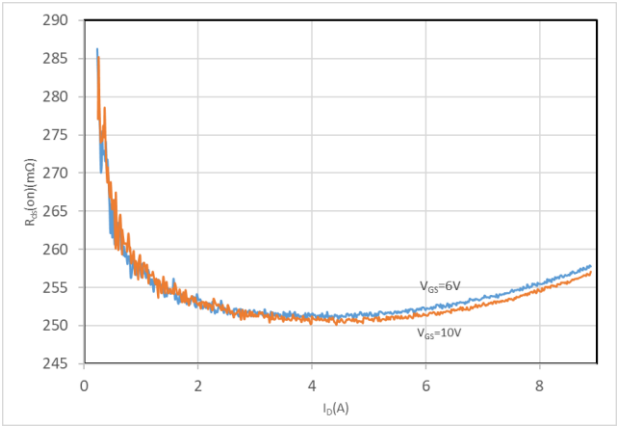


Figure 3. Typical Rds(on) Characteristics characteristics (V_{GS} = 6V and V_{GS} = 10V)

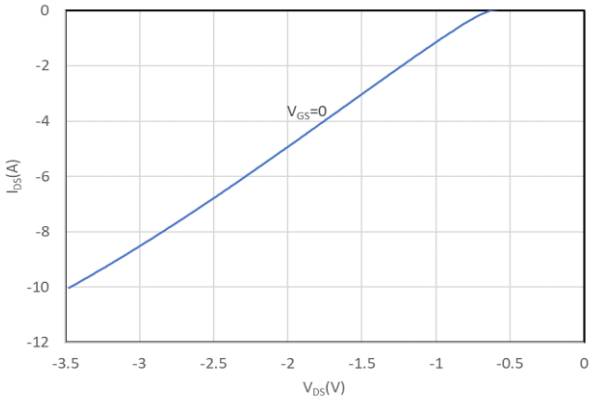


Figure 4. Typical channel reverse (V_{GS} = 0V)

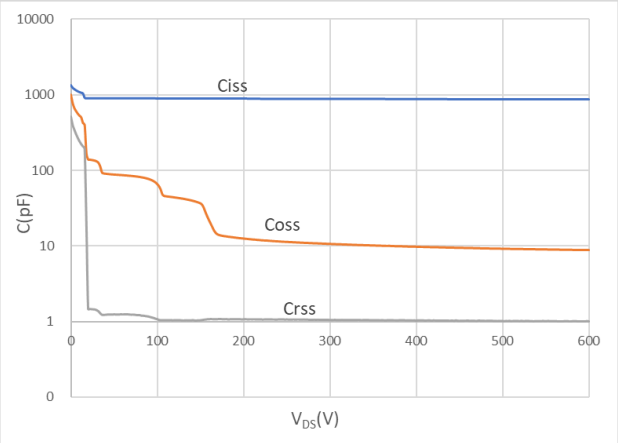


Figure 5. Typical Capacitance

(V_{GS} = 0V, *f* = 1MHz)

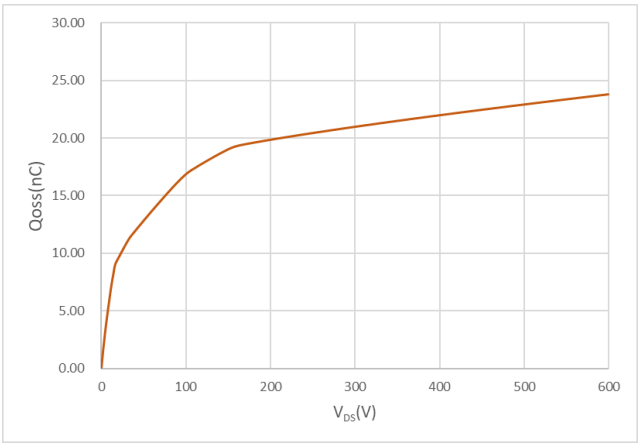


Figure 6. Typical output charge

(V_{GS} = 0V, *f* = 1MHz)

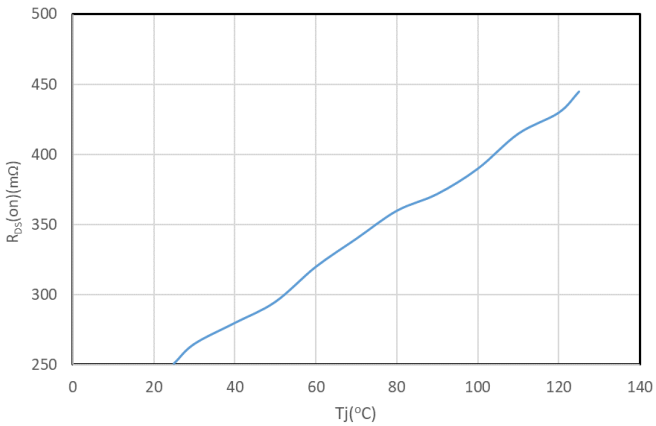


Figure 7. Typical drain to source on-resistance (VG = 6 V)

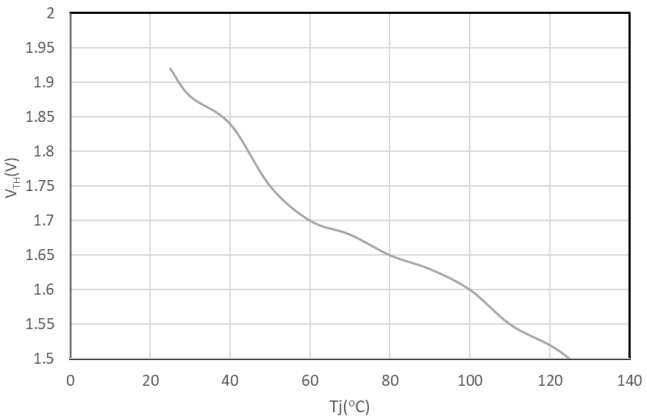


Figure 8. Typical gate threshold voltage

(VG = VD, ID = 1mA)

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific
PCB layout guidelines and probing techniques.

DO	DO NOT
The package has an exposed center pad (ePAD) as a thermal enhancement at the bottom of the package. The ePAD needs to be soldered directly to the PCB for an efficient thermal path from the die to the board.	Pin9 is another exposed pad with die connection, but it will keep 30V voltage when GaN MOS is open in working time. The pin must be "NO-CONNECTED" with any signals or GND or Power in the design.
Place gate driver close to the GaN device and separate input traces from output traces	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor
Minimize trace length of the PCB layout for both drive loop and power loop	Use a traditional differential voltage probe for V_{gs} of high side device

7. Circuit Implementation

(1) Flyback Schematic

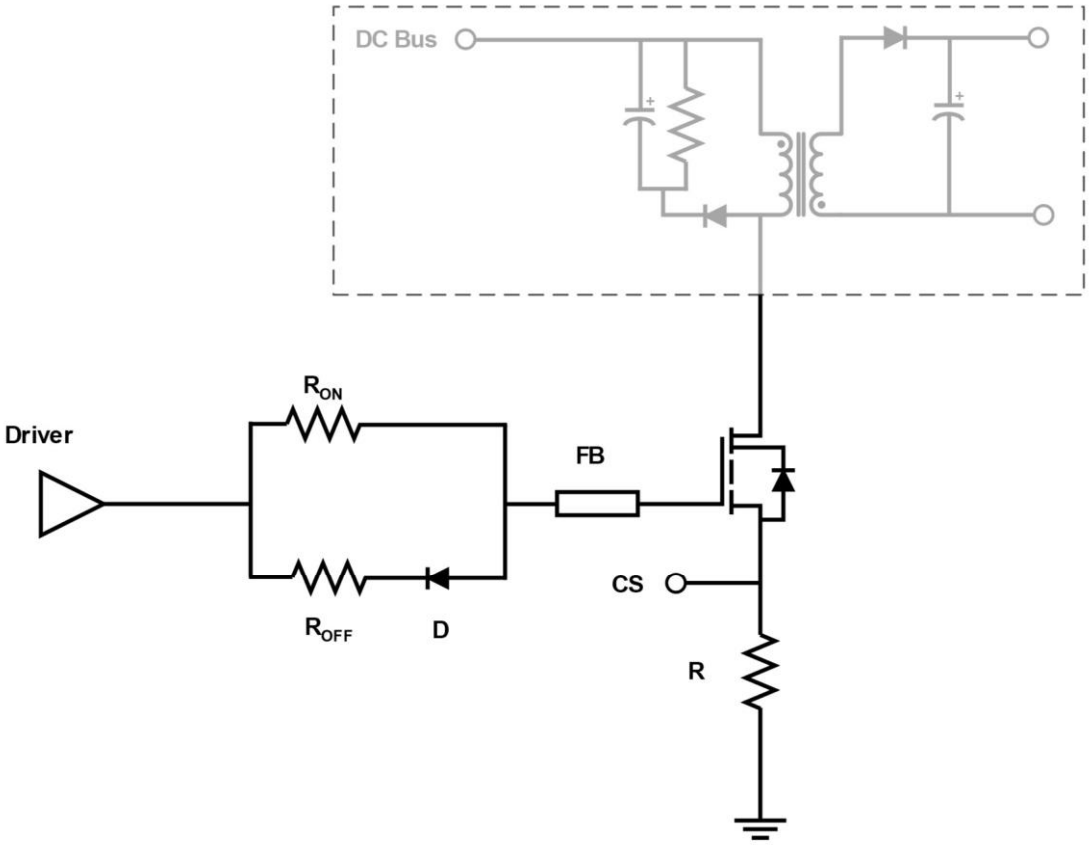


Figure 13. Simplified flyback schematic

Recommended gate drive: (0V, 12V)

Ferrite Bead (FB)	RON	ROFF
60-300Ω @100MHz	100-330Ω	2-10Ω

Recommended gate drive: (0V, 6V)

Ferrite Bead (FB)	RON	ROFF
60-300Ω @100MHz	10-120Ω	2-5Ω

(2) Half-bridge Schematic

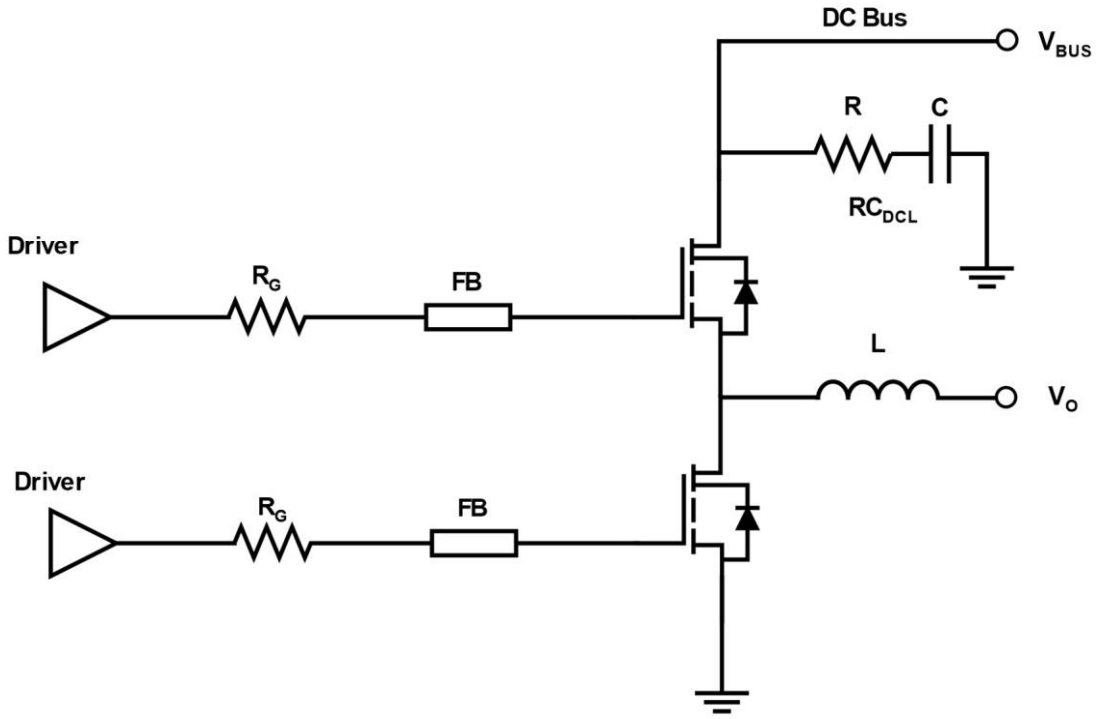


Figure 14. Simplified half-bridge schematic

Recommended gate drive: (0V, 12V) with $R_{G(tot)}$ = 30 Ω [a)]

Gate Ferrite Bead (FB)	Required DC Link RC Snubber (RC_{DCL}) [b)]
200-300Ω @100MHz	4.7-10nF + 5Ω

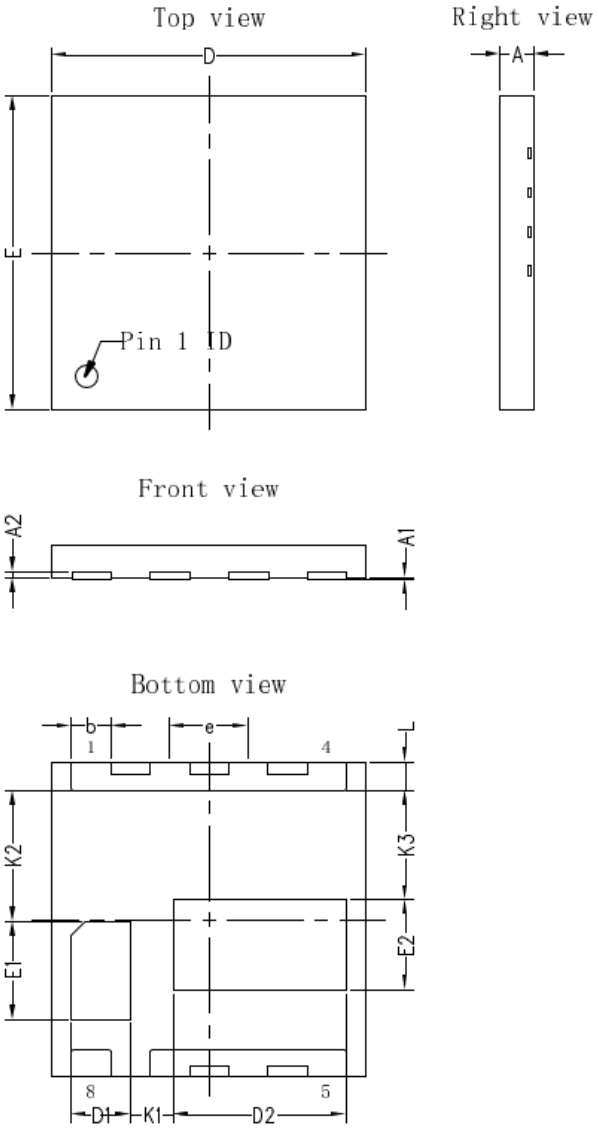
Notes:

[a)] For bridge topologies only. R_G could be smaller in single ended topologies.

[b)] RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitors should be located away from the RC_{DCL}.

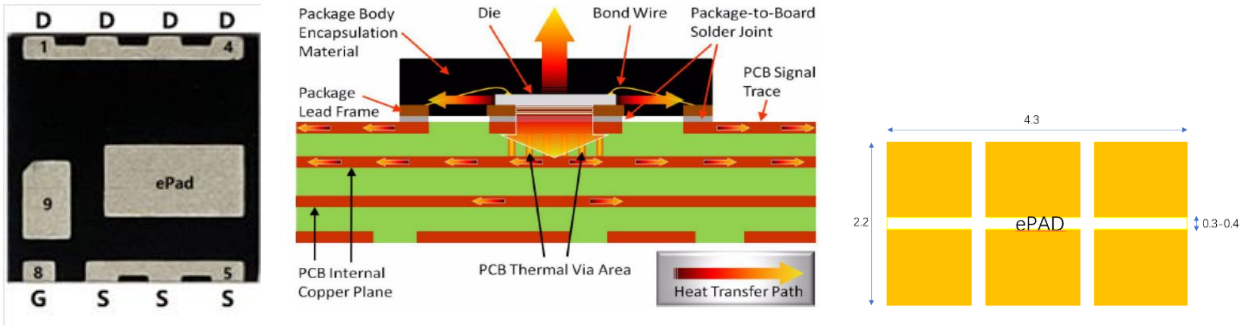
8. Package Dimensions

Dimension / Symbol	MIN	NOM	MAX	Dimension / Symbol	MIN	NOM	MAX
A	0.75	0.85	0.95	E2	2.20	2.30	2.40
A1	0.00	0.02	0.05	K1	1.00	1.10	1.20
A2	---	0.203	---	K2	3.24	3.34	3.44
b	0.95	1.00	1.05	K3	2.70	2.80	2.90
D		8.00		e	---	2.00	---
D1	1.40	1.50	1.60	L	0.60	0.70	0.80
D2	4.30	4.40	4.50				
E	---	8.00	---	DFN 8x8（KuanXin: KX1N65R***PD8）			
E1	2.40	2.50	2.60	Unit:	mm	Date:	Jul.,2022



9. PCB Land Pattern Guidelines

The DFN is a surface mountable package with bottom termination of its external connections (pins). The land pattern design for all DFN type packages is based on the IPC-7093 and IPC-7351 standards. A Non-Solder-Mask Defined (NSMD) pad design is suggested for all perimeter pins.
The solderable area of the center pad, as defined by the solder mask (SMD) or NSMD, should match the size of the ePAD of the component. An array of solid vias should be incorporated in the PCB center pad design in order to achieve maximum thermal and electrical performance of the device. Examples of typical PCB land pattern guidelines and dimensions are provided below, which can be segmented into symmetric pad array.



10. Revision History

Revision No.	Date	Description of Change(s)
Rev01	2022-09-19	First Edition
Rev05	2022-11-19	Update test data
Rev06	2022-12-07	Update the data of RΘJA