LITE-ON SEMICONDUCTOR

L02U5V0NA-4C

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - 5.0 Volts
POWER DISSIPATION - 20 Watts

GENERAL DESCRIPTION

The L02U5V0NA-4C is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Protects four I/O lines (Data line)
- Max. peak pulse power: Ppp=20w at tp = 8/20 us.
- Low capacitance: 0.28pF typical (I/O to I/O)
- IEC 61000-4-2 ,>±30KV(air)；>±16KV(contact)
- Qualified to AEC-Q101 Rev_C

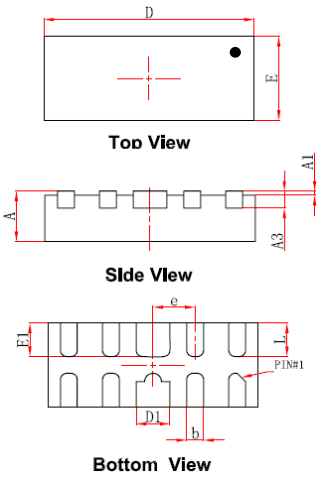
MECHANICAL DATA

- Case material:"Green"molding compound UL flammability classification 94V-0 (No Br, Sb, Cl)
- Terminals: lead free plating
- Component in accordance to RoHs 2011/65/EU

APPLICATION

- High definition multi-media interface (HDMI) 1.3 & 1.4 and 2.0 version
- Digital visual interface (DVI)
- Display prot™ interface
- SATA and ESATA interface
- USB 3.0 / 3.1
- Desktop and Notebooks PCs

SLP2510P8



SLP2510P8		
DIM.	MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.152 REF.	
D	2.45	2.55
E	0.95	1.05
D1	0.35	0.45
E1	0.35	0.45
b	0.15	0.25
e	0.50 BSC	
L	0.35	0.45
All dimension in millimeter		

PIN ASSIGNMENT	
1,2,4,5	Input lines
6,7,9,10	NC
3,8	Ground

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

ABSOLUTE RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (tp = 8/20us)	P_{pk}	20	W
Peak pulse current (tp = 8/20us)	I_{pp}	1.5	A
Operating junction temperature range	T_J	-55 to +125	°C
Storage temperature range	T_{STG}	55 to +150	°C
Soldering temperature, t max = 10s	T_L	260	°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Reverse standoff voltage	Any I/O pin to ground	V_{RWM}	--	--	5.0	V
Reverse leakage current	V_{DRM} = 5V, Any I/O pin to ground	I_{RM}	--	--	0.5	uA
Breakdown voltage	I_R = 1 mA	V_{BR}	6.0	--	9.0	V
Clamping Voltage	Ipp=1A, tp = 8/20 us	Vc	--	--	11	V
Junction capacitance	VR = 0~2.5V, f = 1MHz, between I/O pins	C_J	--	0.28	0.3	pF
	VR = 0~2.5V, f = 1MHz, any I/O pin to ground		--	0.43	0.5	

RATING AND CHARACTERISTIC CURVES
L02U5V0NA-4C

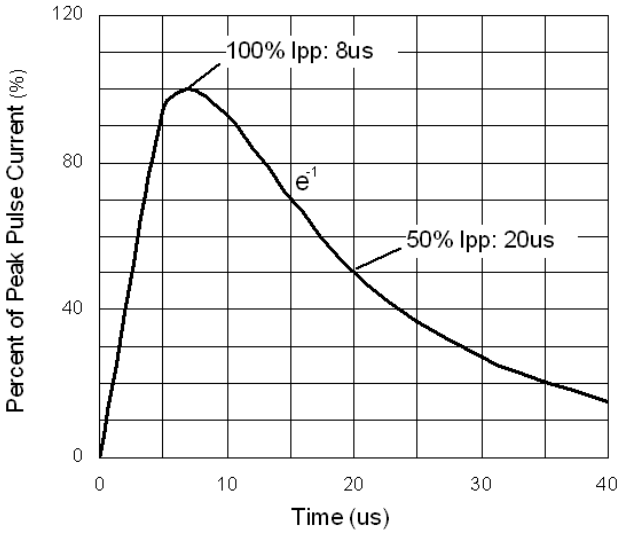


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

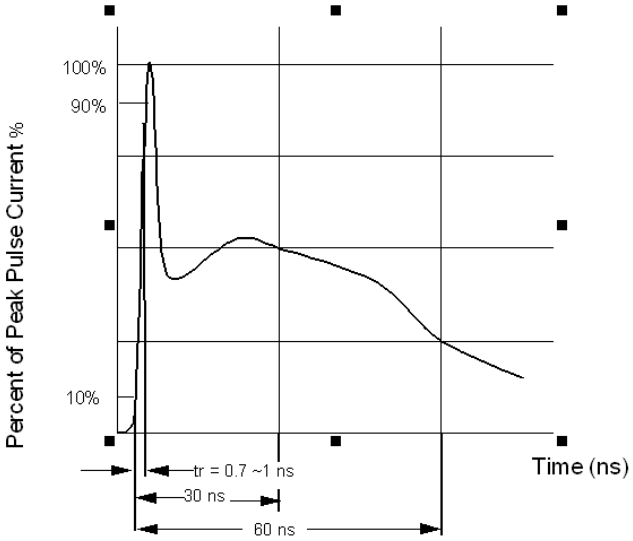


Figure 2. ESD pulse waveform according to IEC 61000-4-2

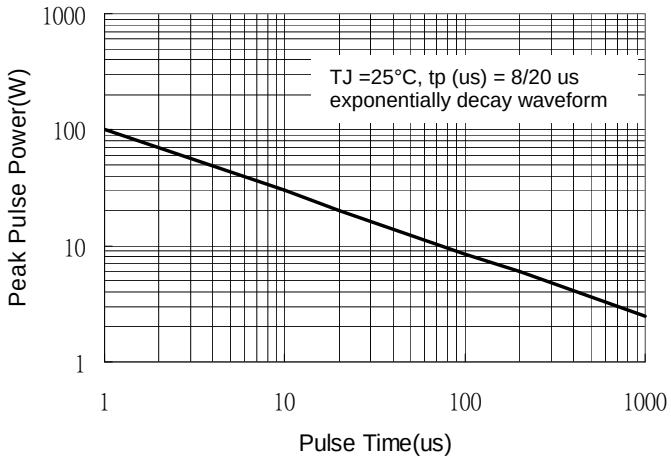


Figure 3. Power Dissipation versus Pulse Time

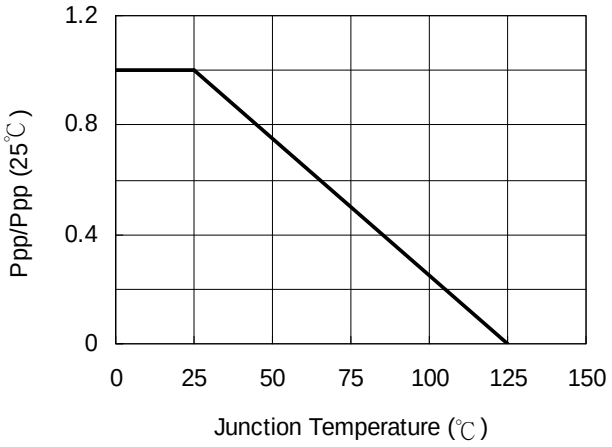


Figure 4. Peak pulse power versus TJ

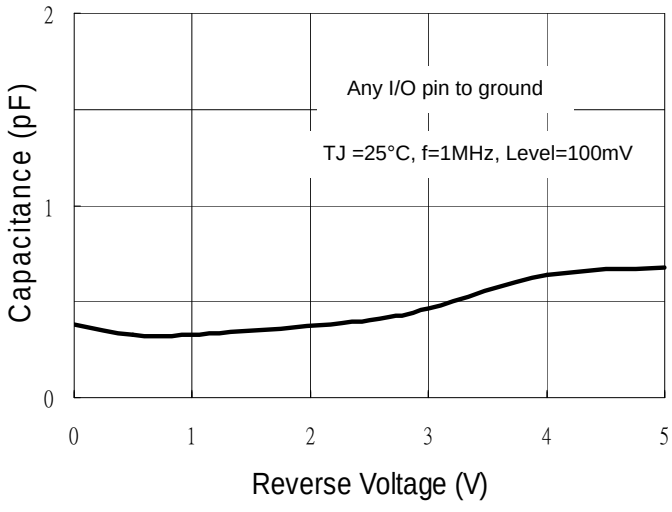


Figure 5. Typical Junction Capacitance

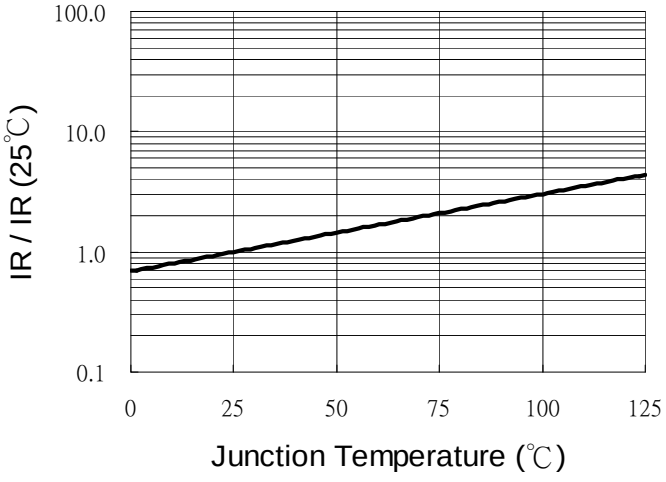


Figure 6. Reverse Leakage Current versus TJ

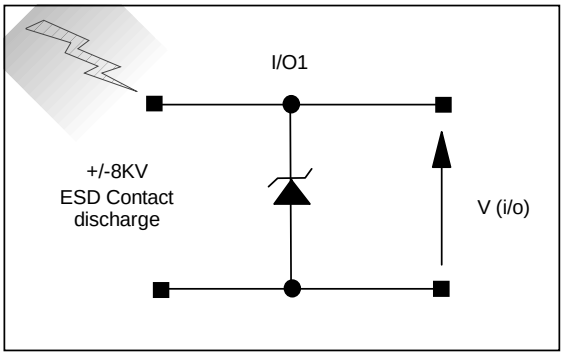


Figure 7. ESD Test Configuration

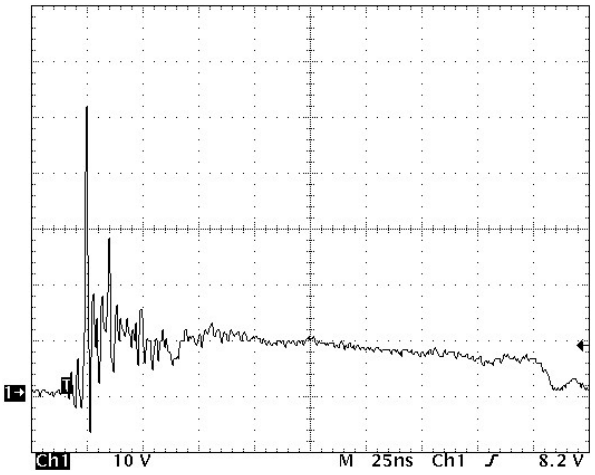


Figure 8. Clamped +8 kV ESD voltage waveform

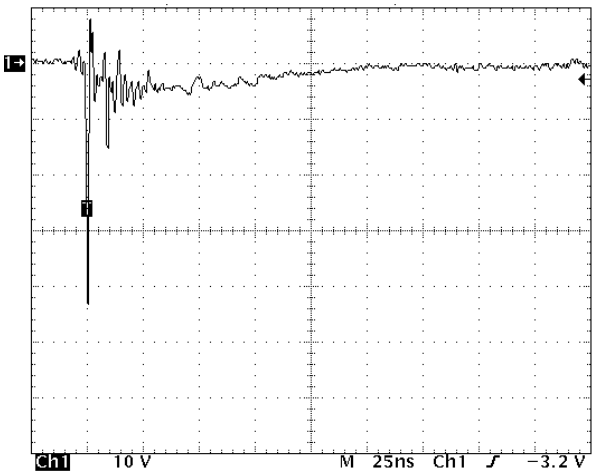
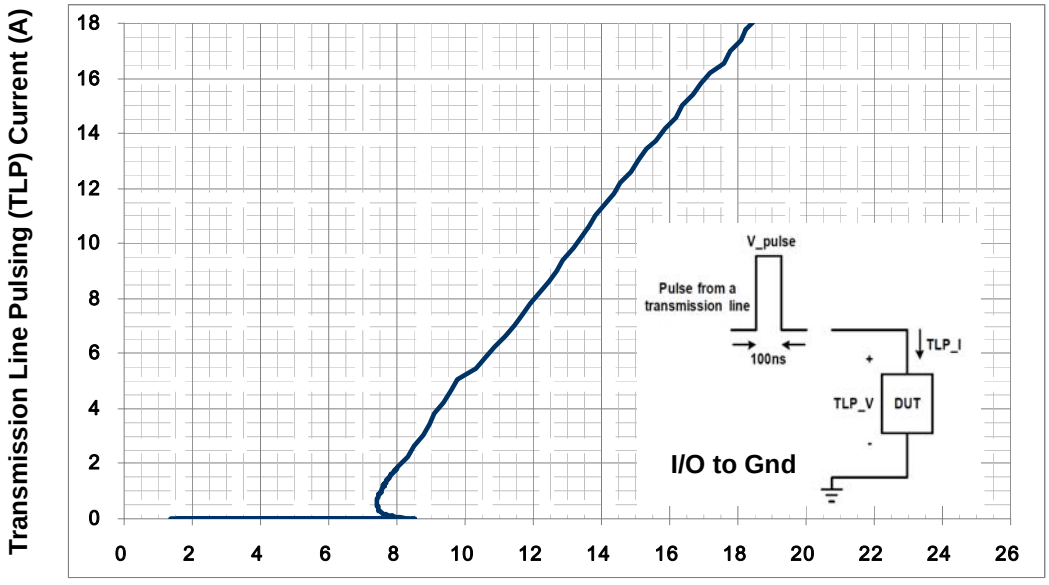


Figure 9. Clamped -8 kV ESD voltage waveform

Transmission Line Pulsing (TLP) Measurement



Transmission Line Pulsing (TLP) Voltage (V)

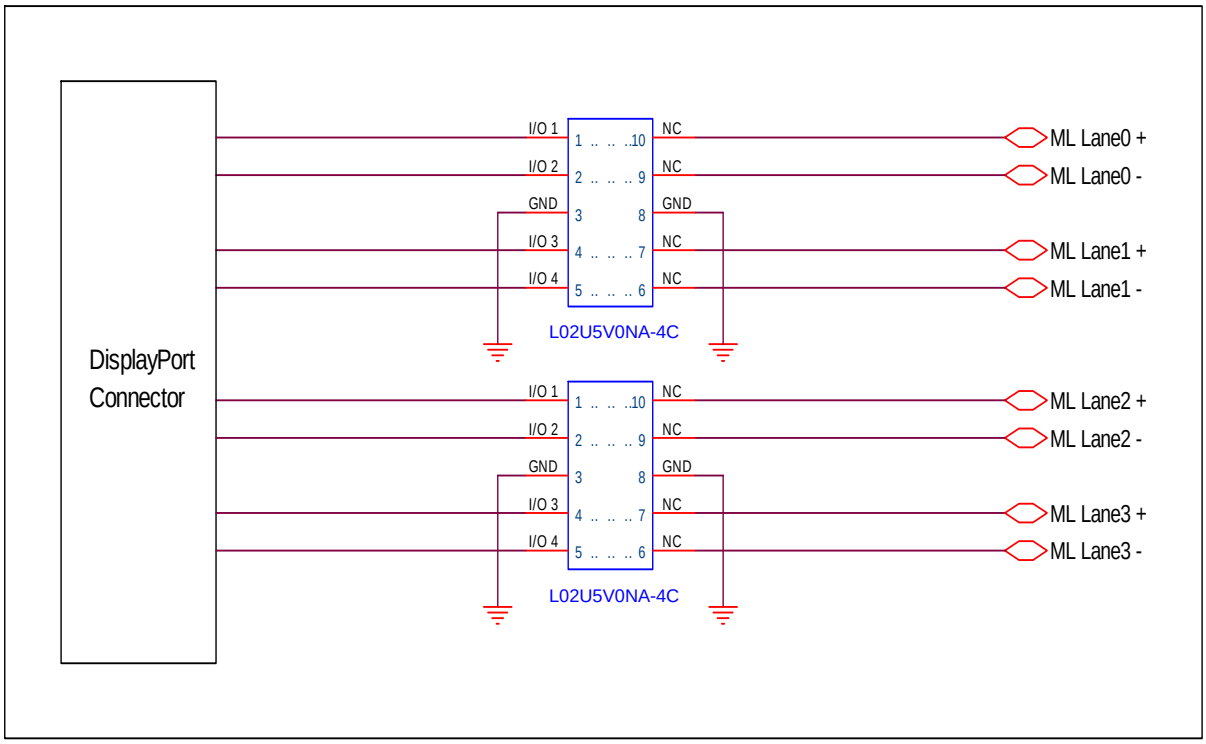


Figure 10. Display Port ESD Protection

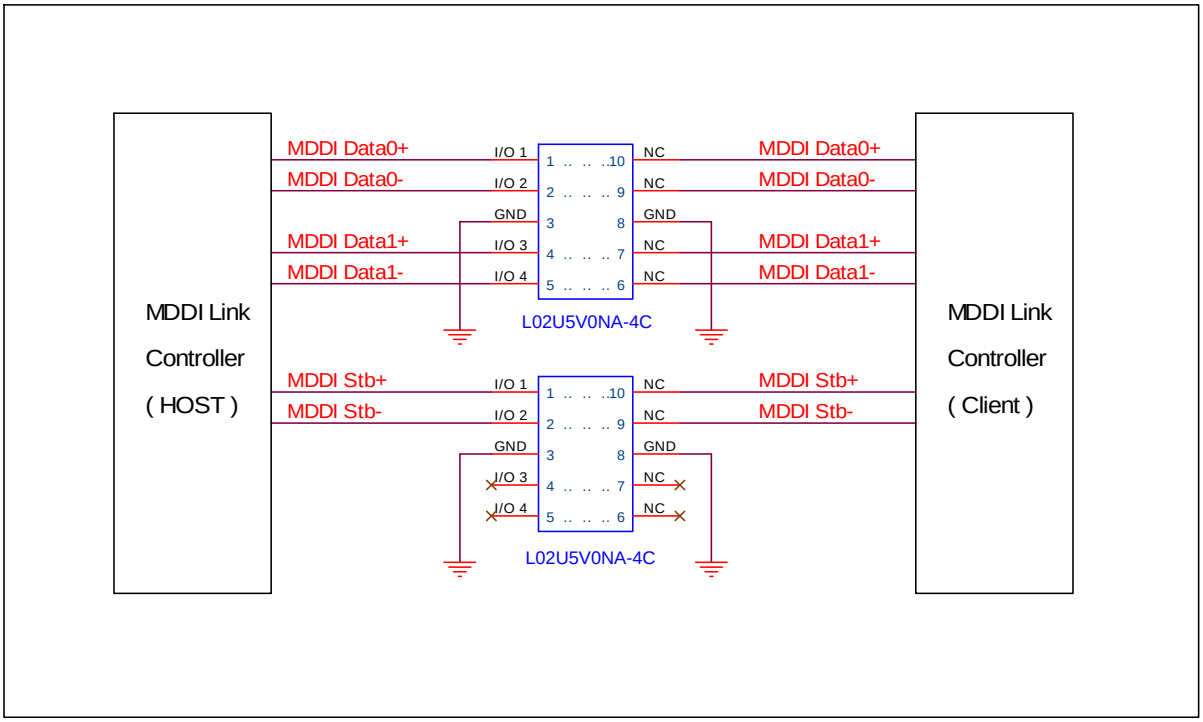


Figure 11. MDDI Interface ESD Protection

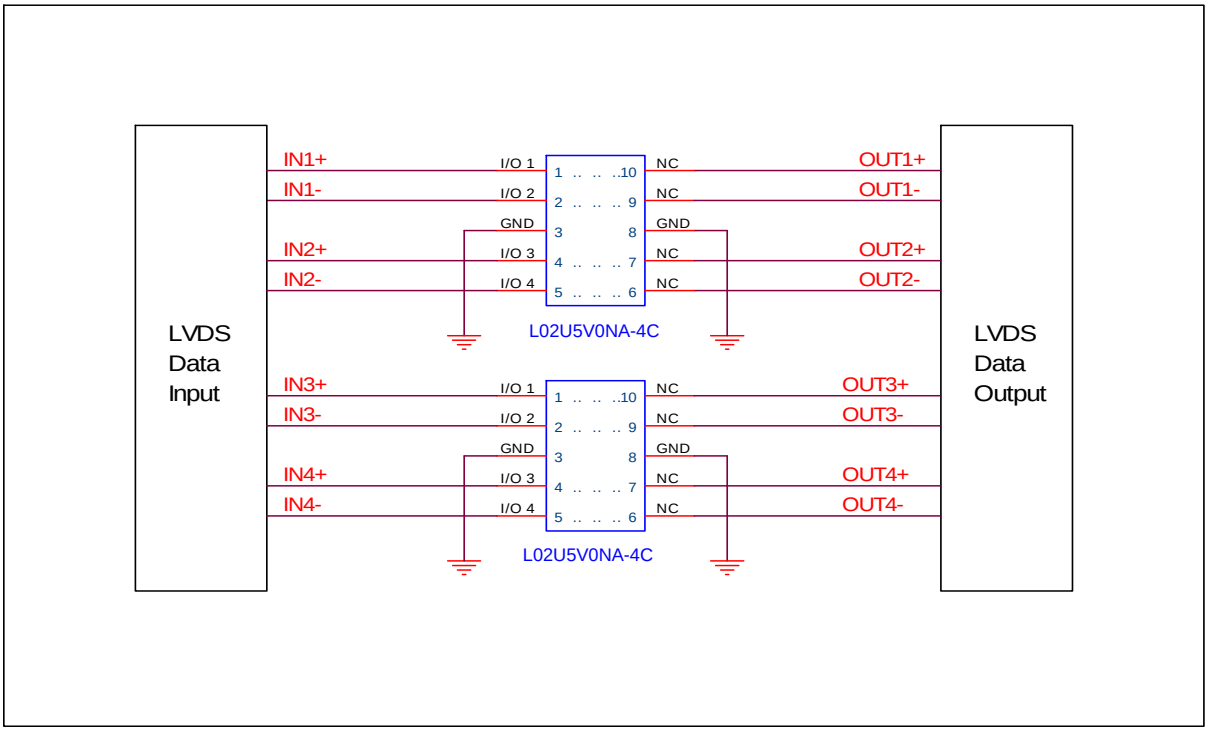


Figure 12. LVDS Interface ESD Protection

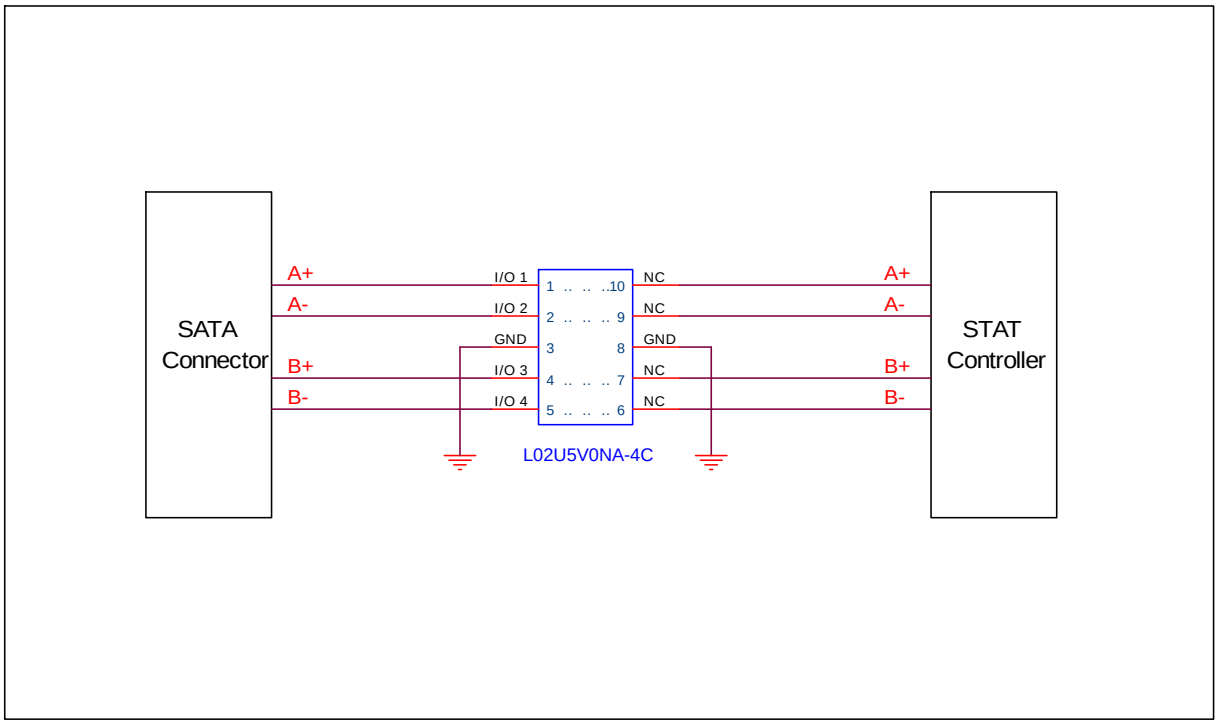
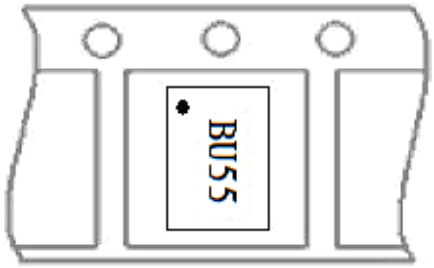


Figure 13. Serial ATA ESD Protection

MARKING AND PACKAGING INFORMATION
L02U5V0NA-4C

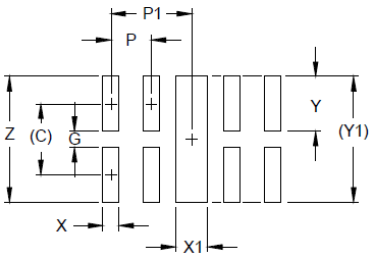
Marking and Orientation :



Packaging Information :

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L02U5V0NA-4C	3000	7	45000	90K/180K

SLP2510P8 Soldering Pad Layout :



Dim.	Millimeters	Inches
C	(0.875)	(0.034)
G	0.20	0.008
P	0.50	0.020
P1	1.00	0.039
X	0.20	0.008
X1	0.40	0.016
Y	0.68	0.027
Y1	(1.550)	(0.061)
Z	1.55	0.061

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