LITE-ON SEMICONDUCTOR

L04ESD5V0CP2

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE – **5.0** Volts
POWER DISSIPATION – **40** WATTS

GENERAL DESCRIPTION

The L04ESD5V0CP2 is designed to protect sensitive semiconductor components from damage or upset due to Electro Static Discharge (ESD).

FEATURES

- Protects one data or I/O line
- Max. peak pulse power : Ppp = 40W at tp = 8/20 us.
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air) ; > ±8KV (contact)

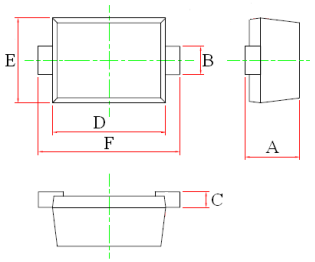
APPLICATION

- Computers and peripherals
- Communication system
- Audio & video equipment
- Portable Instrumentation

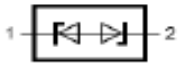
MECHANICAL DATA

- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E

SOD-923

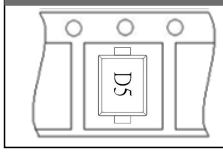


SOD-923		
DIM.	MIN.	MAX.
A	0.36	0.41
B	0.18	0.26
C	0.08	0.14
D	0.76	0.84
E	0.56	0.64
F	0.92	1.08
All Dimensions in millimeter		



PIN ASSIGNMENT	
1	Cathode
2	Cathode

Marking & Orientation



MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P_{pk}	40 (Max)	W
Peak Pulse Current (tp = 8/20us)	Ipp	3.5	A
Operating Junction Temperature Range	T_J	-55 to + 125	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	Mln	Typ	Max	Unit
Reverse standoff voltage	V_{RWM}		---	---	5.0	V
Breakdown voltage	VBR	I_R = 1 mA	5.5	---	8.5	V
Reverse leakage current	IRM	V_{DRM} = 5V	---	----	0.1	uA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs	---	---	9.0	V
Clamping Voltage	V_C	I_{PP} = 3.5A, tp = 8/20μs	---	---	12.5	V
Junction capacitance	C_J	V_R = 0V, f = 1MHz	---	4.5	---	pF

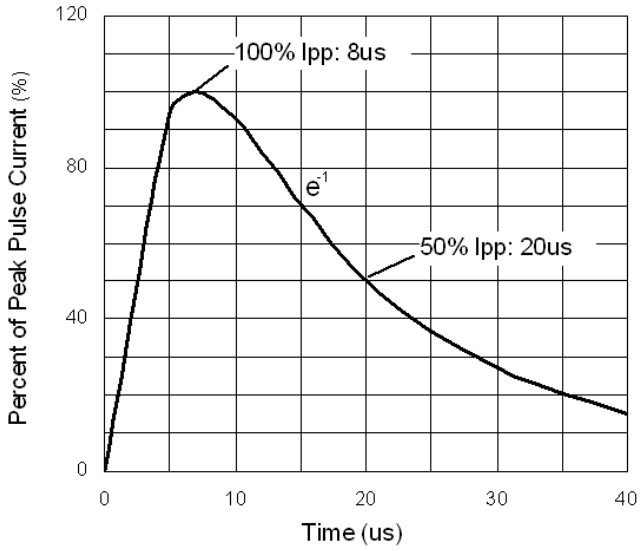


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

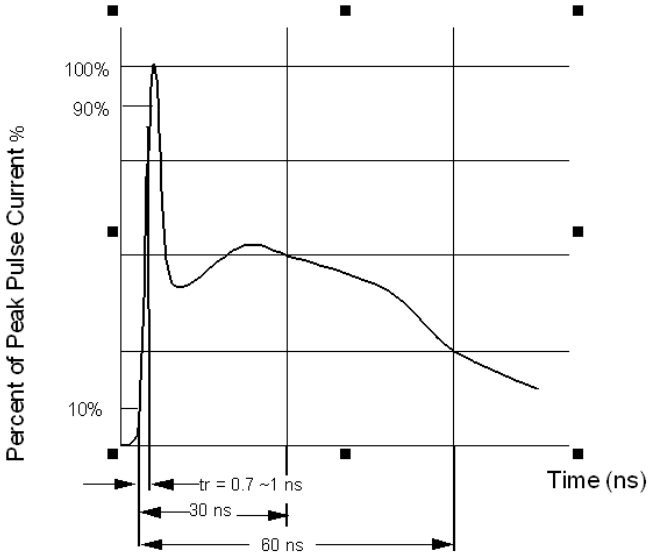


Figure 2. ESD pulse waveform according to IEC 61000-4-2

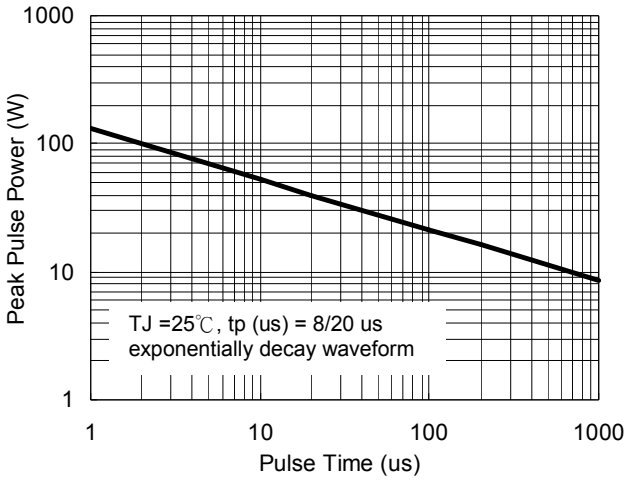


Figure 3. Power Dissipation versus Pulse Time

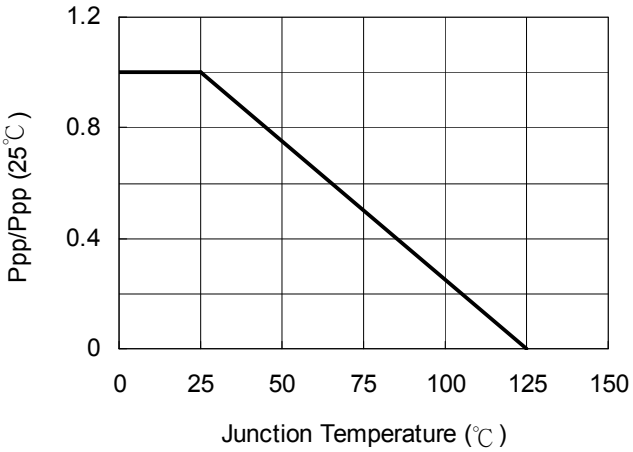


Figure 4. Peak pulse power versus TJ

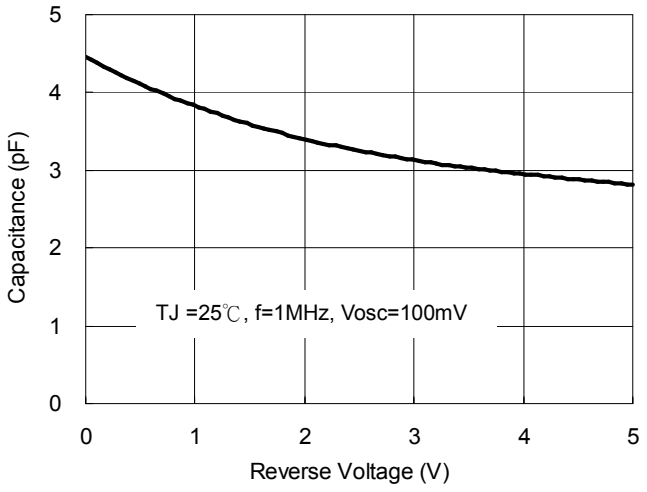


Figure 5. Typical Junction Capactiance

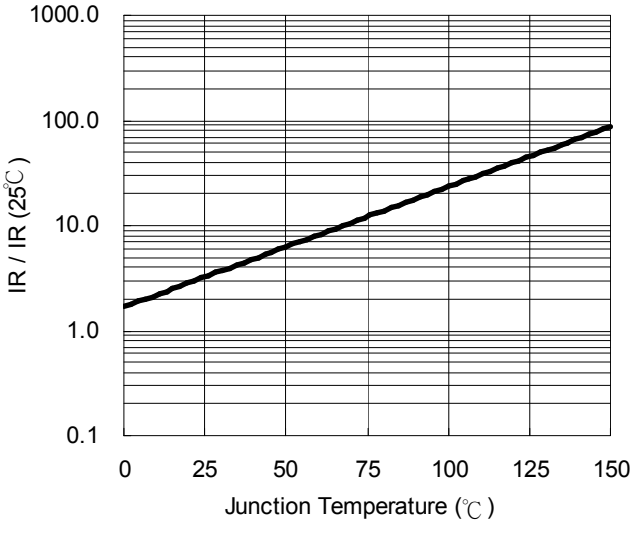


Figure 6. Reverse Leakage Current versus TJ

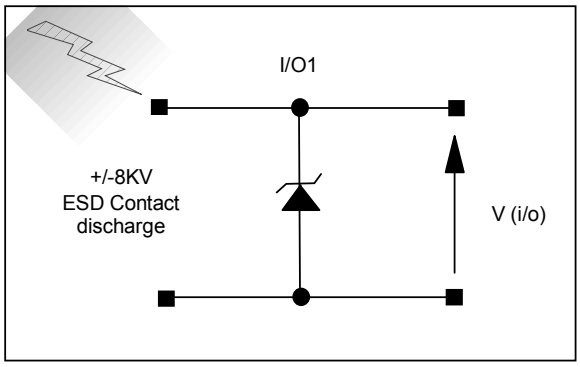


Figure 7. ESD Test Configuration

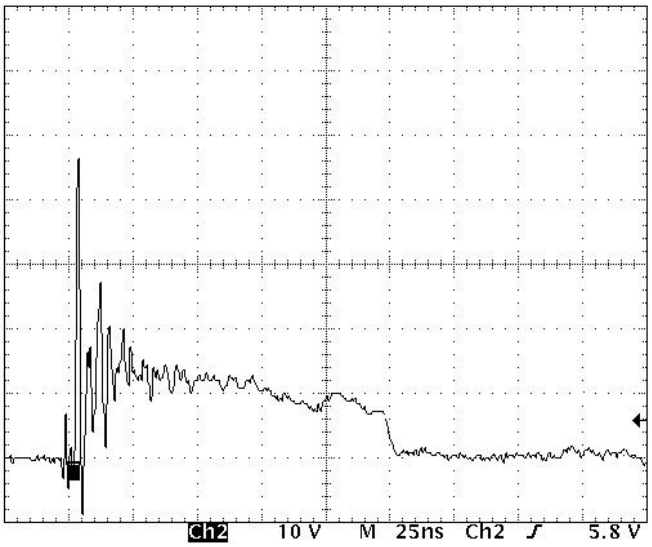


Figure 8. Clamped +8 kV ESD voltage waveform

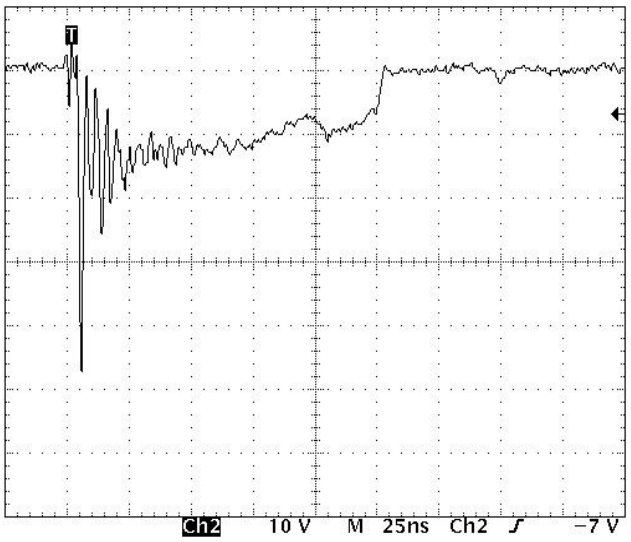


Figure 9. Clamped -8 kV ESD voltage waveform

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