LITE-ON SEMICONDUCTOR

L13ESD5V0CC5-4

BIDIRECTIONAL
ESD PROTECTION DIODE

STAND-OFF VOLTAGE - **5.0** Volts
POWER DISSIPATION - **130** WATTS

GENERAL DESCRIPTION

The L13ESD5V0CC5-4 is designed to protect sensitive electronics from damage or latch up due to ESD, lightning, and other voltage induced transient events. The device will protect four line operating at 5.0 volts.

FEATURES

- Bi-directional ESD Protectionof four line.
- Max. peak pulse power : Ppp = 130W at tp = 8/20 us
- Low clamping voltage.
- ESD protection > 25KV
- IEC 61000-4-2, level 4 (ESD), > 15KV (air) ; > 8KV (contact).
- IEC 61000-4-5, Ipp = 10A at tp = 8/20 us

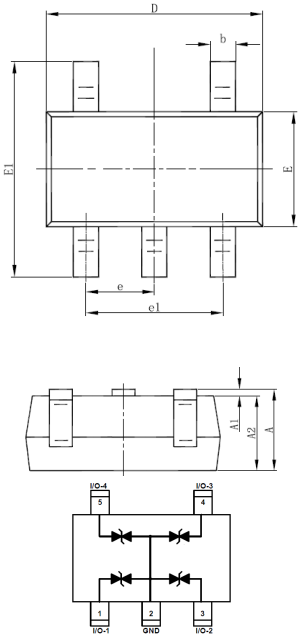
APPLICATION

- Computers and peripherals
- Communication system
- Audio & video equipment
- Portable instrumentation

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E

SOT23-5L



4 lines Protection

SOT23-5L		
DIM.	MIN.	MAX.
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
D	2.82	3.02
E	1.50	1.70
E1	2.65	2.95
e	0.95(BSC)	
e1	1.80	2.00
All Dimensions in millimeter		

PIN ASSIGNMENT	
1, 3, 4, 5	I/O Lines
2	Ground

MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak pulse Power (8/20us Waveform)	P_{PPM}	130	W
Peak Pulse Current (8/20us Waveform)	I_{PP}	10	A
Operating Junction Temperature Range	T_J	-55 to + 150	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	MIn	Max	Unit
Reverse standoff voltage	V_{DRM}	---	---	5.0	V
Reverse leakage current	I_{RM}	V_{DRM} = 5 V	---	100	nA
Breakdown voltage	V_{BR}	I_R = 1 mA	5.5	9.5	V
Junction capacitance(Each I/O pin and ground)	C_J	V_R = 0 V , f = 1MHz	---	15	pF
Clamping voltage	V_{CL}	I_{PP} = 1 A (8/20us)	---	10	V
Clamping voltage	V_{CL}	I_{PP} = 10 A (8/20us)	---	13	V

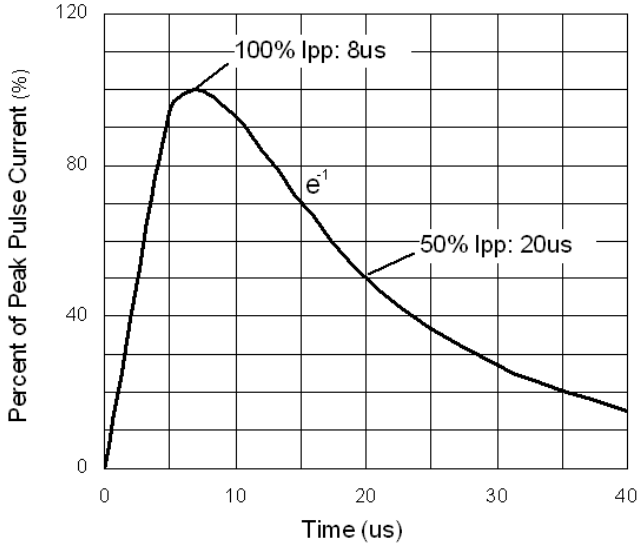


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

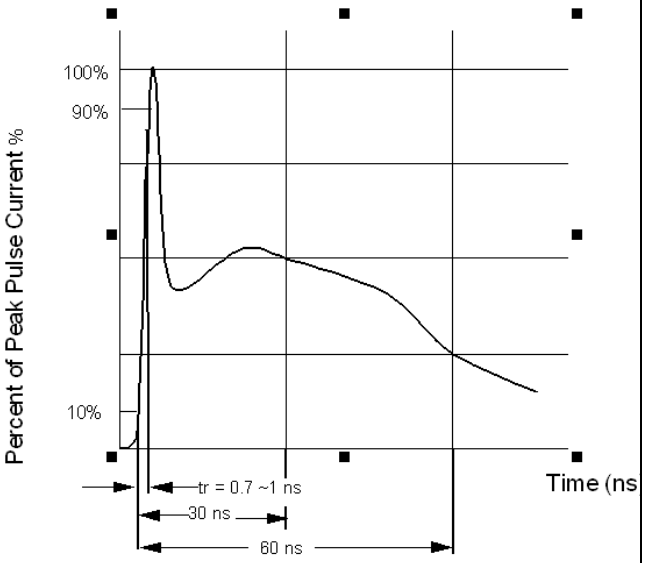


Figure 2. ESD pulse waveform according to IEC 61000-4-2

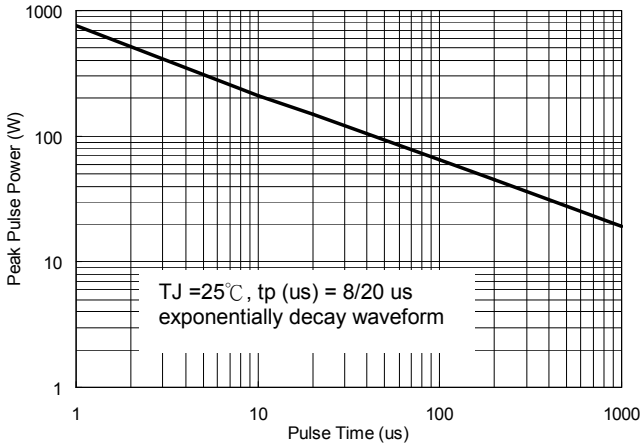


Figure 3. Power Dissipation versus Pulse Time

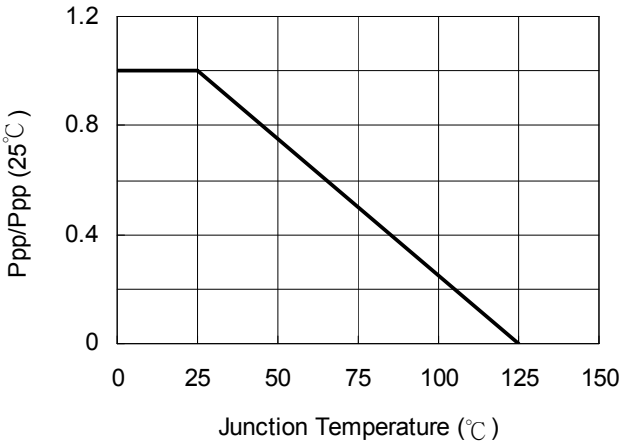


Figure 4. Peak pulse power versus TJ

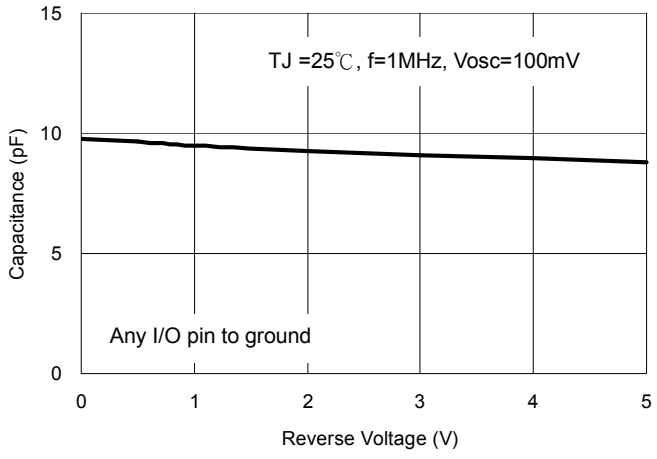


Figure 5. Typical Junction Capacitance

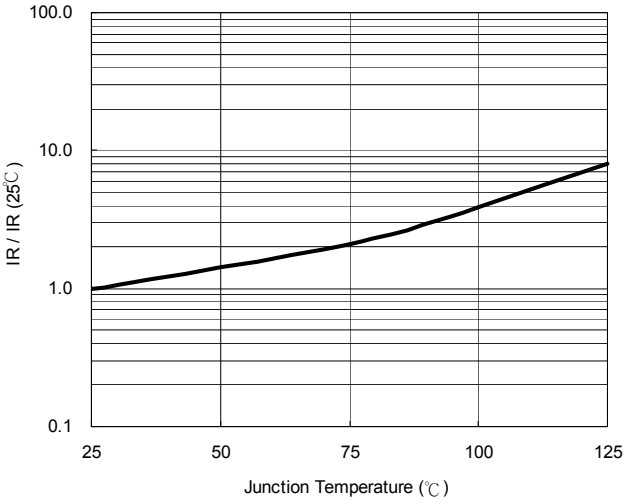


Figure 6. Reverse Leakage Current versus TJ

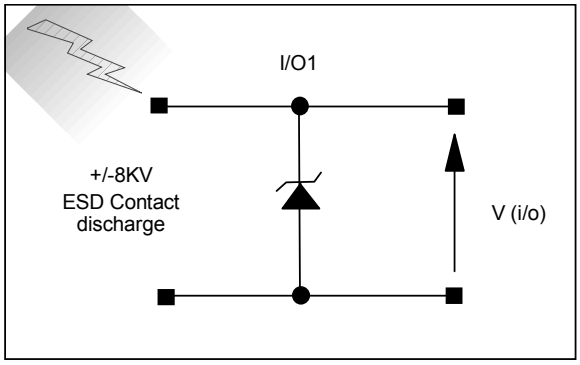


Figure 7. ESD Test Configuration

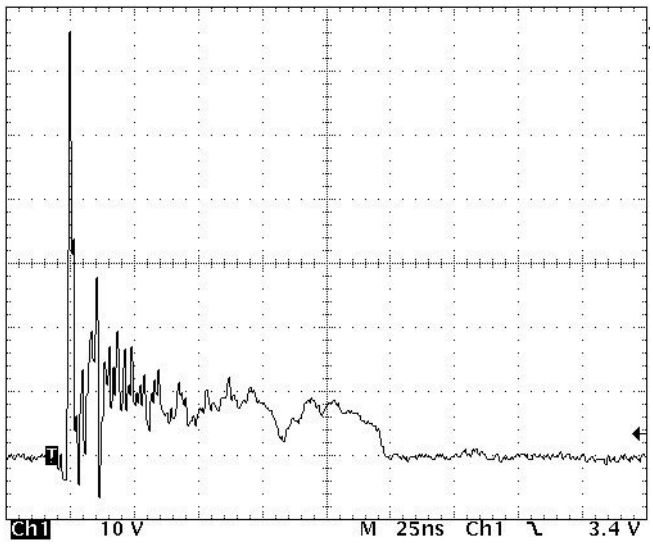


Figure 8. Clamped +8 kV ESD voltage waveform

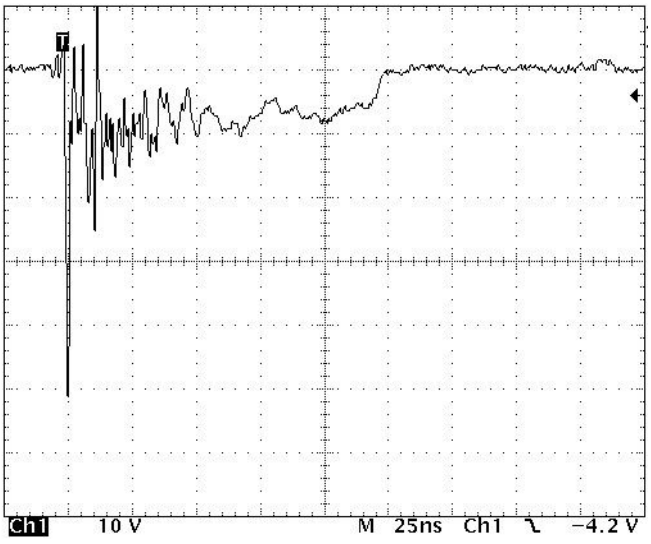


Figure 9. Clamped -8 kV ESD voltage waveform

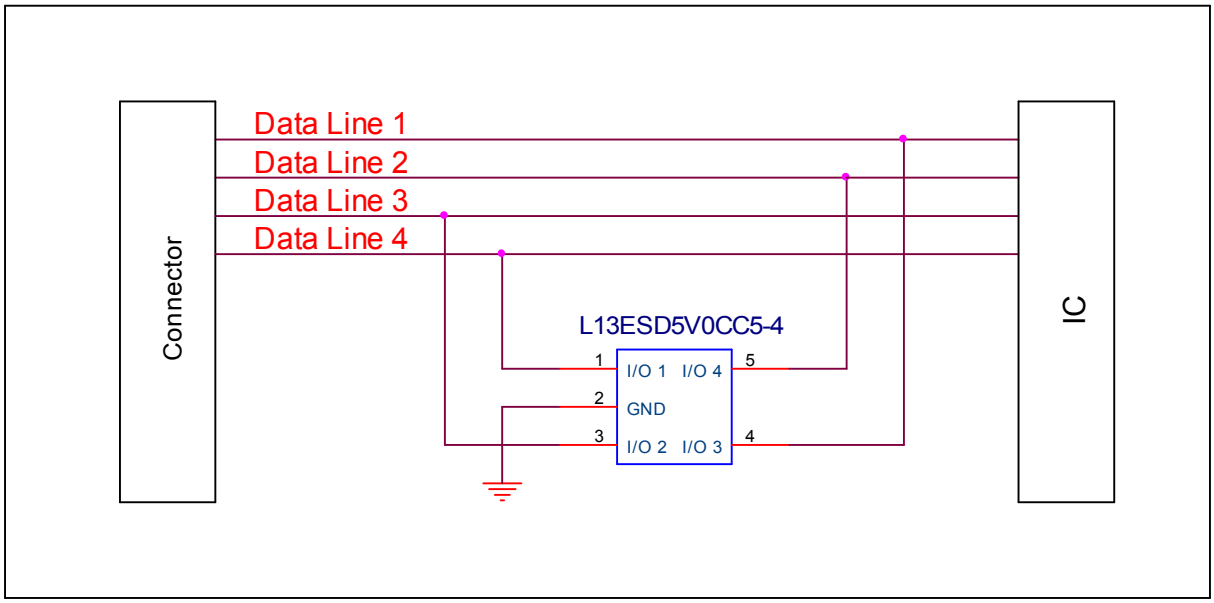
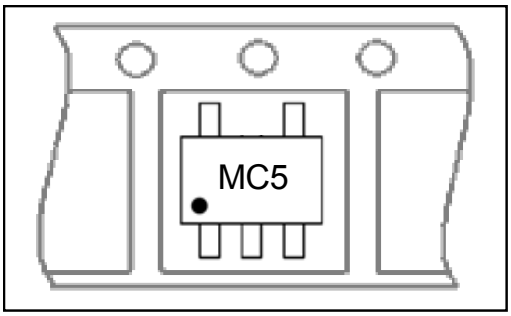


Figure 10. L13ESD5V0CC5-4 ESD Protection Circuit

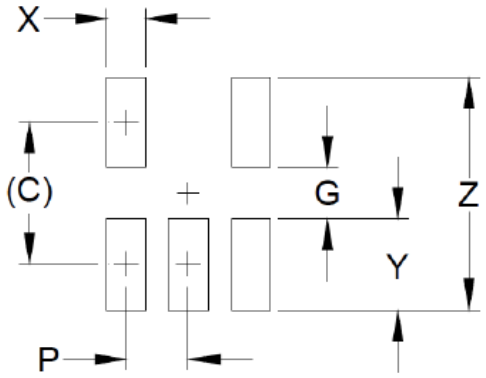
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L13ESD5V0CC5-4	3000	7	45000	90K/180K

SOT23-5L Soldering Pad Layout



Dim.	Millimeters	Inches
C	(2.50)	(0.098)
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141

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