LITE-ON SEMICONDUCTOR

L15ESDL5V0N6-2

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - **5.0** Volts
POWER DISSIPATION - **150** WATTS

GENERAL DESCRIPTION

The L15ESDL5V0N6-2 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Flow-Through design
- Protects two I/O lines (Data lines)
- Max. peak pulse power : Ppp = 150W at tp = 8/20 us.
- Low capacitance: 0.3pF typical (I/O to I/O)
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air) ; > ±8KV (contact).

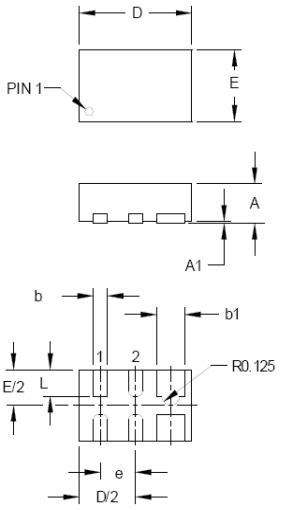
APPLICATION

- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interface (DVI)
- DisplayPort™ Interface
- MDDI Ports
- LVDS
- Serial ATA
- PCI Express

MECHANICAL DATA

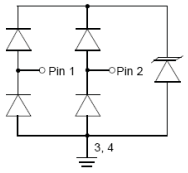
- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/EC

SLP1610P4



SLP1610P4		
DIM.	MIN.	MAX.
A	0.50	0.65
A1	0.00	0.05
b	0.15	0.25
b1	0.35	0.45
D	1.50	1.70
E	0.90	1.10
e	0.50 BSC	
L	0.30	0.43
All Dimensions in millimeter		

PIN ASSIGNMENT	
1,2	Input Lines
3,4	Ground
5,6	NC



2 lines Protection

MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P_{pk}	150 (Max)	W
Peak Pulse Current (tp = 8/20us)	Ipp	5.0	A
Operating Junction Temperature Range	T_J	-55 to + 125	℃
Storage Temperature Range	Tstg	-55 to + 150	℃
Soldering Temperature, t max = 10s	T_L	260	℃

ELECTRICAL CHARACTERISTICS (Tj= 25℃ unless otherwise noticed)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V_{RWM}	Any I/O pin to ground	--	---	5.0	V
Reverse leakage current	I_{RM}	VDRM = 5V	--	---	1.0	uA
Breakdown voltage	V_{BR}	IR = 1 mA	6.0	---	---	V
Clamping Voltage	Vc	Ipp=1A, tp = 8/20 us	---	---	15	V
Junction capacitance	CJ	VR = 0 V , f = 1MH Between I/O pins	---	0.3	0.4	pF
Junction capacitance	CJ	VR = 0 V , f = 1MHz Any I/O pin to ground	---	---	0.8	pF

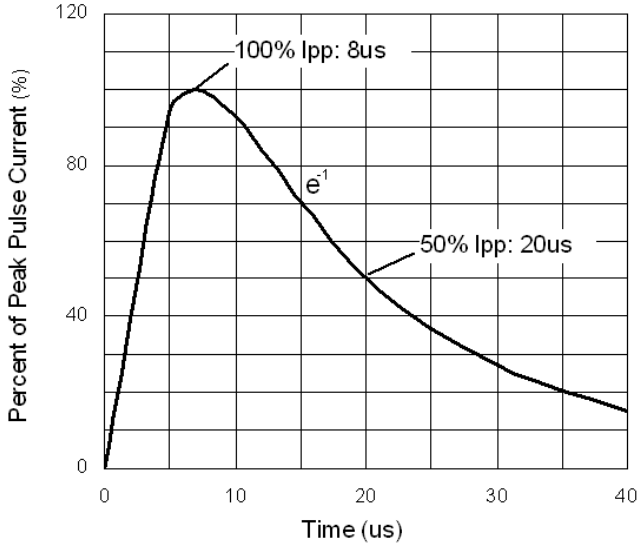


Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

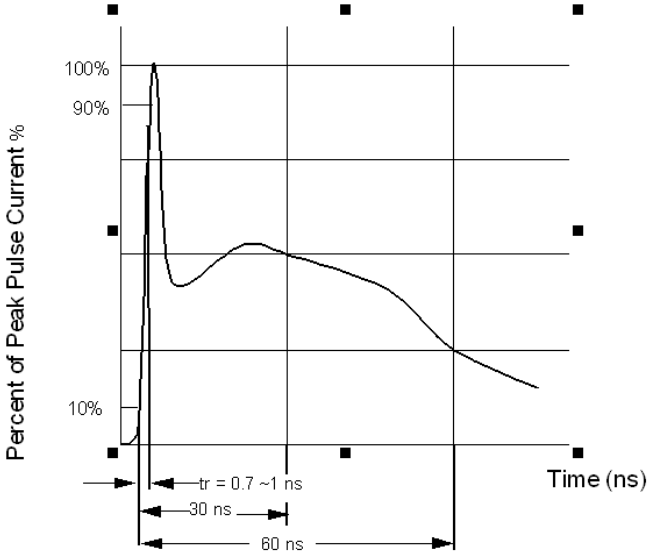


Figure 2. ESD pulse waveform according to IEC 61000-4-2

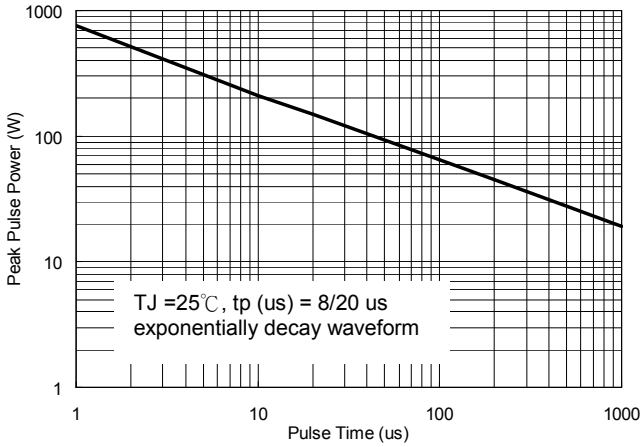


Figure 3. Power Dissipation versus Pulse Time

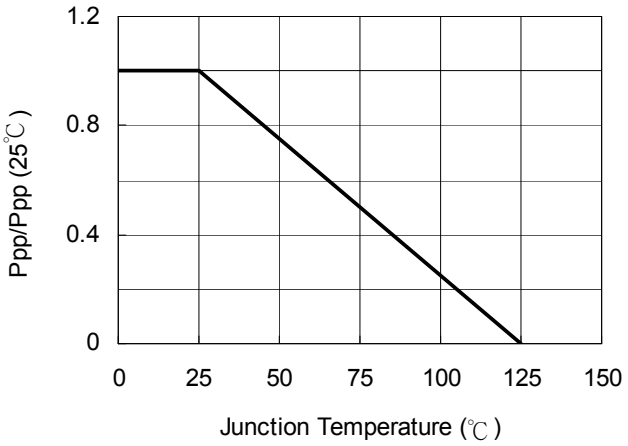


Figure 4. Peak pulse power versus TJ

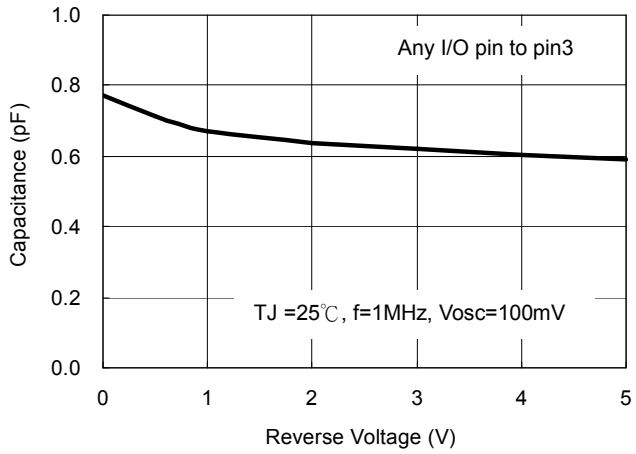


Figure 5. Typical Junction Capacitance

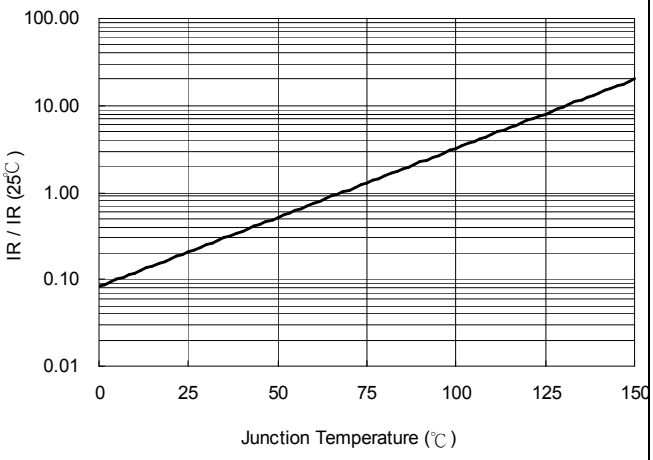


Figure 6. Reverse Leakage Current versus TJ

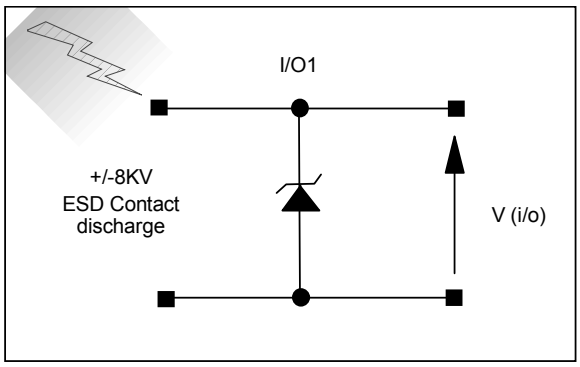


Figure 7. ESD Test Configuration

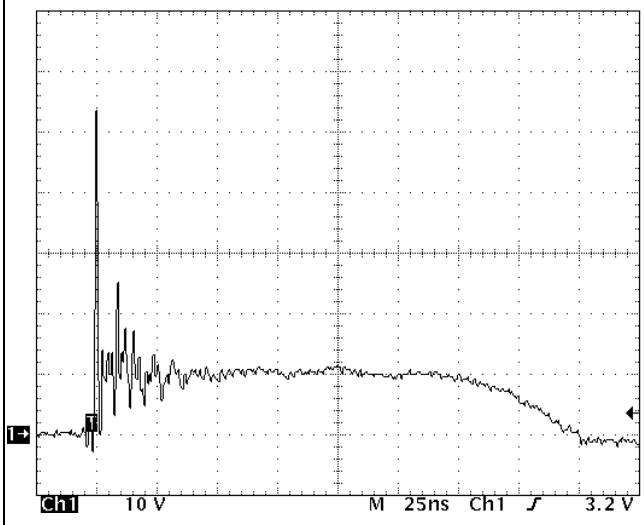


Figure 8. Clamped +8 kV ESD voltage waveform

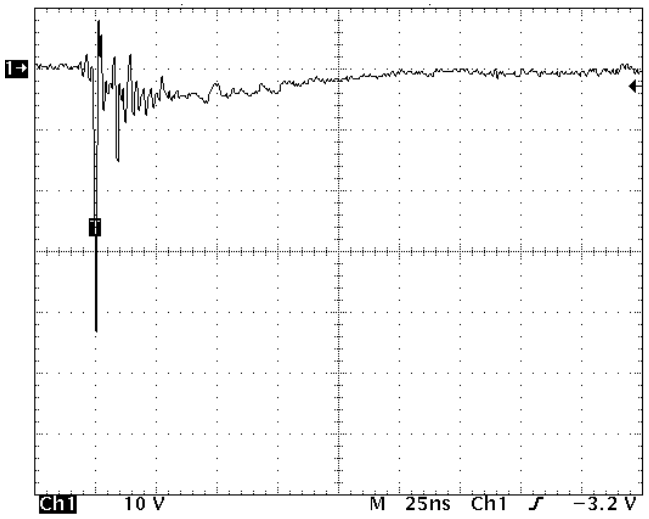


Figure 9. Clamped -8 kV ESD voltage waveform

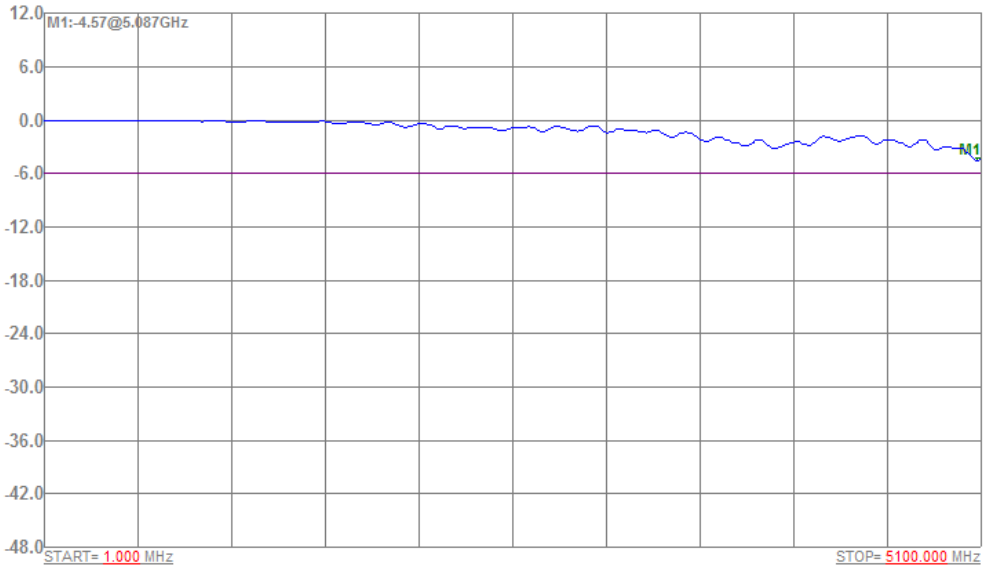
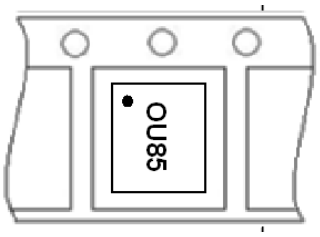


Figure 10. Insertion Loss (Each Line)

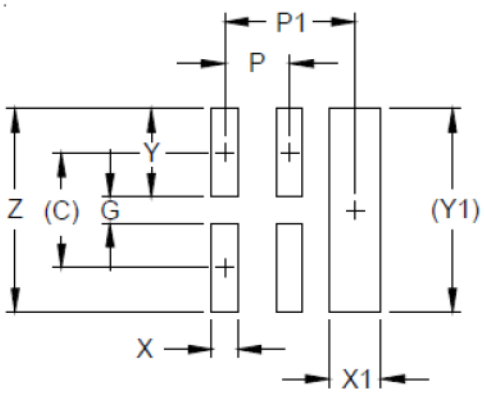
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L15ESDL5V0N6-2	3000	7	45000	90K/180K

SLP1610P4 Soldering Pad Layout



Dim.	Millimeters
C	(0.87)
G	0.19
P	0.50
P1	1.00
X	0.20
X1	0.40
Y	0.68
Y1	1.55
Z	1.55

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