



## L16B45A

Preliminary

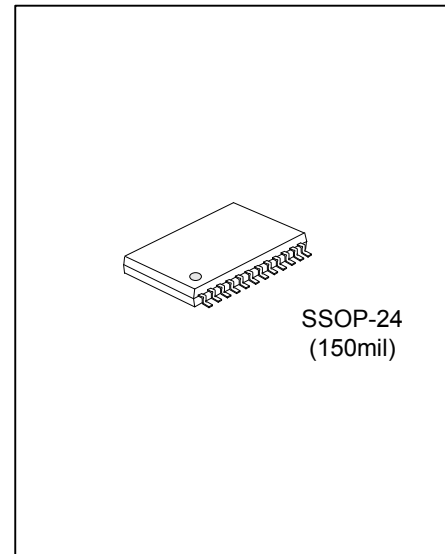
CMOS IC

### 16-BIT CONSTANT CURRENT LED SINK DRIVER

#### DESCRIPTION

The UTC **L16B45A** is designed for LED displays. UTC **L16B45A** contains a serial buffer and data latches which convert serial input data into parallel output format. At UTC **L16B45A** output stage, sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of  $V_f$  variations.

UTC **L16B45A** provides users with great flexibility and device performance while using UTC **L16B45A** in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 3mA to 45mA through an external resistor,  $R_{ext}$ , which gives users flexibility in controlling the light intensity of LEDs. UTC **L16B45A** guarantees to endure maximum 17V at the output port. The high clock frequency, 25MHz, also satisfies the system requirements of high volume data transmission.



#### FEATURES

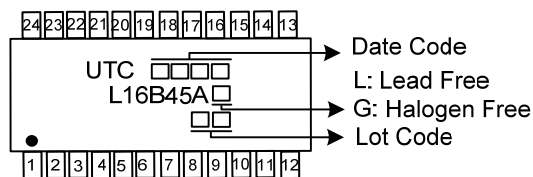
- \* 16 constant-current output channels
- \* Constant output current invariant to load voltage change  
Constant output current range:
  - 3~45mA @  $V_{DD}=5V$
  - 3~30mA @  $V_{DD}=3.3V$
- \* Excellent output current accuracy:
  - between channels:  $\pm 2.5\%$  (max.),
  - between ICs:  $\pm 3.0\%$  (max.)
- \* Output current adjusted through an external resistor
- \* Fast response of output current,  $\overline{OE}$  (min.): 70ns @  $V_{DD}=3.3V$
- \* 25MHz clock frequency
- \* Schmitt trigger input
- \* 3.3V/5V supply voltage
- \* Halogen Free

#### ORDERING INFORMATION

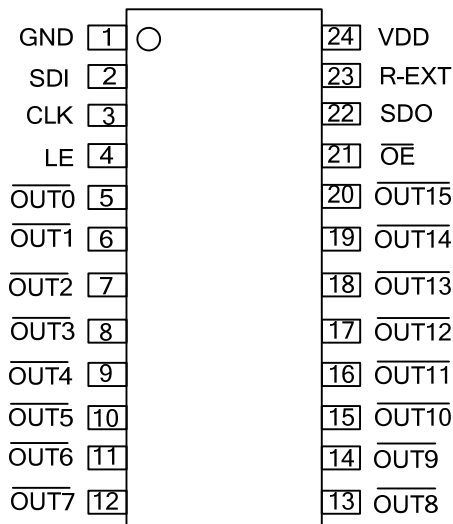
Ordering Number		Package	Packing
Lead Free	Halogen Free		
L16B45AL-R24-R	L16B45AG-R24-R	SSOP-24	Tape Reel

<p>L16B45AG-R24-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) R24: SSOP-24</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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### MARKING



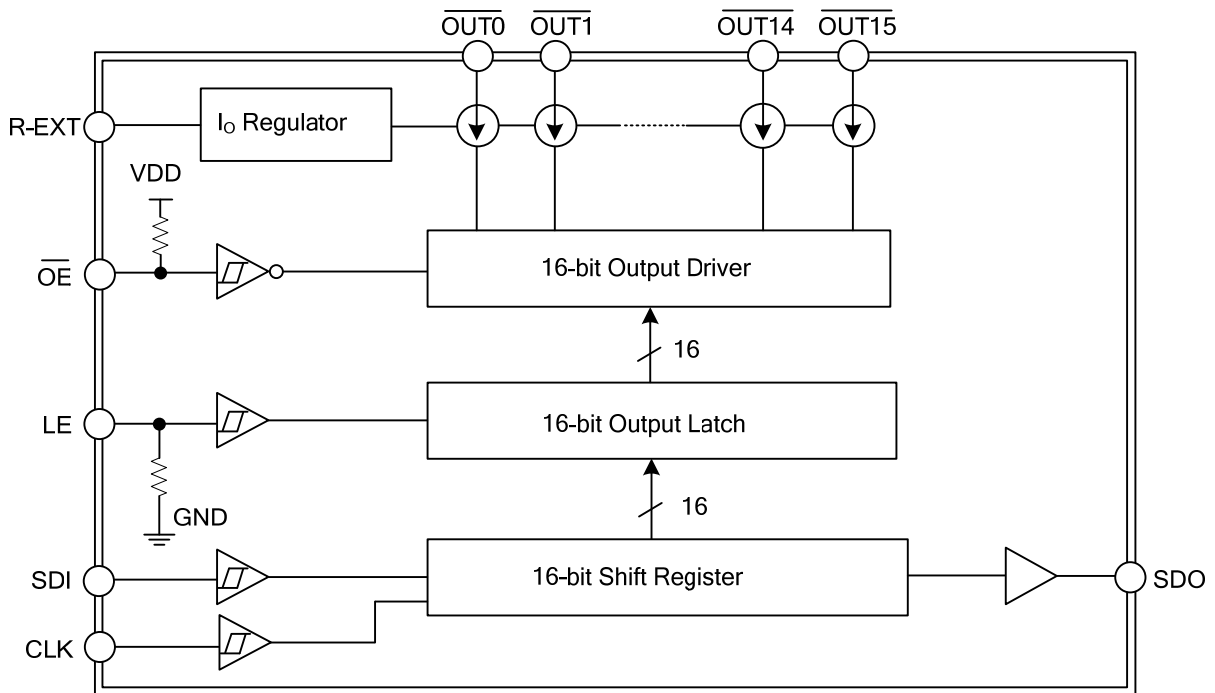
### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the output latch when LE is high. The data is latched when LE goes low.
5~20	$\overline{OUT0} \sim \overline{OUT15}$	Constant current output terminals
21	$\overline{OE}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
24	V <sub>DD</sub>	3.5V/5V supply voltage terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	0 ~ 7.0	V
Input Voltage	$V_{IN}$	-0.4 ~ $V_{DD}+0.4$	V
Output Current	$I_{OUT}$	+45	mA
Output Voltage	$V_{DS}$	-0.5 ~ +17.0	V
GND Terminal Current	$I_{GND}$	720	mA
Power Dissipation (On PCB, $T_A=25^{\circ}C$ )	$P_D$	1.37	W
Thermal Resistance (On PCB, $T_A=25^{\circ}C$ )	$\theta_{JA}$	91	$^{\circ}C/W$
Junction Temperature	$T_J$	+150	$^{\circ}C$
Operating Temperature	$T_{OPR}$	-40 ~ +85	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DC ELECTRICAL CHARACTERISTICS ( $V_{DD}=5.0V$ )

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		$V_{DD}$		4.5	5.0	5.5	V
Output Voltage		$V_{DS}$	$\overline{OUT0} \sim \overline{OUT15}$			17.0	V
Output Current		$I_{OUT}$	DC Test Circuit	3		45	mA
		$I_{OH}$	SDO			-1.0	mA
		$I_{OL}$	SDO			1.0	mA
Input Voltage	"H" Level	$V_{IH}$	$T_A=-40\sim 85^{\circ}C$	$0.7 \times V_{DD}$		$V_{DD}$	V
	"L" Level	$V_{IL}$	$T_A=-40\sim 85^{\circ}C$	GND		$0.3 \times V_{DD}$	V
Output Leakage Current		$I_{OH}$	$V_{DS}=17.0V$		0.5		$\mu A$
Output Voltage	SDO	$V_{OL}$	$I_{OL}=+1.0mA$		0.4		V
		$V_{OH}$	$I_{OH}=-1.0mA$		4.6		V
Output Current 1		$I_{OUT1}$	$V_{DS}=1.0V, R_{EXT}=6000\Omega$		3.1		mA
Current Skew		$dI_{OUT1}$	$I_{OL}=3.1mA, V_{DS}=1.0V, R_{EXT}=6000\Omega$		$\pm 2.5$		%
Output Current 2		$I_{OUT2}$	$V_{DS}=1.0V, R_{EXT}=720\Omega$		25.8		mA
Current Skew		$dI_{OUT2}$	$I_{OL}=25.8mA, V_{DS}=1.0V, R_{EXT}=720\Omega$		$\pm 2$		%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	$V_{DS}=1.0\sim 3.0V$		$\pm 0.1$		$\%/V$
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	$V_{DD}=4.5\sim 5.5V$		$\pm 1.0$		$\%/V$
Pull-Up Resistor		$R_{IN(up)}$	$\overline{OE}$	250	500	800	K $\Omega$
Pull-Down Resistor		$R_{IN(down)}$	LE	250	500	800	K $\Omega$
Supply Current	"OFF"	$I_{DD(off) 1}$	$R_{EXT}=\text{Open}, \overline{OUT0} \sim \overline{OUT15}=\text{Off}$		2	2.8	mA
		$I_{DD(off) 2}$	$R_{EXT}=1240\Omega, \overline{OUT0} \sim \overline{OUT15}=\text{Off}$		4	4.8	mA
		$I_{DD(off) 3}$	$R_{EXT}=620\Omega, \overline{OUT0} \sim \overline{OUT15}=\text{Off}$		6	6.8	mA
	"ON"	$I_{DD(on) 1}$	$R_{EXT}=1240\Omega, \overline{OUT0} \sim \overline{OUT15}=\text{On}$		5.2	8.2	mA
		$I_{DD(on) 2}$	$R_{EXT}=620\Omega, \overline{OUT0} \sim \overline{OUT15}=\text{On}$		6.5	9.5	mA

■ DC ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=3.3V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V <sub>DD</sub>		3.0	3.3	4.5	V
Output Voltage		V <sub>DS</sub>	OUT0 ~ OUT15			17.0	V
Output Current		I <sub>OUT</sub>	DC Test Circuit	3		30	mA
		I <sub>OH</sub>	SDO			-1.0	mA
		I <sub>OL</sub>	SDO			1.0	mA
Input Voltage	"H" Level	V <sub>IH</sub>	T <sub>A</sub> =-40~85°C	0.7×V <sub>DD</sub>		V <sub>DD</sub>	V
	"L" Level	V <sub>IL</sub>	T <sub>A</sub> =-40~85°C	GND		0.3×V <sub>DD</sub>	V
Output Leakage Current		I <sub>OH</sub>	V <sub>DS</sub> =17.0V		0.5		μA
Output Voltage	SDO	V <sub>OL</sub>	I <sub>OL</sub> =+1.0mA		0.4		V
		V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA		2.9		V
Output Current 1		I <sub>OUT1</sub>	V <sub>DS</sub> =1.0V, R <sub>EXT</sub> =6000Ω		3.1		mA
Current Skew		dI <sub>OUT1</sub>	I <sub>OL</sub> =3.1mA, V <sub>DS</sub> =1.0V, R <sub>EXT</sub> =6000Ω		±2.5		%
Output Current 2		I <sub>OUT2</sub>	V <sub>DS</sub> =1.0V, R <sub>EXT</sub> =720Ω		25.8		mA
Current Skew		dI <sub>OUT2</sub>	I <sub>OL</sub> =25.8mA, V <sub>DS</sub> =1.0V, R <sub>EXT</sub> =720Ω		±2		%
Output Current vs. Output Voltage Regulation		%/dV <sub>DS</sub>	V <sub>DS</sub> =1.0~3.0V		±0.1		%/V
Output Current vs. Supply Voltage Regulation		%/dV <sub>DD</sub>	V <sub>DD</sub> =3.0~3.6V		±1.0		%/V
Pull-Up Resistor		R <sub>IN(up)</sub>	$\overline{OE}$	250	500	800	KΩ
Pull-Down Resistor		R <sub>IN(down)</sub>	LE	250	500	800	KΩ
Supply Current	"OFF"	I <sub>DD(off) 1</sub>	R <sub>EXT</sub> =Open, $\overline{OUT0} \sim \overline{OUT15}$ =Off		1.7	2.3	mA
		I <sub>DD(off) 2</sub>	R <sub>EXT</sub> =1851Ω, $\overline{OUT0} \sim \overline{OUT15}$ =Off		3.9	4.5	mA
		I <sub>DD(off) 3</sub>	R <sub>EXT</sub> =748Ω, $\overline{OUT0} \sim \overline{OUT15}$ =Off		5.2	5.8	mA
	"ON"	I <sub>DD(on) 1</sub>	R <sub>EXT</sub> =1851Ω, $\overline{OUT0} \sim \overline{OUT15}$ =On		3.9	5.0	mA
		I <sub>DD(on) 2</sub>	R <sub>EXT</sub> =748Ω, $\overline{OUT0} \sim \overline{OUT15}$ =On		5.2	5.8	mA

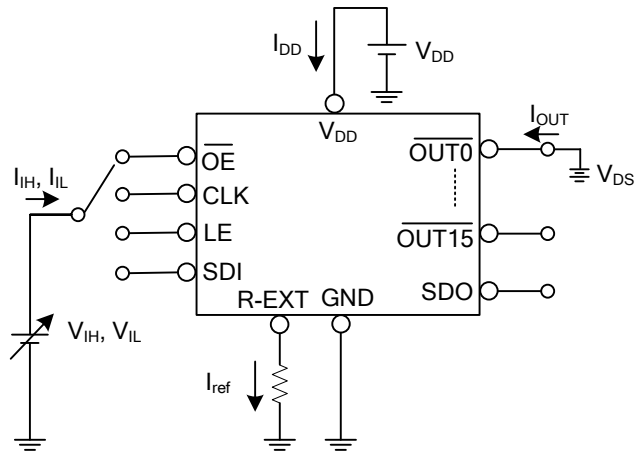
■ SWITCHING ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=5.0V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK- OUT2n	t <sub>pLH1</sub>	V <sub>DD</sub> =5.0V, V <sub>DS</sub> =1.0V, V <sub>IH</sub> =V <sub>DD</sub> , V <sub>IL</sub> =GND R <sub>ext</sub> =930Ω, V <sub>L</sub> =4.5V, R <sub>L</sub> =162Ω, C <sub>L</sub> =10pF		50	70	ns
	CLK- OUT2n+1				35	55	ns
	LE- OUT2n	t <sub>pLH2</sub>			50	70	ns
	LE- OUT2n+1				35	55	ns
	OE - OUT2n	t <sub>pLH3</sub>			50	70	ns
	OE - OUT2n+1				35	55	ns
	CLK-SDO	t <sub>pLH</sub>			20	40	ns
Propagation Delay Time ("H" to "L")	CLK- OUT2n	t <sub>pHL1</sub>			90	110	ns
	CLK- OUT2n+1				75	95	ns
	LE- OUT2n	t <sub>pHL2</sub>			90	110	ns
	LE- OUT2n+1				75	95	ns
	OE - OUT2n	t <sub>pHL3</sub>			90	110	ns
	OE - OUT2n+1				75	95	ns
	CLK-SDO	t <sub>pHL</sub>			20	40	ns
Pulse Width	CLK	t <sub>w(CLK)</sub>		20		ns	
	LE	t <sub>w(L)</sub>		20		ns	
	OE	t <sub>w(OE)</sub>		70	100	ns	
Hold Time for LE		t <sub>h(L)</sub>		30		ns	
Setup Time for LE		t <sub>su(L)</sub>		5		ns	
Hold Time for SDI		t <sub>h(D)</sub>		5		ns	
Setup Time for SDI		t <sub>su(D)</sub>		3		ns	
Maximum CLK Rise Time		t <sub>r</sub>				500 ns	
Maximum CLK Fall Time		t <sub>f</sub>				500 ns	
SDO Rise Time		t <sub>r, SDO</sub>		10		ns	
SDI Fall Time		t <sub>f, SDO</sub>		10		ns	
Output Rise Time of I <sub>OUT</sub>		t <sub>or</sub>		40		ns	
Output Fall Time of I <sub>OUT</sub>		t <sub>of</sub>		55		ns	

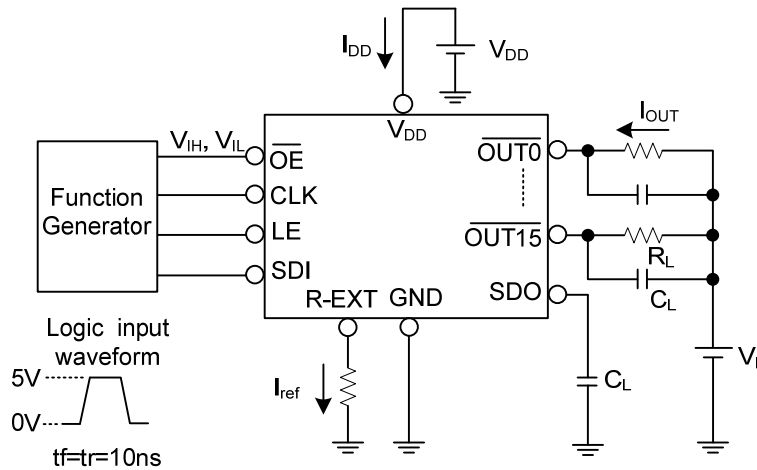
■ SWITCHING ELECTRICAL CHARACTERISTICS ( $V_{DD}=3.3V$ )

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time ("L" to "H")	CLK- $\overline{OUT2n}$	$t_{pLH1}$	$V_{DD}=3.3V, V_{DS}=1.0V, V_{IH}=V_{DD}, V_{IL}=GND$ $R_{ext}=930\Omega, V_L=3.0V, R_L=100\Omega, C_L=10pF$		50	70	ns
	CLK- $\overline{OUT2n+1}$				35	55	ns
	LE- $\overline{OUT2n}$	$t_{pLH2}$			50	70	ns
	LE- $\overline{OUT2n+1}$				35	55	ns
	$\overline{OE}$ - $\overline{OUT2n}$	$t_{pLH3}$			50	70	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				35	55	ns
	CLK-SDO	$t_{pLH}$			20	40	ns
Propagation Delay Time ("H" to "L")	CLK- $\overline{OUT2n}$	$t_{pHL1}$			115	135	ns
	CLK- $\overline{OUT2n+1}$				100	120	ns
	LE- $\overline{OUT2n}$	$t_{pHL2}$			115	135	ns
	LE- $\overline{OUT2n+1}$				100	120	ns
	$\overline{OE}$ - $\overline{OUT2n}$	$t_{pHL3}$			105	125	ns
	$\overline{OE}$ - $\overline{OUT2n+1}$				90	110	ns
	CLK-SDO	$t_{pHL}$			20	40	ns
Pulse Width	CLK	$t_{w(CLK)}$		20		ns	
	LE	$t_{w(L)}$		20		ns	
	$\overline{OE}$	$t_{w(OE)}$		100	130	ns	
Hold Time for LE	$t_{h(L)}$		30		ns		
Setup Time for LE	$t_{su(L)}$		5		ns		
Hold Time for SDI	$t_{h(D)}$		5		ns		
Setup Time for SDI	$t_{su(D)}$		3		ns		
Maximum CLK Rise Time	$t_r$				500	ns	
Maximum CLK Fall Time	$t_f$				500	ns	
SDO Rise Time	$t_{r, SDO}$			10		ns	
SDI Fall Time	$t_{f, SDO}$			10		ns	
Output Rise Time of $I_{OUT}$	$t_{or}$			40		ns	
Output Fall Time of $I_{OUT}$	$t_{of}$			65		ns	

■ TEST CIRCUIT FOR DC ELECTRICAL CHARACTERISTICS

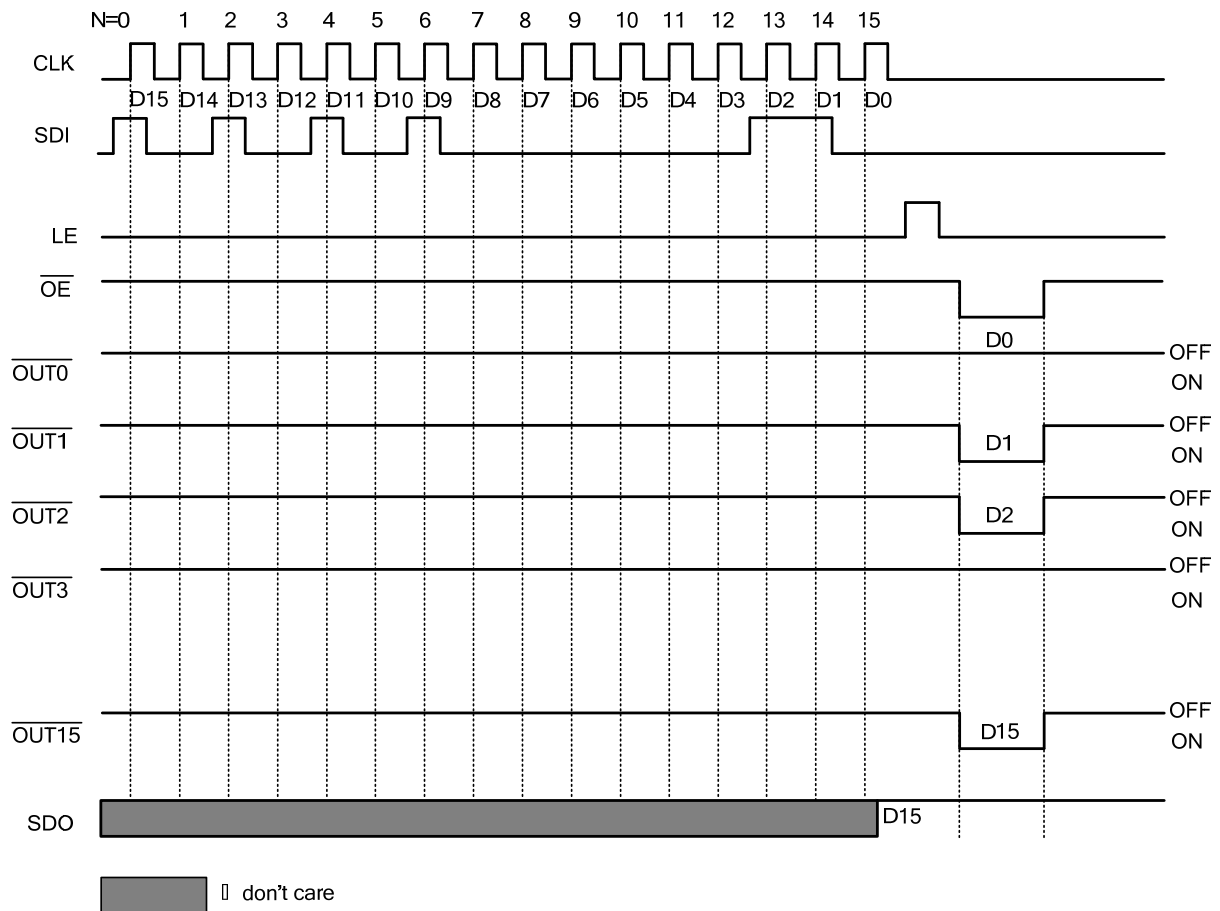


■ TEST CIRCUIT FOR SWITCHING ELECTRICAL CHARACTERISTICS





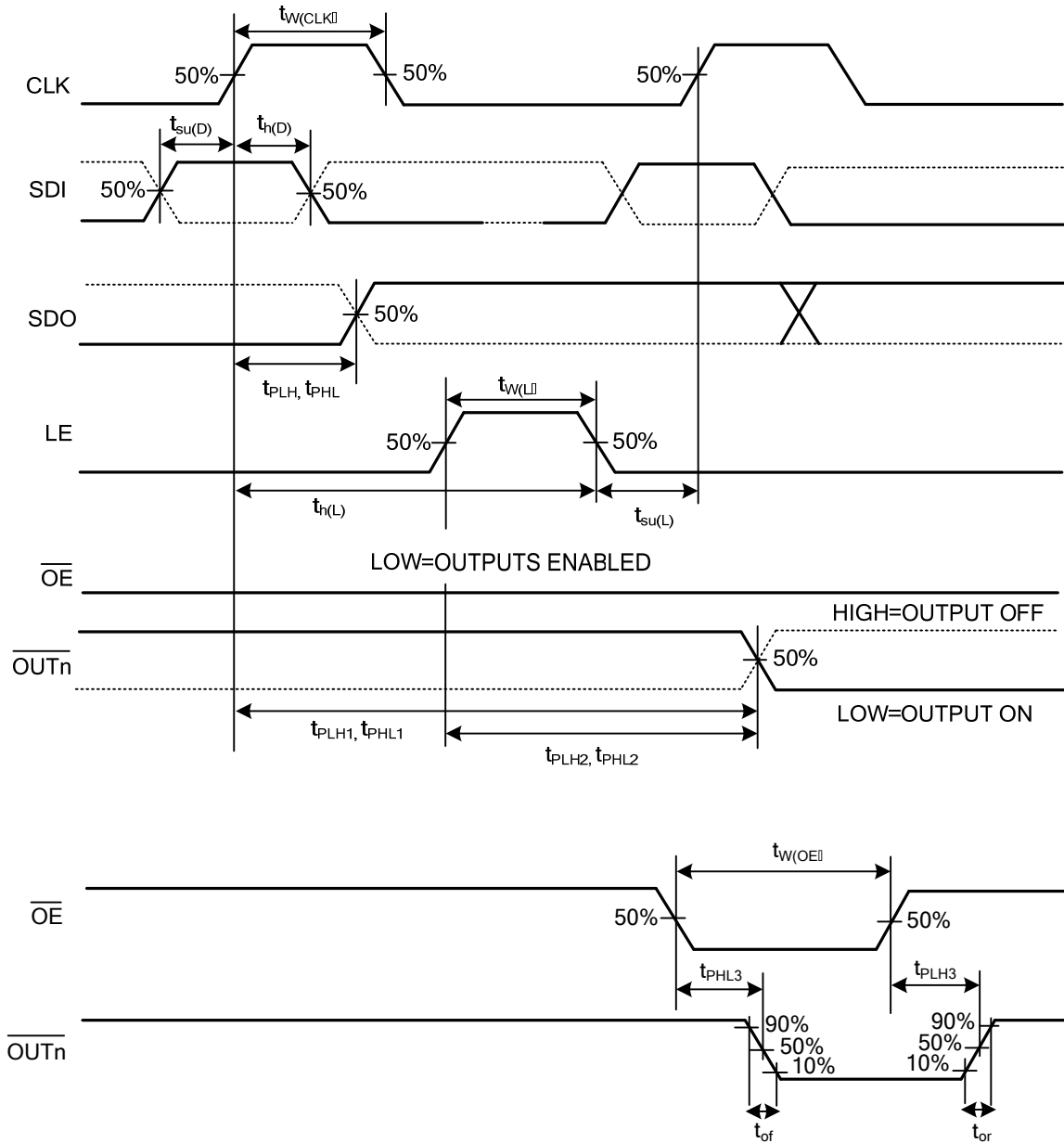
### ■ TIMING DIAGRAM



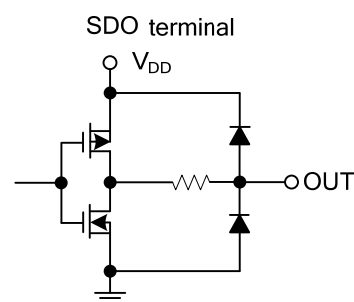
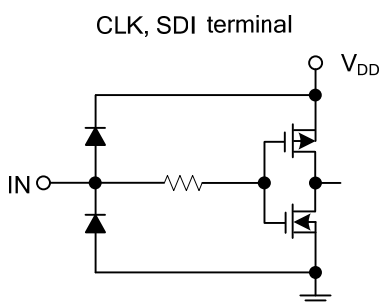
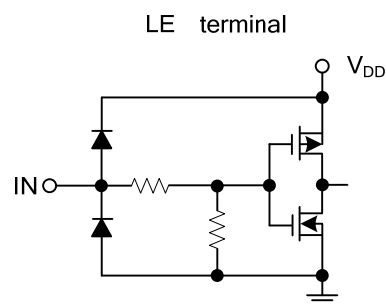
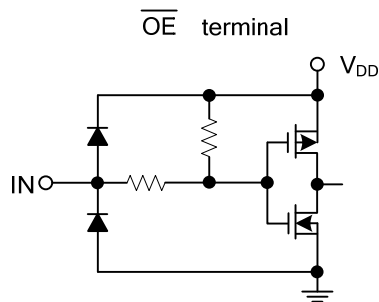
### ■ TRUTH TABLE

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0} \dots \overline{OUT7} \dots \overline{OUT15}$	SDO
	H	L	$D_n$	$\overline{D_n} \dots \overline{D_{n-7}} \dots \overline{D_{n-15}}$	$D_{n-15}$
	L	L	$D_{n+1}$	No Change	$D_{n-14}$
	H	L	$D_{n+2}$	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	$D_{n-13}$
	X	L	$D_{n+3}$	$\overline{D_{n+2}} \dots \overline{D_{n-5}} \dots \overline{D_{n-13}}$	$D_{n-13}$
	X	H	$D_{n+3}$	Off	$D_{n-13}$

■ TIMING WAVEFORM



■ EQUIVALENT CIRCUITS OF INPUTS AND OUTPUTS



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